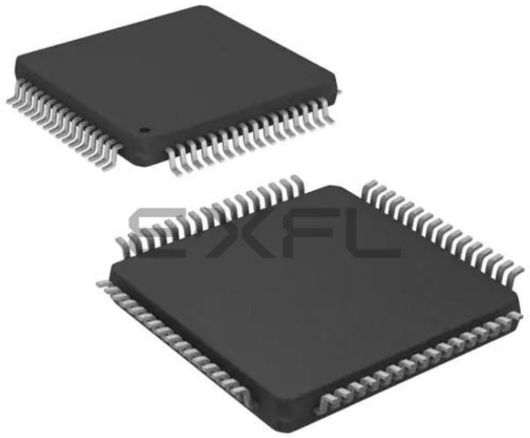
Silicon Labs - EFM32G232F128G-E-QFP64 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g232f128g-e-qfp64

3. System Overview

3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32G devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32G Reference Manual.

The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

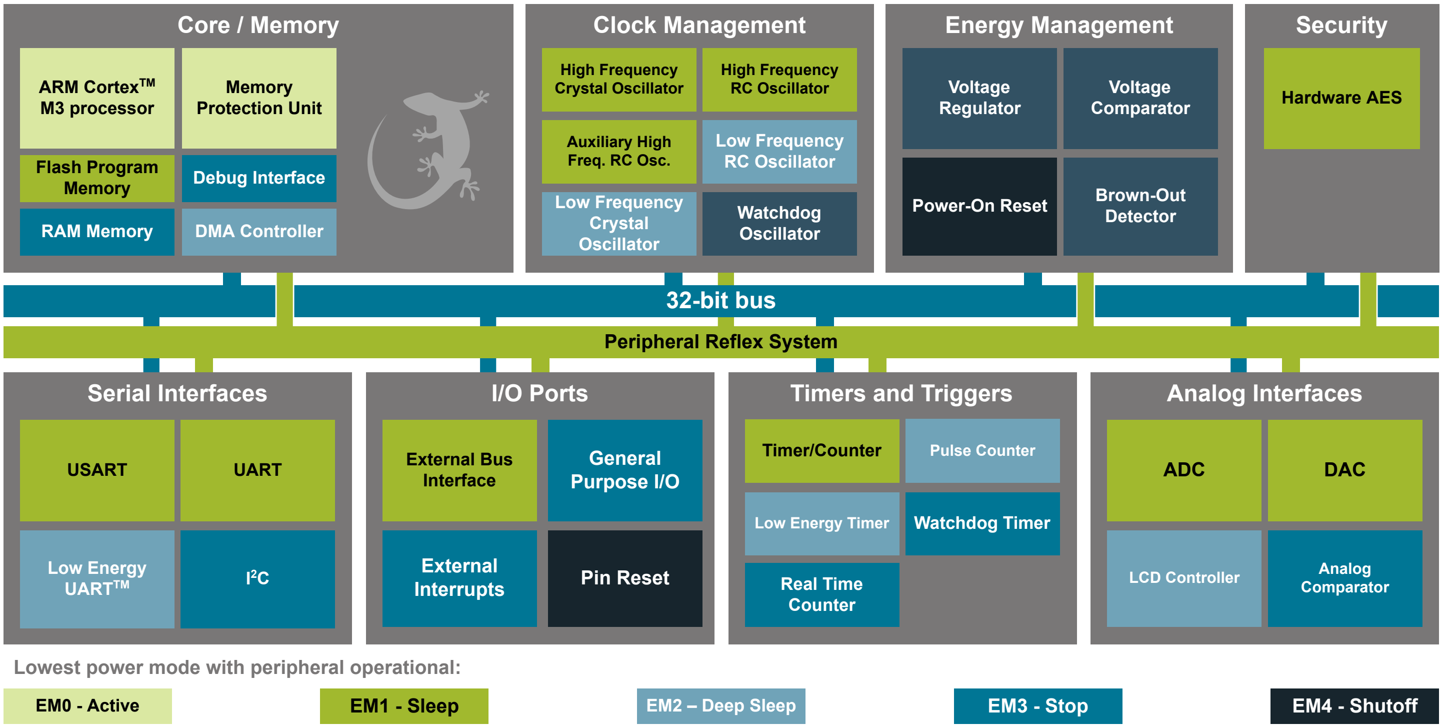


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32G Reference Manual.

3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

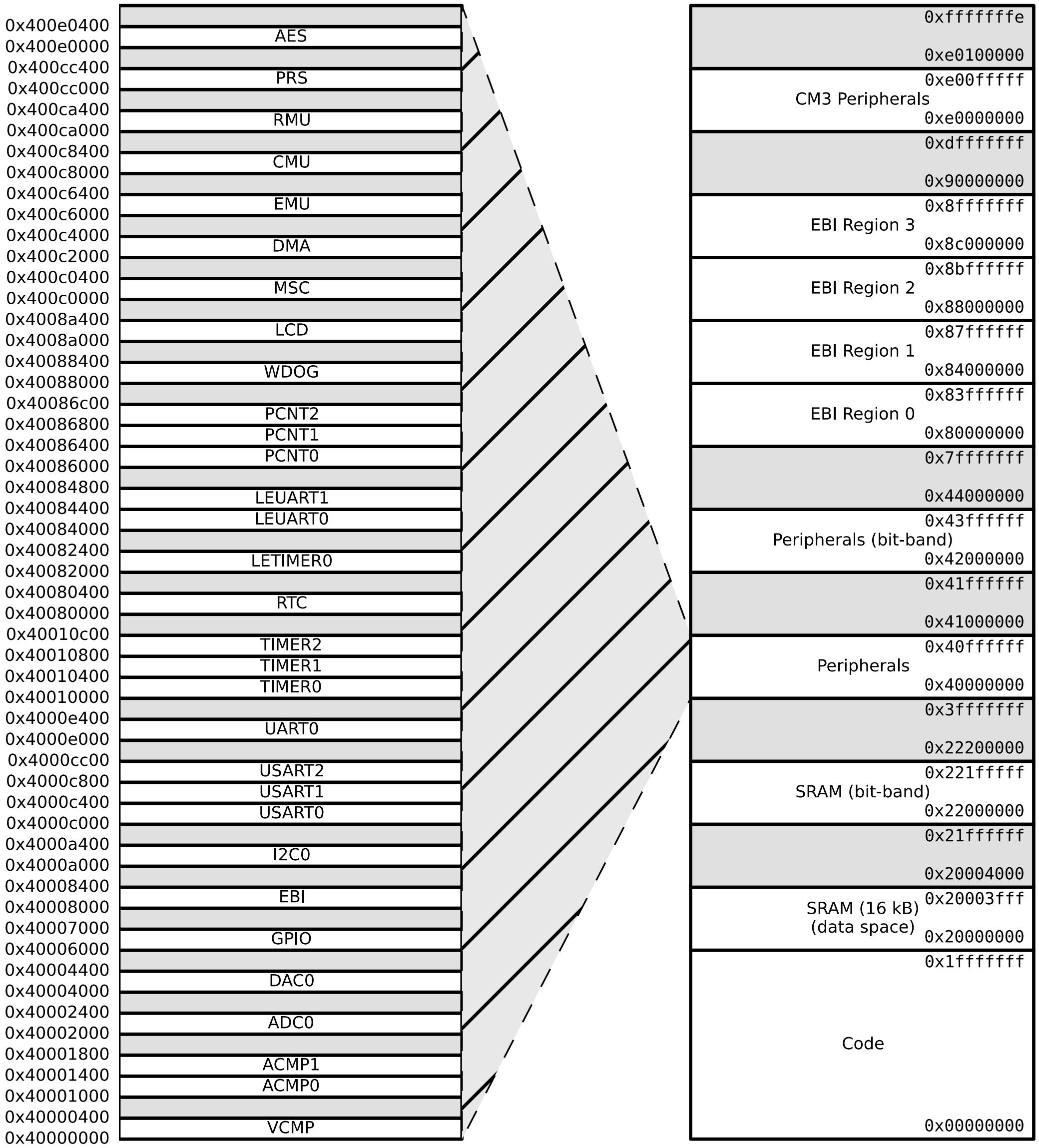


Figure 3.3. System Address Space with Peripheral Listing

4.4.2 EM1 Current Consumption

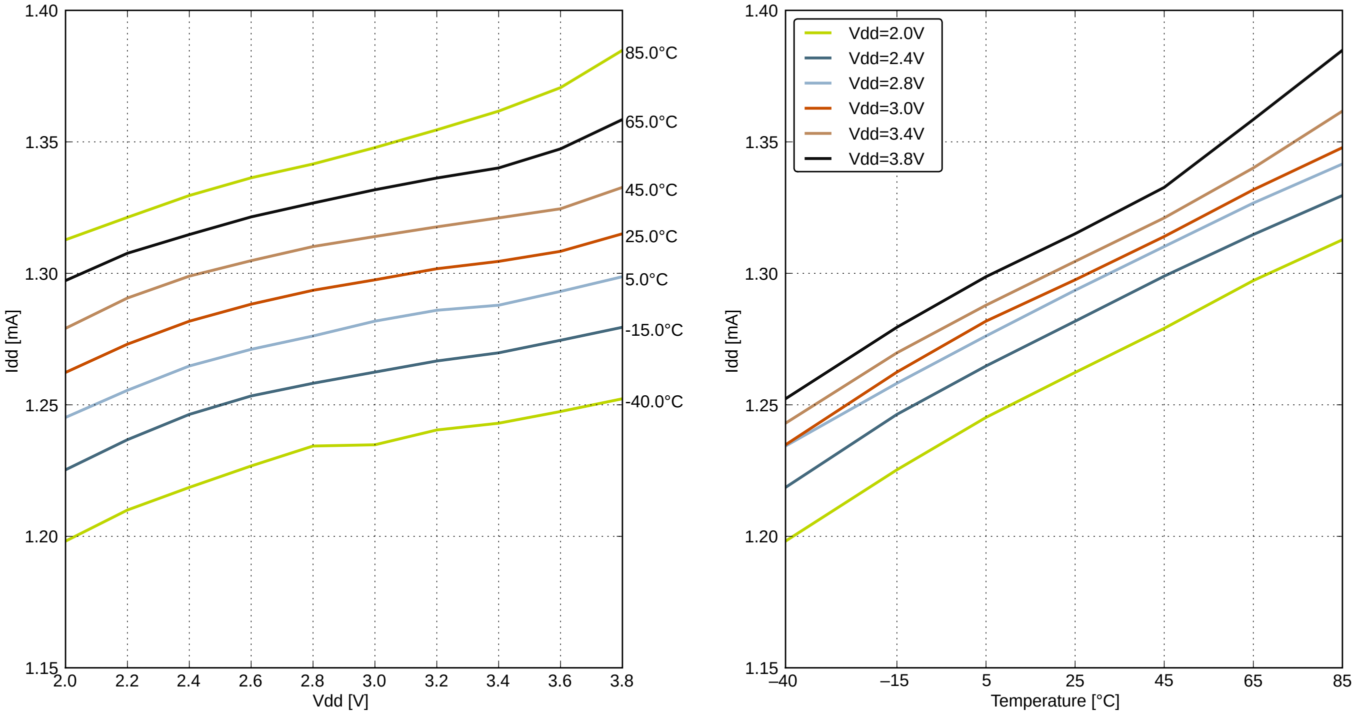


Figure 4.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28 MHz

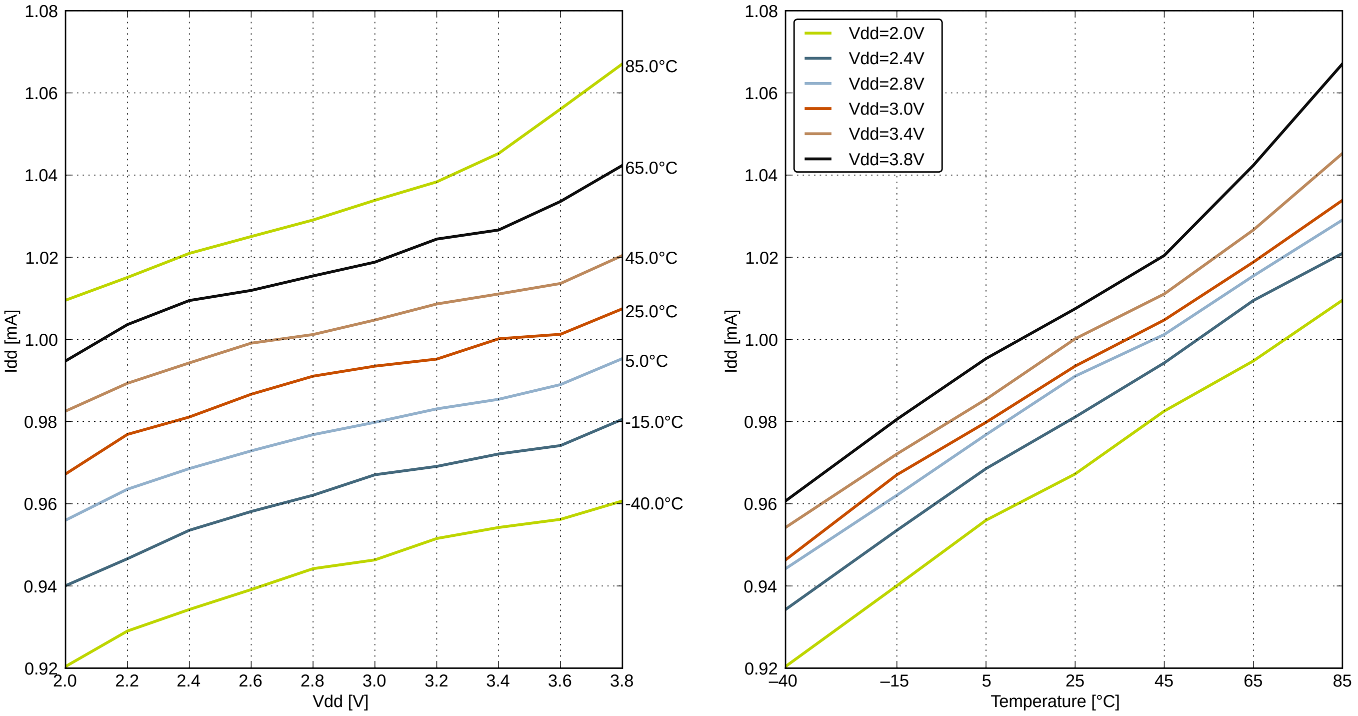


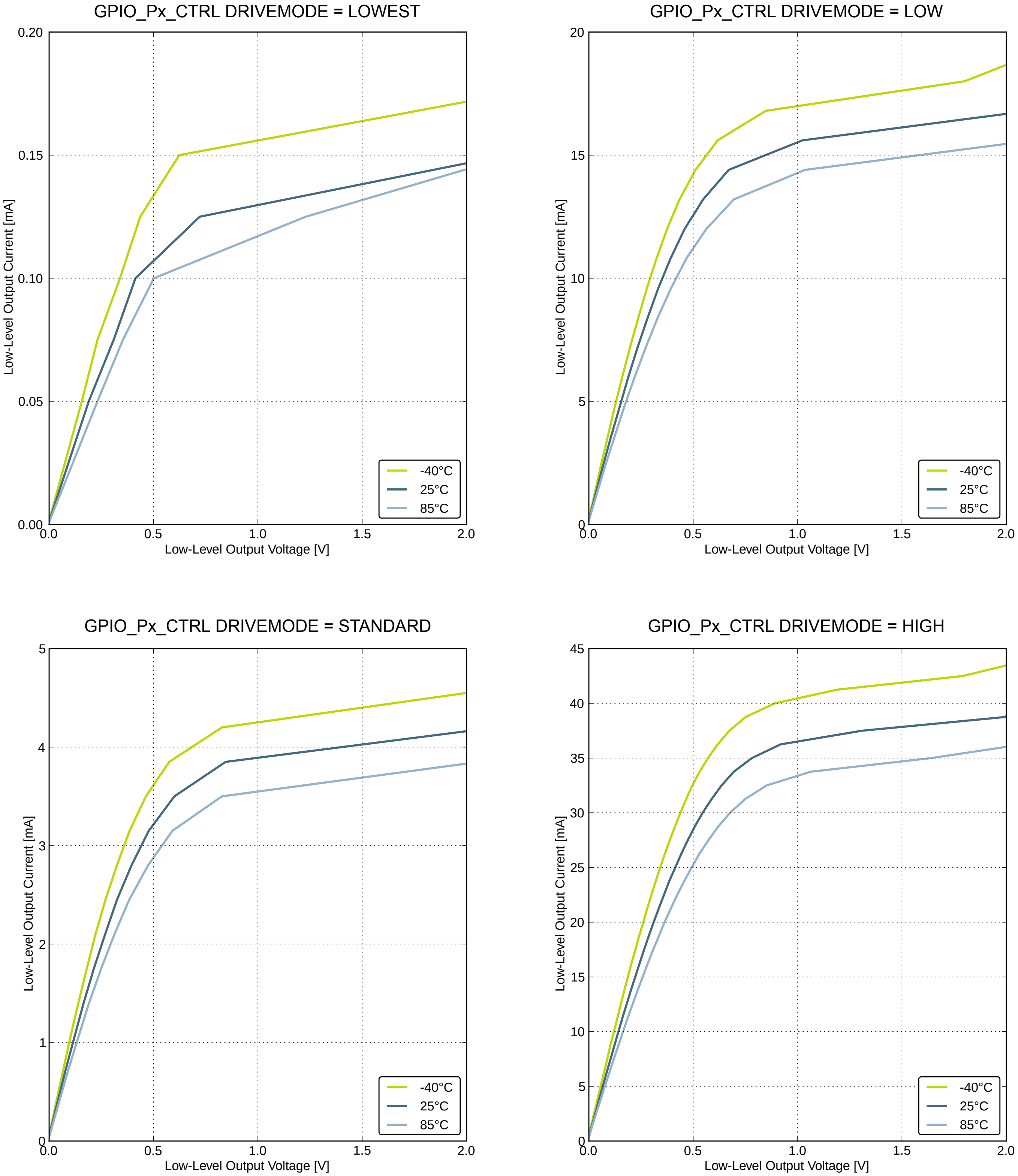
Figure 4.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz

4.6 Power Management

The EFM32G requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 4.5. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$	EM0	1.74	—	1.96	V
		EM1	1.74	—	1.96	V
		EM2	1.74	—	1.96	V
BOD threshold on rising external supply voltage	$V_{BODextthr+}$	EM0	—	1.85	—	V
Power-on Reset (POR) threshold on rising external supply voltage	$V_{PORthr+}$		—	—	1.98	V
Delay from reset is released until program execution starts	$t_{RESETdly}$	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	µs
negative pulse length to ensure complete reset of device	t_{RESET}		50	—	—	ns
Voltage regulator decoupling capacitor.	$C_{DECOUPLE}$	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	µF



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW

GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage

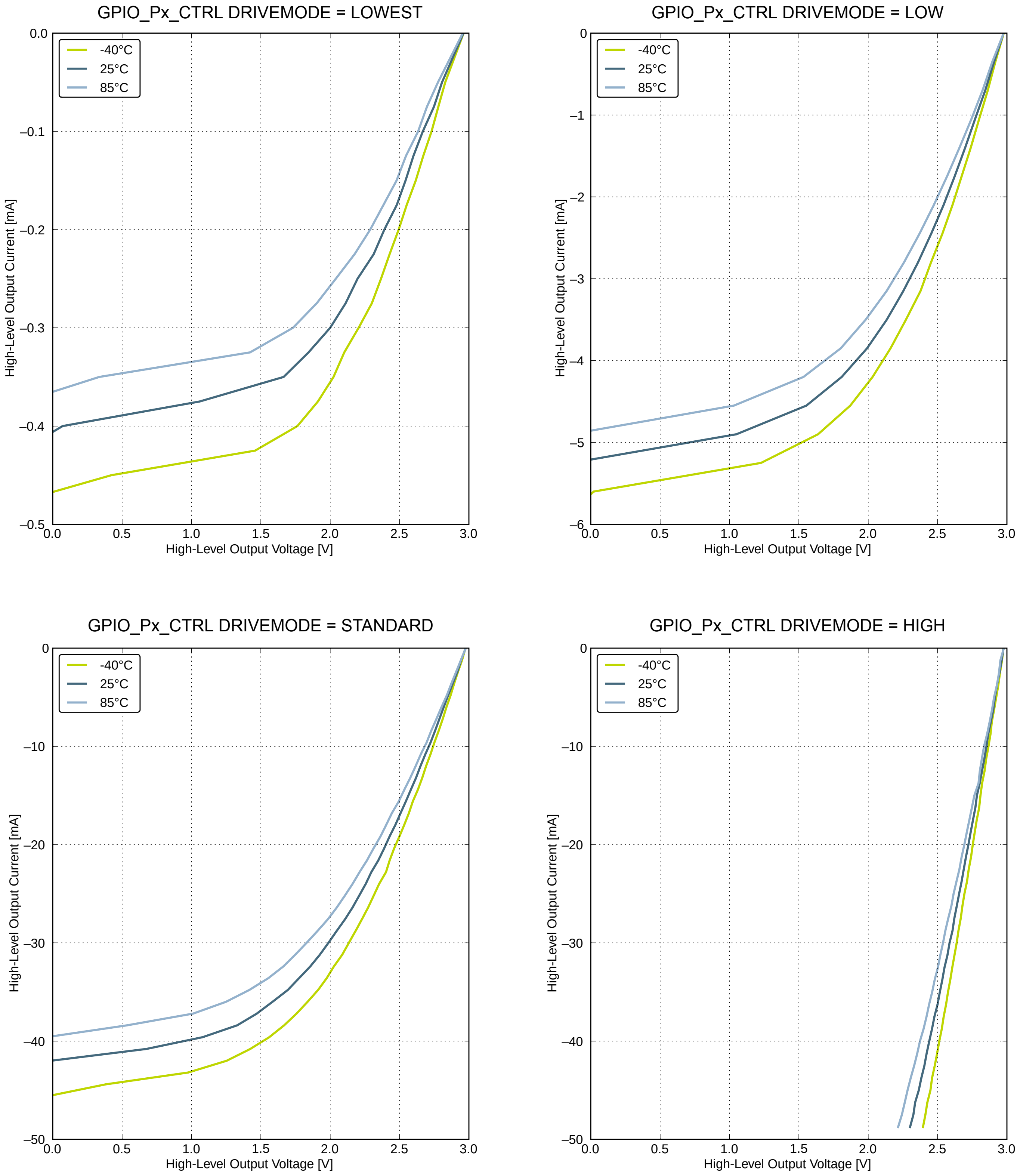


Figure 4.17. Typical High-Level Output Current, 3V Supply Voltage

4.9.3 LFRCO

Table 4.10. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	f_{LFRCO}		31.29	32.768	34.24	kHz
Startup time not including software calibration	t_{LFRCO}		—	150	—	µs
Current consumption	I_{LFRCO}		—	190	—	nA
Temperature coefficient	TC_{LFRCO}		—	±0.02	—	%/°C
Supply voltage coefficient	VC_{LFRCO}		—	±15	—	%/V
Frequency step for LSB change in TUNING value	$TUNESTEP_{LFRCO}$		—	1.5	—	%

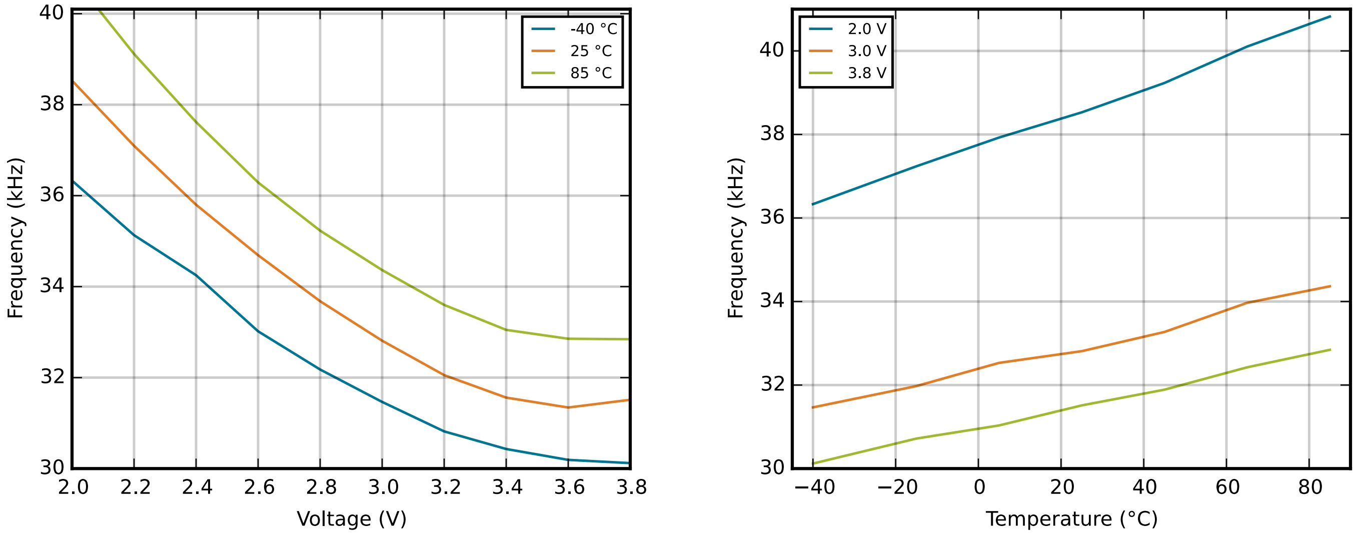


Figure 4.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

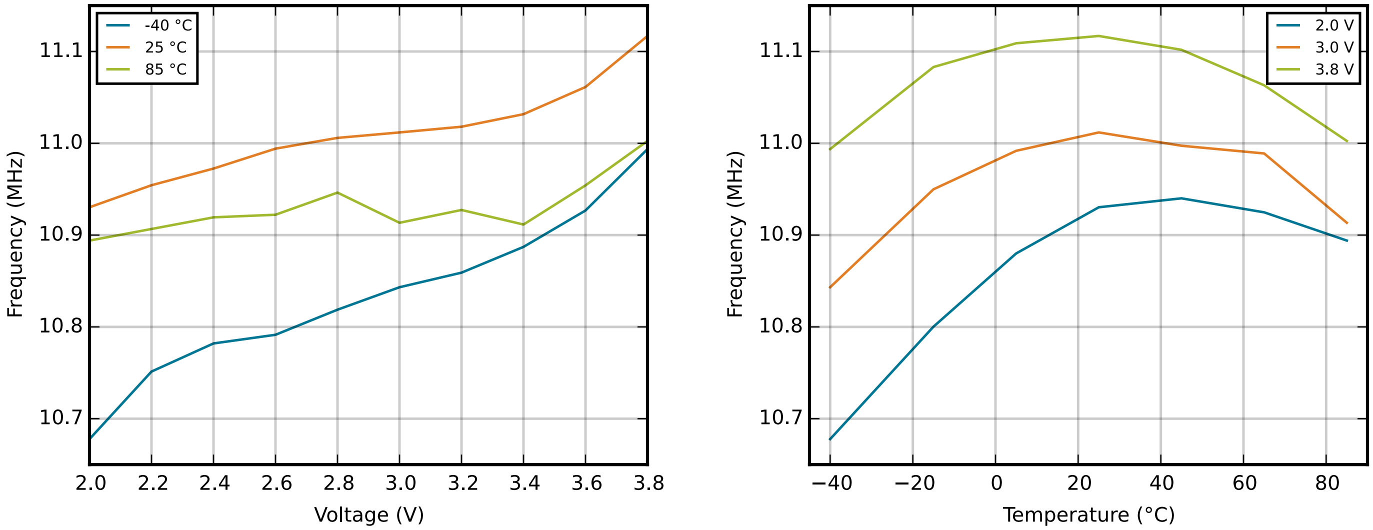


Figure 4.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

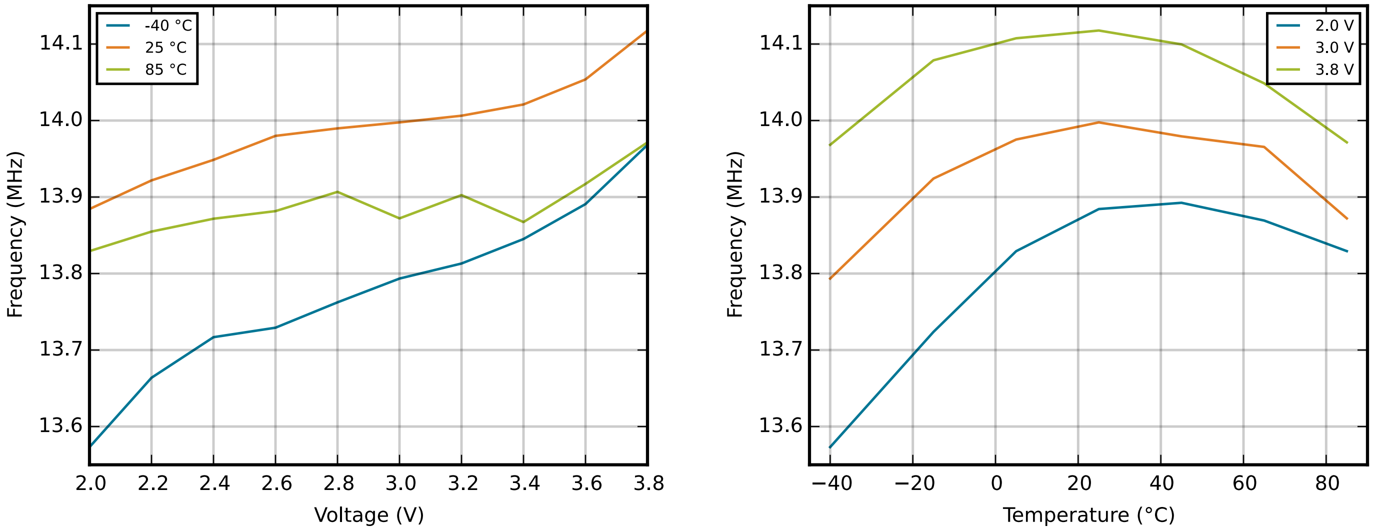


Figure 4.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

Alternate	LOCATION				
Functionality	0	1	2	3	Description
US0_TX	PE10		PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7				USART1 clock input / output.
US1_CS	PB8				USART1 chip select input / output.
US1_RX	PC1				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

5.2.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G222 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.6. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	—	—	—	—	PA10	PA9	PA8	—	—	—	—	—	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	—	—	—	—	—	—	—
Port C	PC15	PC14	PC13	—	PC11	PC10	PC9	PC8	—	—	—	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	—	—	—	—	—	PD7	PD6	PD5	PD4	—	—	—	—
Port E	—	—	PE13	PE12	PE11	PE10	—	—	—	—	—	—	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

5.4 EFM32G232 (TQFP64)

5.4.1 Pinout

The EFM32G232 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

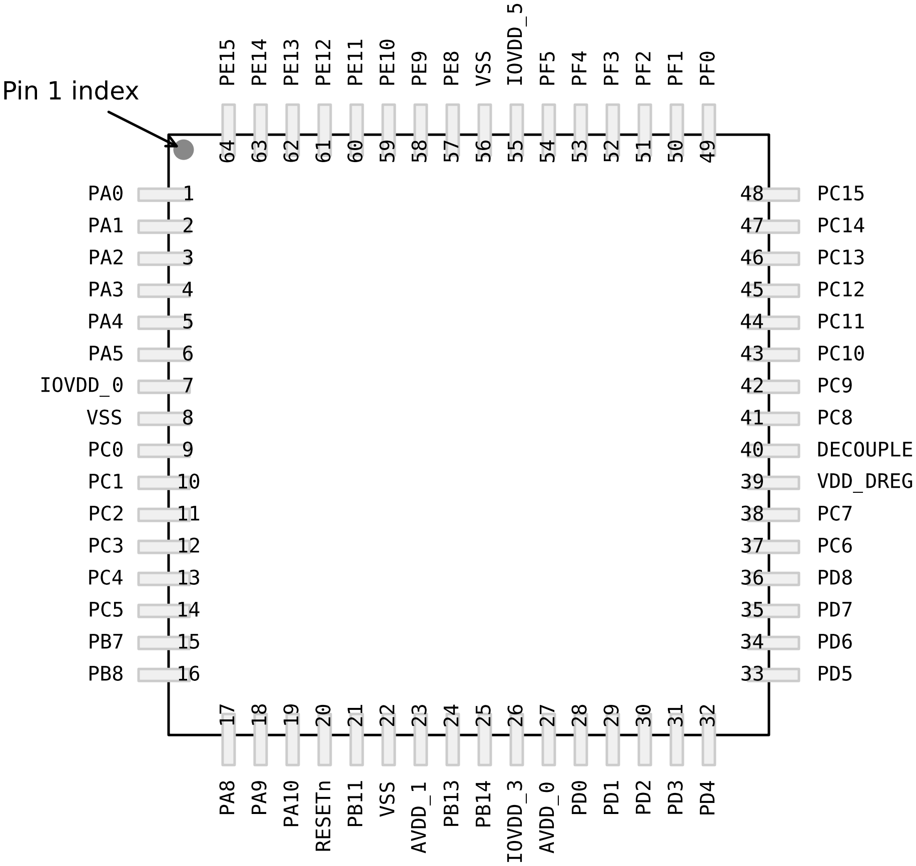


Figure 5.4. EFM32G232 Pinout (top view, not to scale)

Table 5.10. Device Pinout

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3		TIM0_CDTI0 #0		
5	PA4		TIM0_CDTI1 #0		

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Other**
6	PA5		TIM0_CDTI2 #0	LEU1_TX #1	
7	IOVDD_0	Digital IO power supply 0.			
8	VSS	Ground.			
9	PC0	ACMP0_CH0	PCNT0_S0IN #1	US1_TX #1	
10	PC1	ACMP0_CH1	PCNT0_S1IN #1	US1_RX #1	
11	PC2	ACMP0_CH2		US1_CLK #1	
12	PC3	ACMP0_CH3		US1_CS #1	
13	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
14	PC5	ACMP0_CH5	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
15	PB7	LFXTAL_P		US1_CLK #0	
16	PB8	LFXTAL_N		US1_CS #0	
17	PA8		TIM2_CC0 #0		
18	PA9		TIM2_CC1 #0		
19	PA10		TIM2_CC2 #0		
20	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
22	VSS	Ground.			
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		LEU0_TX #1	
25	PB14	HFXTAL_N		LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	
31	PD3	ADC0_CH3	TIM0_CC2 #3	US1_CS #1	
32	PD4	ADC0_CH4		LEU0_TX #0	
33	PD5	ADC0_CH5		LEU0_RX #0	
34	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
35	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
36	PD8				CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	

Alternate	LOCATION				
Functionality	0	1	2	3	Description
US0_CS	PE13		PC8		USART0 chip select input / output.
US0_RX	PE11		PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10		PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4				USART2 clock input / output.
US2_CS	PC5				USART2 chip select input / output.
US2_RX	PC3				USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2				USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G2322 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.12. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	—	—	—	—	PA10	PA9	PA8	—	—	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	—	—	—	—	—	—	—
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	—	—	—	—	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

Alternate	LOCATION				
Functionality	0	1	2	3	Description
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0		PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12			Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13			Timer 2 Capture Compare input / output channel 1.
TIM2_CC2		PA14			Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12	PE5			USART0 clock input / output.
US0_CS	PE13	PE4			USART0 chip select input / output.
US0_RX	PE11	PE6			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7			USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX		PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX		PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX		PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).

5.8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.23. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**EBI**	**Timers**	**Communication**	**Other**
4	PA3	LCD_SEG 16	EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
5	PA4	LCD_SEG 17	EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
6	PA5	LCD_SEG 18	EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
7	PA6	LCD_SEG 19	EBI_AD15 #0		LEU1_RX #1	
8	IOVDD_0	Digital IO power supply 0.				
9	PB0	LCD_SEG 32		TIM1_CC0 #2		
10	PB1	LCD_SEG 33		TIM1_CC1 #2		
11	PB2	LCD_SEG 34		TIM1_CC2 #2		
12	PB3	LCD_SEG 20		PCNT1_S0IN #1	US2_TX #1	
13	PB4	LCD_SEG 21		PCNT1_S1IN #1	US2_RX #1	
14	PB5	LCD_SEG 22			US2_CLK #1	
15	PB6	LCD_SEG 23			US2_CS #1	
16	VSS	Ground.				
17	IOVDD_1	Digital IO power supply 1.				
18	PC0	ACMP0_CH0		PCNT0_S0IN #2	US1_TX #0	
19	PC1	ACMP0_CH1		PCNT0_S1IN #2	US1_RX #0	
20	PC2	ACMP0_CH2			US2_TX #0	
21	PC3	ACMP0_CH3			US2_RX #0	
22	PC4	ACMP0_CH4		LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
23	PC5	ACMP0_CH5		LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
24	PB7	LFXTAL_P			US1_CLK #0	
25	PB8	LFXTAL_N			US1_CS #0	
26	PA7	LCD_SEG 35				
27	PA8	LCD_SEG 36		TIM2_CC0 #0		

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A4	PE9	LCD_SEG5	EBI_AD01 #0	PCNT2_S1IN #1		
A5	PD10	LCD_SEG29	EBI_CS1 #0			
A6	PF7	LCD_SEG25		TIM0_CC1 #2	U0_RX #0	
A7	PF5	LCD_SEG3	EBI_REn #0	TIM0_CDTI2 #2		
A8	PF4	LCD_SEG2	EBI_WEn #0	TIM0_CDTI1 #2		
A9	PE4	LCD_COM0			US0_CS #1	
A10	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
A11	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
B1	PA15	LCD_SEG12	EBI_AD08 #0			
B2	PE13	LCD_SEG9	EBI_AD05 #0		US0_CS #0	ACMP0_O #0
B3	PE11	LCD_SEG7	EBI_AD03 #0	TIM1_CC1 #1	US0_RX #0	BOOT_RX
B4	PE8	LCD_SEG4	EBI_AD00 #0	PCNT2_S0IN #1		
B5	PD11	LCD_SEG30	EBI_CS2 #0			
B6	PF8	LCD_SEG26		TIM0_CC2 #2		
B7	PF6	LCD_SEG24		TIM0_CC0 #2	U0_TX #0	
B8	PF3	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2		
B9	PE5	LCD_COM1			US0_CLK #1	
B10	PC12	ACMP1_CH4				CMU_CLK0 #1
B11	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
C1	PA1	LCD_SEG14	EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
C2	PA0	LCD_SEG13	EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	

7. LQFP100 Package Specifications

7.1 LQFP100 Package Dimensions

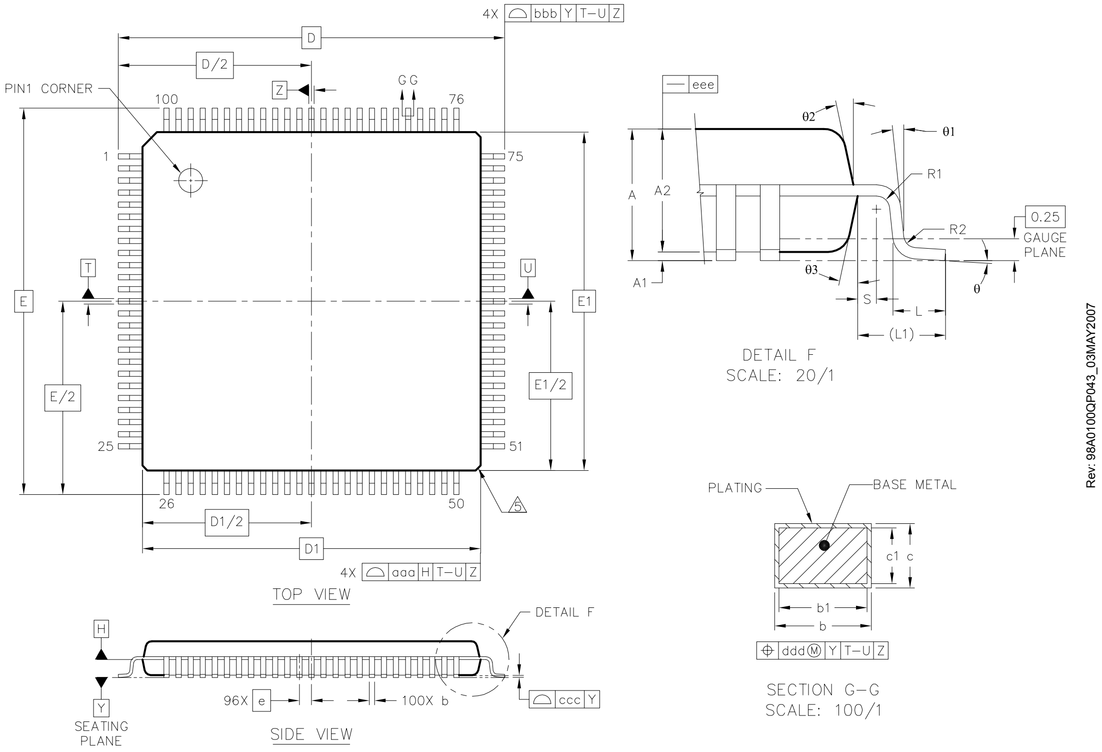


Figure 7.1. LQFP100

Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause thelead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be locatedon the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
5. Exact shape of each corner is optional.

Table 7.1. LQFP100 (Dimensions in mm)

	SYMBOL	MIN	NOM	MAX
total thickness	A	—	—	1.6
stand off	A1	0.05	—	0.15
mold thickness	A2	1.35	1.4	1.45
lead width (plating)	b	0.17	0.2	0.27
lead width	b1	0.17	—	0.23
L/F thickness (plating)	c	0.09	—	0.2
lead thickness	c1	0.09	—	0.16

13.15 Revision 0.90

This revision applies the following devices:

- EFM32G222

Initial preliminary revision, April 14th, 2011

This revision applies the following devices:

- EFM32G232
- EFM32G842

Initial preliminary revision, June 30th, 2011

13.16 Revision 0.85

February 19th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Renamed DBG_SWV pin to DBG_SWO.

13.17 Revision 0.84

February 11th, 2010

This revision applies the following devices:

- EFM32G230
- EFM32G840

Corrected pinout tables.

13.18 Revision 0.83

January 25th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Updated errata section.

Specified flash word width in Flash Electrical Characteristics.

Added Capacitive Sense Internal Resistor values in ACMP Electrical Characteristics.

13.19 Revision 0.82

December 9th, 2009

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For LQFP100 devices, incorrect pin 0 removed from pinout table.

Updated contact information.

ADC current consumption numbers updated in ADC Electrical Characteristics.

For devices with LCD, updated LCD supply voltage range in LCD Electrical Characteristics.

13.20 Revision 0.81

November 20th, 2009

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For devices without a differential DAC, System Summary updated.

Electrical Characteristics updated.

Storage temperature in Electrical Characteristics updated.

Temperature coefficient of band-gap reference in Electrical Characteristics added.

Erase times in Flash Electrical Characteristics updated.

Definitions of DNL and INL added in ADC section.

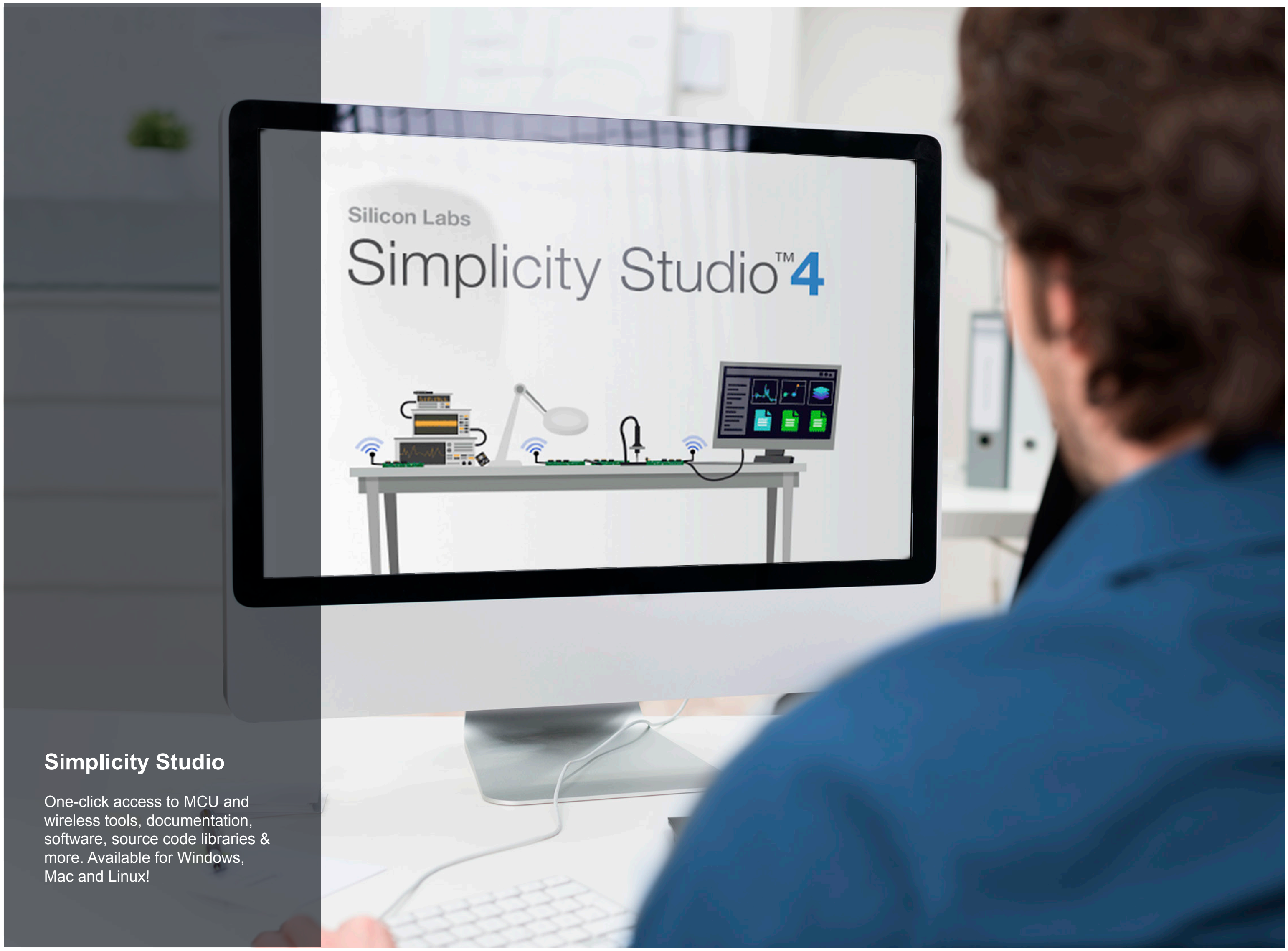
For devices with and LCD, LCD Electrical Characteristics added.

Current consumption of digital peripherals added in Electrical Characteristics.

For LQFP100 devices, package information in Pinout and Package corrected.

For BGA112 devices, pinout information in Pinout table corrected.

Updated errata section.



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