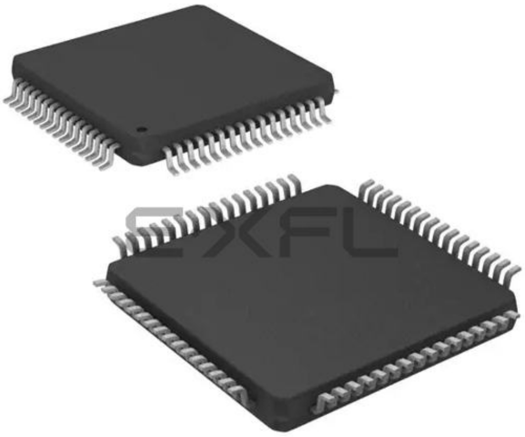

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g232f64-qfp64

3.3 Memory Map

The EFM32G memory map is shown in the figure below. RAM and Flash sizes are for the largest memory configuration.

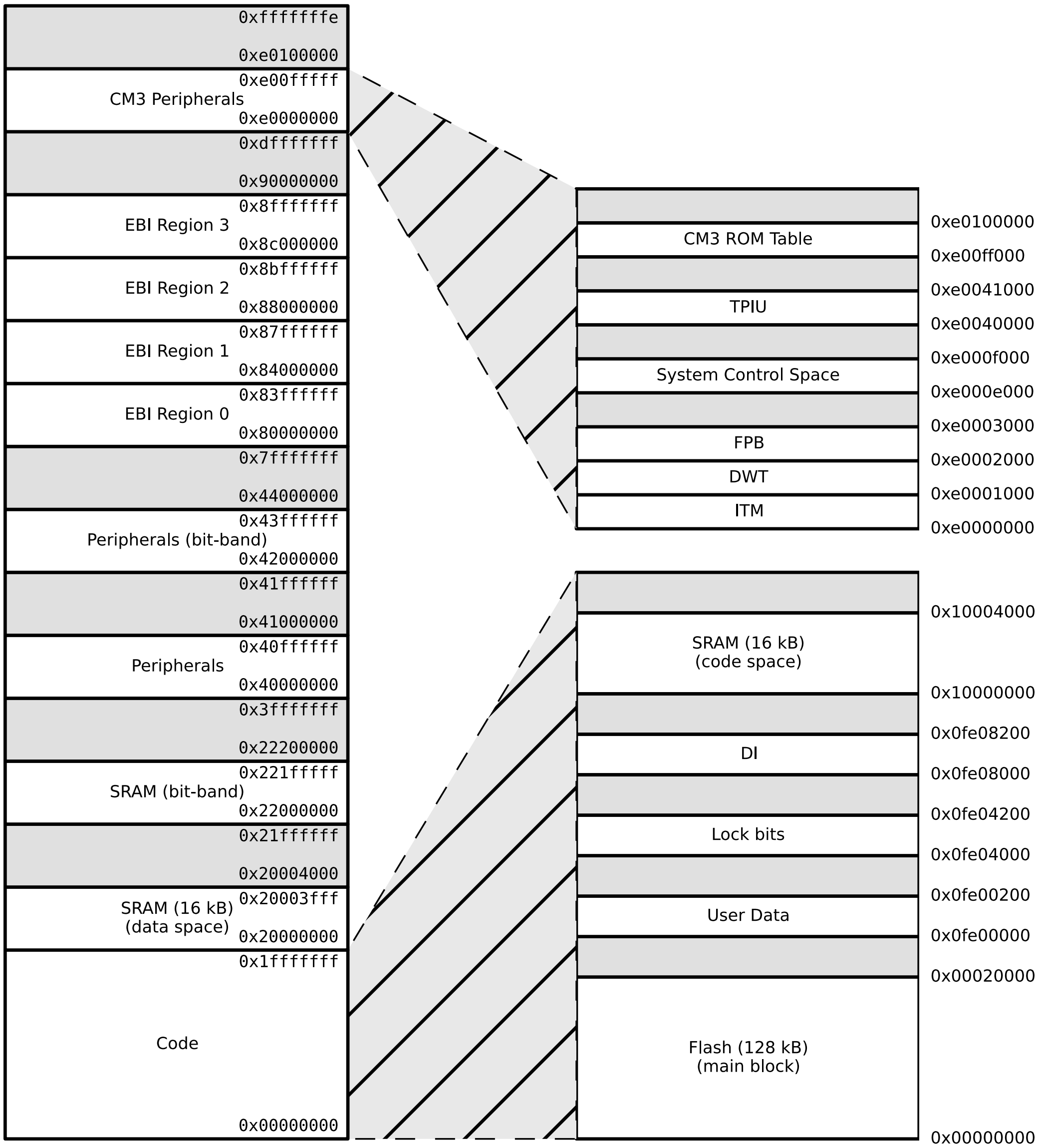

Figure 3.2. System Address Space with Core and Code Space Listing

4.7 Flash

Table 4.6. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 ºC	10000	—	—	h
		T_{AMB}<85 ºC	10	—	—	years
		T_{AMB}<70 ºC	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time[2]	t_{P_ERASE}		20.7	22.0	24.8	ms
Device erase time[3]	t_{D_ERASE}		41.8	45.0	49.2	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

Note:

1. Measured at 25 °C.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.

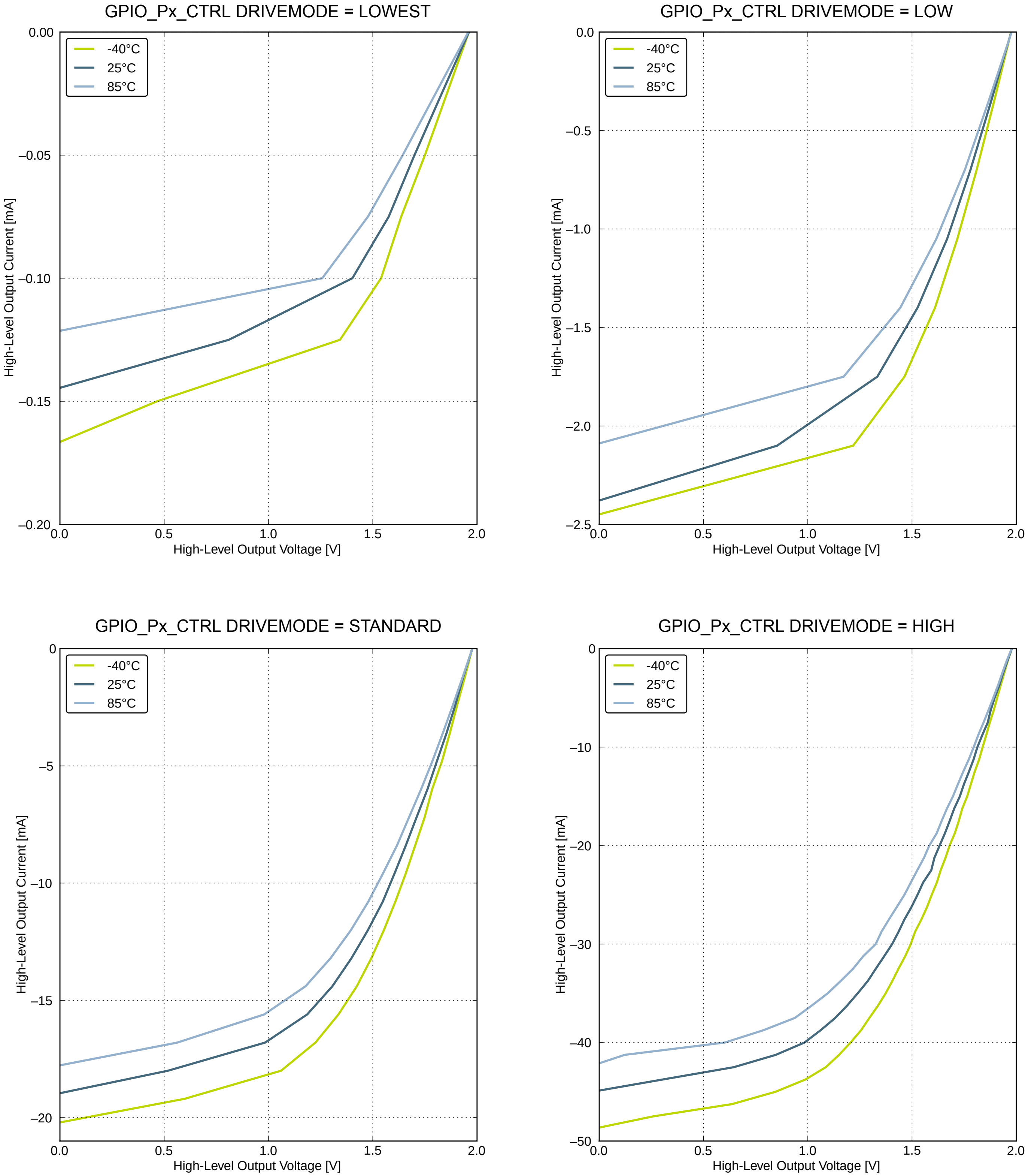

Figure 4.15. Typical High-Level Output Current, 2V Supply Voltage

4.9.2 HFXO

Table 4.9. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal Frequency	f_{HFXO}		4	—	32	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 32 MHz	—	30	60	Ω
		Crystal frequency 4 MHz	—	400	1500	Ω
The transconductance of the HFXO input transistor at crystal startup	g_{mHFXO}	HFXOBOOST in CMU_CTRL equals 0b11	20	—	—	mS
Supported crystal external load range	C_{HFXOL}		5	—	25	pF
Current consumption for HFXO after startup	I_{HFXO}	4 MHz: ESR=400 Ω, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	85	—	µA
		32 MHz: ESR=30 Ω, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	165	—	µA
Startup time	t_{HFXO}	32 MHz: ESR=30 Ω, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	400	—	µs
Pulse width removed by glitch detector			1	—	4	ns

4.9.3 LFRCO

Table 4.10. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	f_{LFRCO}		31.29	32.768	34.24	kHz
Startup time not including software calibration	t_{LFRCO}		—	150	—	µs
Current consumption	I_{LFRCO}		—	190	—	nA
Temperature coefficient	TC_{LFRCO}		—	±0.02	—	%/°C
Supply voltage coefficient	VC_{LFRCO}		—	±15	—	%/V
Frequency step for LSB change in TUNING value	$TUNESTEP_{LFRCO}$		—	1.5	—	%

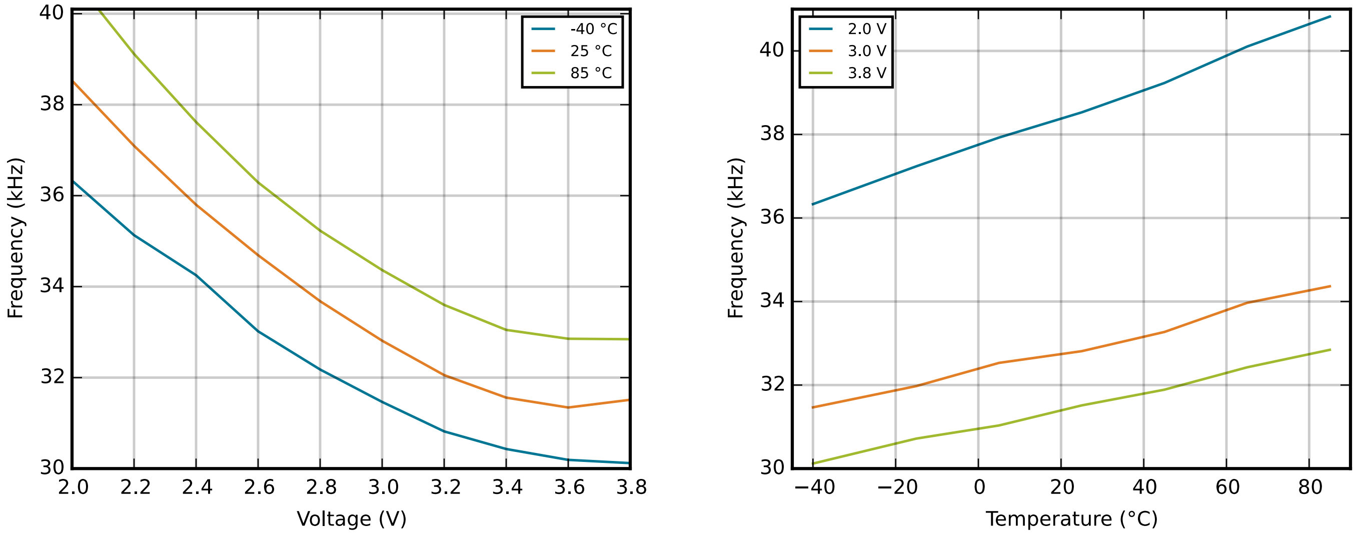

Figure 4.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LETIM0_OUT1	PD7		PF1		Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14			LEUART0 Receive input.
LEU0_TX	PD4	PB13			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		Pulse Counter PCNT0 input number 1.
TIM0_CC0	PA0	PA0			Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0		PC13		PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14		PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15		PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12				USART0 clock input / output.
US0_CS	PE13				USART0 chip select input / output.
US0_RX	PE11				USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10				USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7				USART1 clock input / output.
US1_CS	PB8				USART1 chip select input / output.
US1_RX	PC1				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PA5		TIM0_CDTI2 #0	LEU1_TX #1	
6	PA6			LEU1_RX #1	
8	IOVDD_0	Digital IO power supply 0.			
9	PC0		PCNT0_S0IN #1	US1_TX #0	
10	PC1		PCNT0_S1IN #1	US1_RX #0	
11	PC2			US2_CLK #0	
12	PC3			US2_CS #0	
13	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
14	PC5	ACMP0_CH5	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
15	PB7	LFXTAL_P		US1_CLK #0	
16	PB8	LFXTAL_N		US1_CS #0	
17	PA8		TIM2_CC0 #0		
18	PA9		TIM2_CC1 #0		
19	PA10		TIM2_CC2 #0		
20	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
22	PB12	DAC0_OUT1	LETIM0_OUT1 #1		
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		LEU0_TX #1	
25	PB14	HFXTAL_N		LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	
31	PD3	ADC0_CH3	TIM0_CC2 #3	US1_CS #1	
32	PD4	ADC0_CH4		LEU0_TX #0	
33	PD5	ADC0_CH5		LEU0_RX #0	
34	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
35	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
36	PD8				CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	
39	VDD_DREG	Power supply for on-chip voltage regulator.			

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Other**
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
44	PC11	ACMP1_CH3		US0_TX #2	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2				ACMP1_O #0 DBG_SWO #0
52	PF3		TIM0_CDTI0 #2		
53	PF4		TIM0_CDTI1 #2		
54	PF5		TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground.			
57	PE8		PCNT2_S0IN #1		
58	PE9		PCNT2_S1IN #1		
59	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
60	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX
61	PE12		TIM1_CC2 #1	US0_CLK #0	
62	PE13			US0_CS #0	ACMP0_O #0
63	PE14			LEU0_TX #2	
64	PE15			LEU0_RX #2	

5.5.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.14. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2			Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3			Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0	PF6	PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG9	PE13				LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14				LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15				LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG13	PA0				LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1				LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2				LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3				LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4				LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5				LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20	PB3				LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG21	PB4				LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG22	PB5				LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG23	PB6				LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7				LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**EBI**	**Timers**	**Communication**	**Other**
53	PD7	ADC0_CH7		LETIM0_OUT1 #0	I2C0_SCL #1	
54	PD8					CMU_CLK1 #1
55	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
56	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
57	VDD_DREG	Power supply for on-chip voltage regulator.				
58	VSS	Ground.				
59	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
60	PE0			PCNT0_S0IN #1	U0_TX #1	
61	PE1			PCNT0_S1IN #1	U0_RX #1	
62	PE2					ACMP0_O #1
63	PE3					ACMP1_O #1
64	PE4	LCD_COM0			US0_CS #1	
65	PE5	LCD_COM1			US0_CLK #1	
66	PE6	LCD_COM2			US0_RX #1	
67	PE7	LCD_COM3			US0_TX #1	
68	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
69	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
70	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
71	PC11	ACMP1_CH3			US0_TX #2	
72	PC12	ACMP1_CH4				CMU_CLK0 #1
73	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
74	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
75	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
76	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**EBI**	**Timers**	**Communication**	**Other**
E9	PE0			PCNT0_S0IN #1	U0_TX #1	
E10	PE1			PCNT0_S1IN #1	U0_RX #1	
E11	PE3					ACMP1_O #1
F1	PB1	LCD_SEG 33		TIM1_CC1 #2		
F2	PB2	LCD_SEG 34		TIM1_CC2 #2		
F3	PB3	LCD_SEG 20		PCNT1_S0IN #1	US2_TX #1	
F4	PB4	LCD_SEG 21		PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2					ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
G1	PB5	LCD_SEG 22			US2_CLK #1	
G2	PB6	LCD_SEG 23			US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				
G10	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
G11	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
H1	PC0	ACMP0_CH0		PCNT0_S0IN #2	US1_TX #0	
H2	PC2	ACMP0_CH2			US2_TX #0	
H3	PD14				I2C0_SDA #3	
H4	PA7	LCD_SEG 35				
H5	PA8	LCD_SEG 36		TIM2_CC0 #0		
H6	VSS	Ground.				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8					CMU_CLK1 #1

Alternate	LOCATION				
Functionality	0	1	2	3	Description
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	I2C0 Serial Data input / output.
LCD_BCAP_N	PA13				LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12				LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14				LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4				LCD driver common line number 0.
LCD_COM1	PE5				LCD driver common line number 1.
LCD_COM2	PE6				LCD driver common line number 2.
LCD_COM3	PE7				LCD driver common line number 3.
LCD_SEG0	PF2				LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3				LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4				LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5				LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8				LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9				LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10				LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.

7.2 LQFP100 PCB Layout

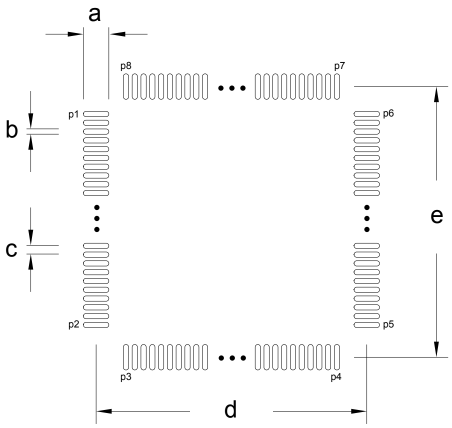

Figure 7.2. LQFP100 PCB Land Pattern

Table 7.2. LQFP100 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	1.45	P1	1	P6	75
b	0.30	P2	25	P7	76
c	0.50	P3	26	P8	100
d	15.40	P4	50		
e	15.40	P5	51		

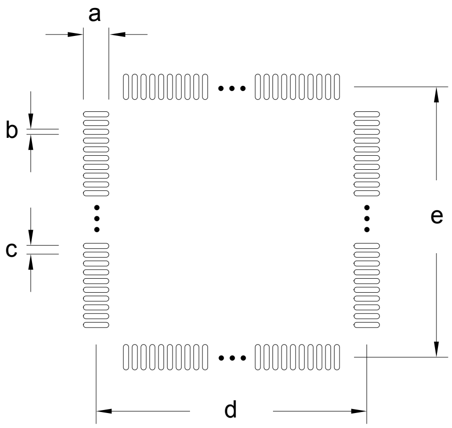

Figure 7.3. LQFP100 PCB Solder Mask

Table 7.3. LQFP100 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.57
b	0.42
c	0.50
d	15.40
e	15.40

9.2 TQFP48 PCB Layout

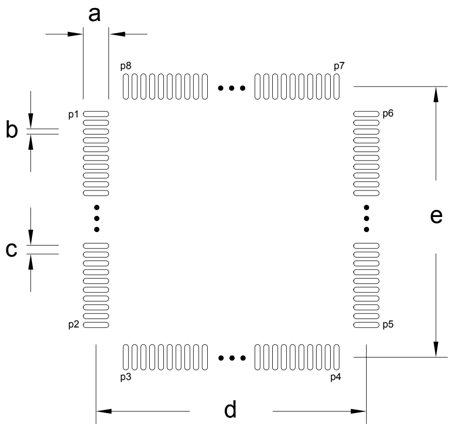

Figure 9.2. TQFP48 PCB Land Pattern

Table 9.2. TQFP48 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	1.60	P1	1	P6	36
b	0.30	P2	12	P7	37
c	0.50	P3	13	P8	48
d	8.50	P4	24		
e	8.50	P5	25		

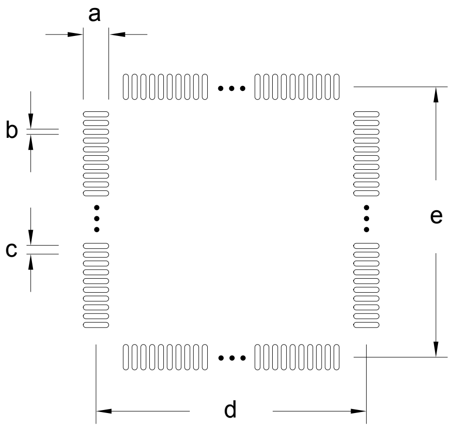

Figure 9.3. TQFP48 PCB Solder Mask

Table 9.3. TQFP48 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	8.50
e	8.50

10.3 QFN64 Package Marking

In the illustration below package fields and position are shown.

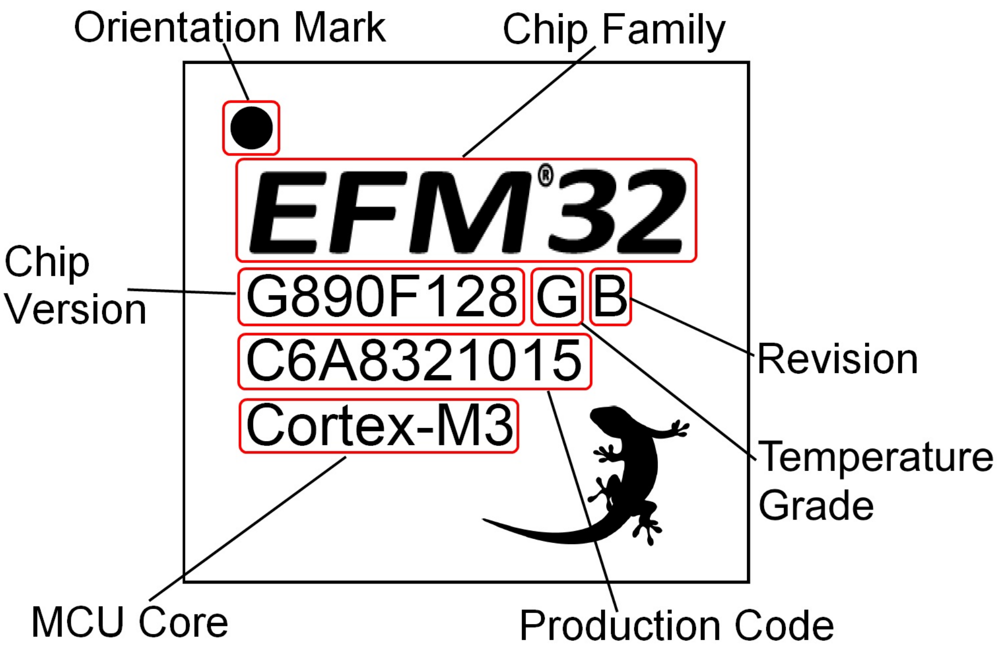

Figure 10.5. Example Chip Marking (Top View)

11. QFN32 Package Specifications

11.1 QFN32 Package Dimensions

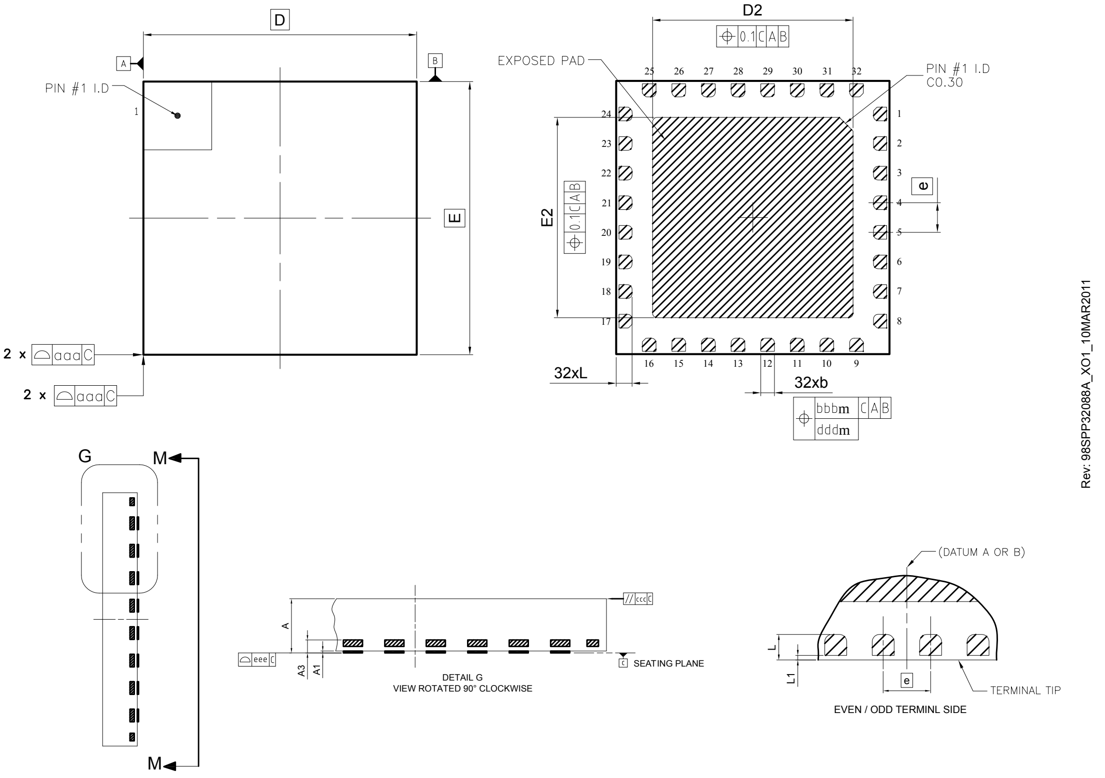

Figure 11.1. QFN32

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm fromthe terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm isacceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 11.1. QFN32 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00	0.203 REF	0.25	6.00 BSC	6.00 BSC	4.30	4.30	0.65 BSC	0.30	0.00	0.10	0.10	0.10	0.05	0.08
Nom	0.85	—		0.30			4.40	4.40		0.35						
Max	0.90	0.05		0.35			4.50	4.50		0.40	0.10					

The QFN32 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

13.9 Revision 1.40

February 27th, 2012

Updated Power Management section.

Corrected operating voltage from 1.8 V to 1.85 V.

Corrected $\mathrm{TGRAD}_{\mathrm{ADCTH}}$ parameter.

Corrected package drawing.

Updated PCB land pattern, solder mask and stencil design.

For LQFP48 devices, corrected available Pulse Counters from 3 to 2.

For LQFP48 devices, corrected available LEUARTs from 2 to 1.

For LQFP64 devices, corrected ordering codes in the ordering information table.

13.10 Revision 1.30

May 20th, 2011

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Updated LFXO load capacitance section.