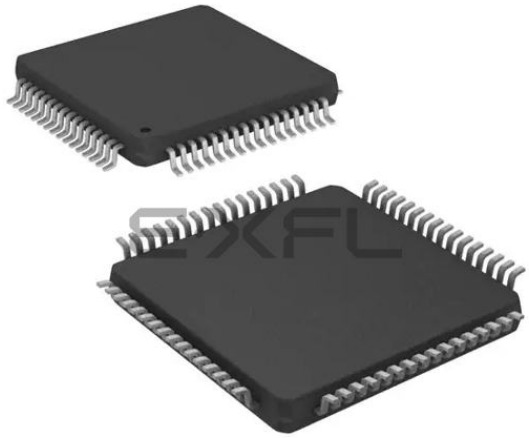

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g232f64-qfp64t

3.2.4 EFM32G230

The features of the EFM32G230 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.4. EFM32G230 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 57)

3.2.8 EFM32G840

The features of the EFM32G840 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.8. EFM32G840 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:4], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:4], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 57)
LCD	Full configuration	LCD_SEG[23:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

4.4 Current Consumption

Table 4.3. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	180	—	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	181	206	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	183	207	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	185	211	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	186	215	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	191	218	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	220	—	µA/MHz
EM1 current (Production test condition = 14 MHz)	I_{EM1}	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	45	—	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	47	62	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	48	64	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	50	69	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	51	72	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V	—	56	83	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V	—	103	—	µA/MHz
EM2 current	I_{EM2}	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25 ºC	—	0.9	1.5	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85 ºC	—	3.0	6.0	µA
EM3 current	I_{EM3}	V_{DD}= 3.0 V, T_{AMB}=25 ºC	—	0.59	1.0	µA
		V_{DD}= 3.0 V, T_{AMB}=85 ºC	—	2.75	5.8	µA
EM4 current	I_{EM4}	V_{DD}= 3.0 V, T_{AMB}=25 ºC	—	0.02	0.045	µA
		V_{DD}= 3.0 V, T_{AMB}=85 ºC	—	0.25	0.7	µA

4.8 General Purpose Input Output

Table 4.7. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	$0.30 \times V_{DD}$[1]	V
Input high voltage	V_{IOIH}		$0.70 \times V_{DD}$[1]	—	—	V
Output high voltage (Production test condition = 3.0 V, DRIVEMODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.80 \times V_{DD}$	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.90 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.85 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.90 \times V_{DD}$	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75 \times V_{DD}$	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80 \times V_{DD}$	—	—	V

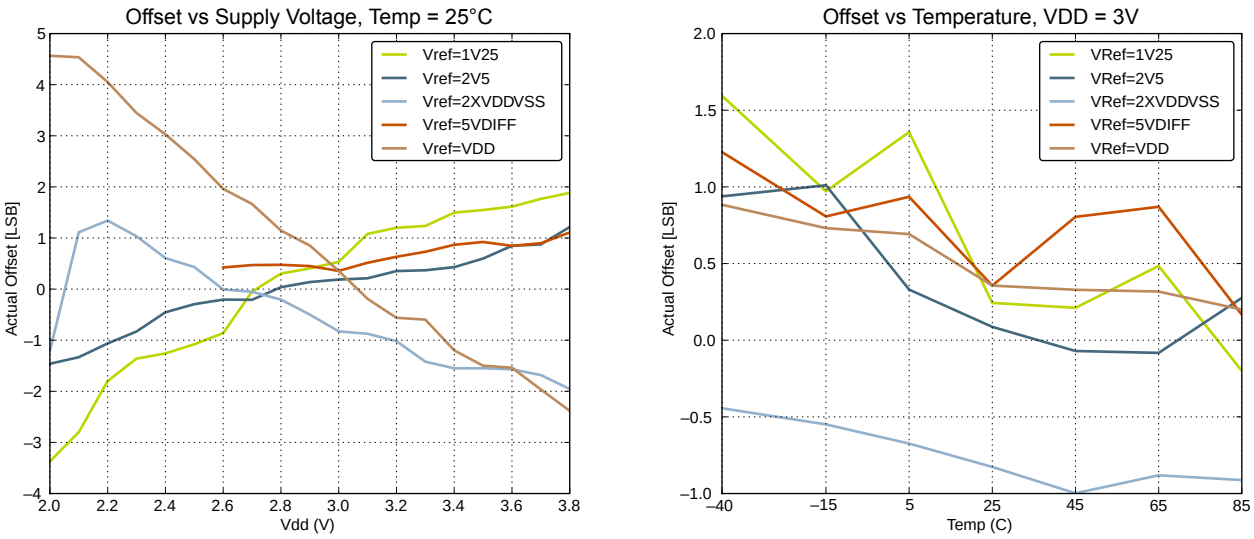

Figure 4.32. ADC Absolute Offset, Common Mode = VDD/2

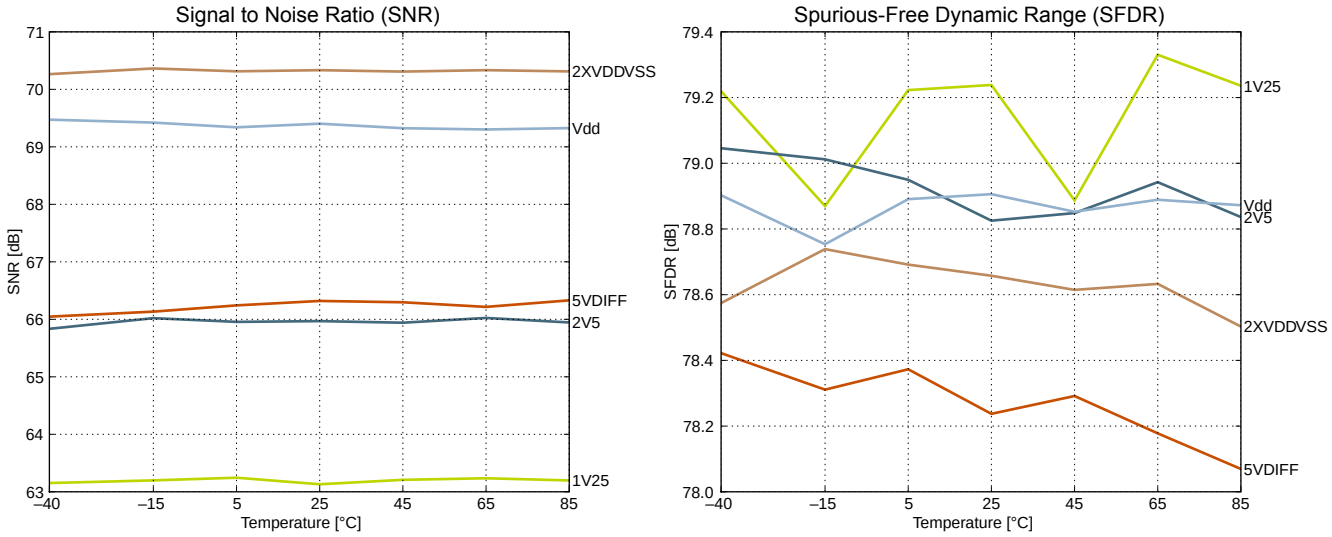

Figure 4.33. ADC Dynamic Performance vs Temperature for all ADC References, VDD = 3V

5.3 EFM32G230 (QFN64)

5.3.1 Pinout

The EFM32G230 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

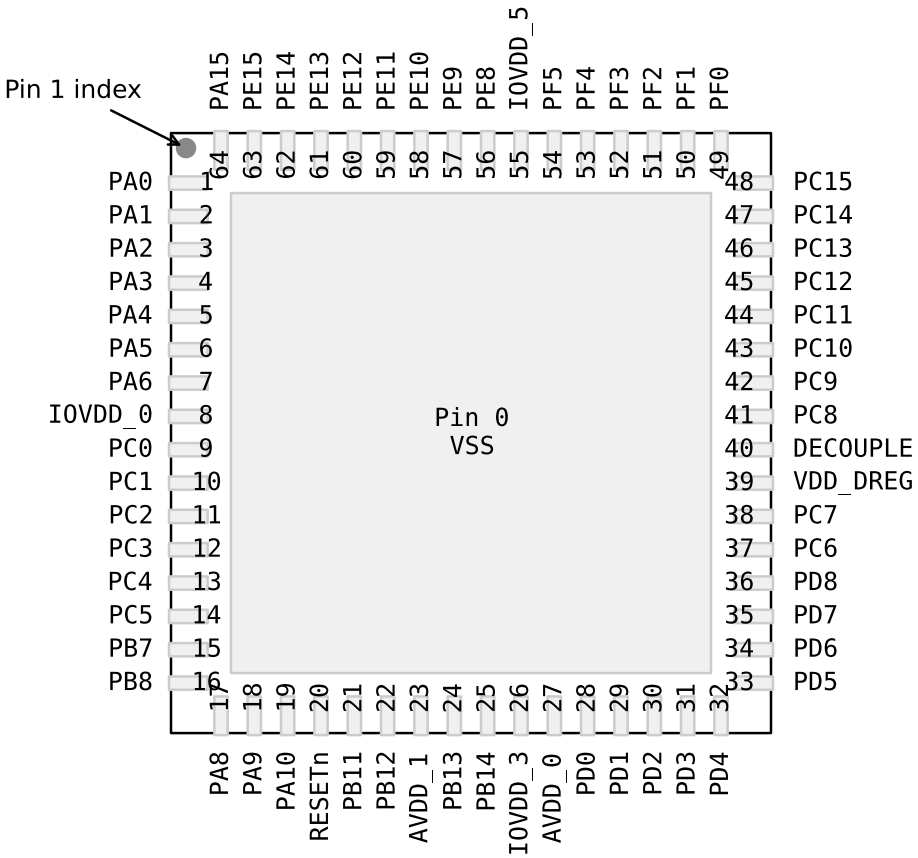

Figure 5.3. EFM32G230 Pinout (top view, not to scale)

Table 5.7. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3		TIM0_CDTI0 #0		
5	PA4		TIM0_CDTI1 #0		

5.4 EFM32G232 (TQFP64)

5.4.1 Pinout

The EFM32G232 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

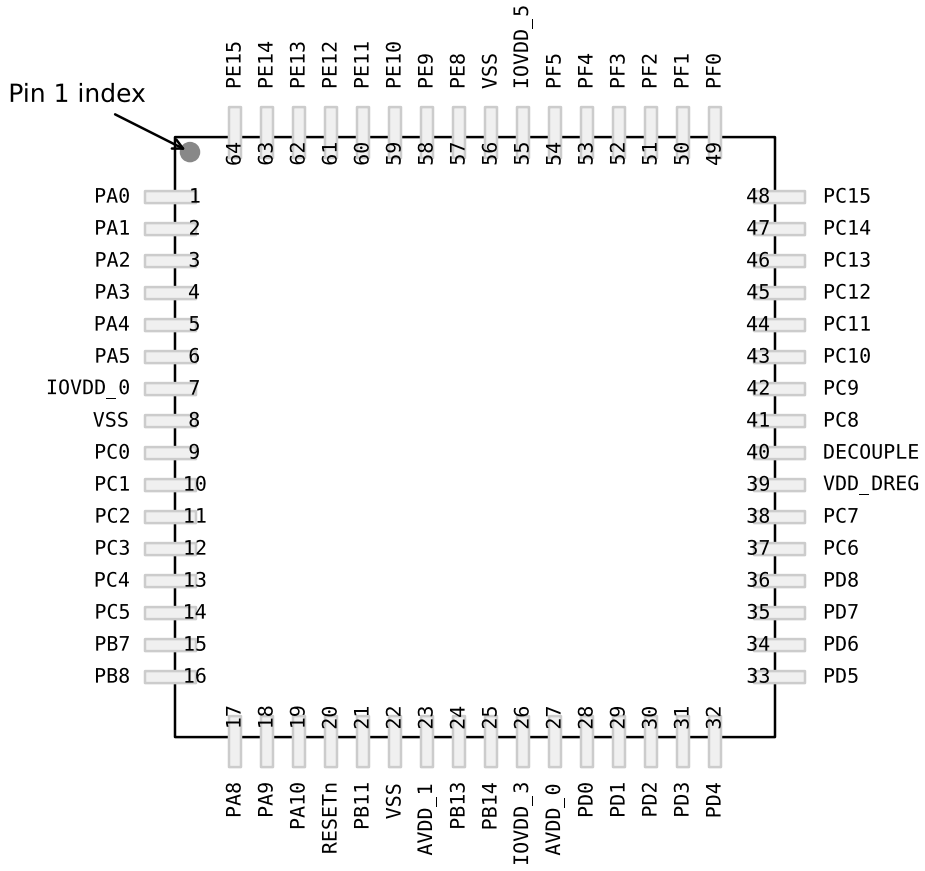

Figure 5.4. EFM32G232 Pinout (top view, not to scale)

Table 5.10. Device Pinout

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3		TIM0_CDTI0 #0		
5	PA4		TIM0_CDTI1 #0		

5.5 EFM32G280 (LQFP100)

5.5.1 Pinout

The EFM32G280 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

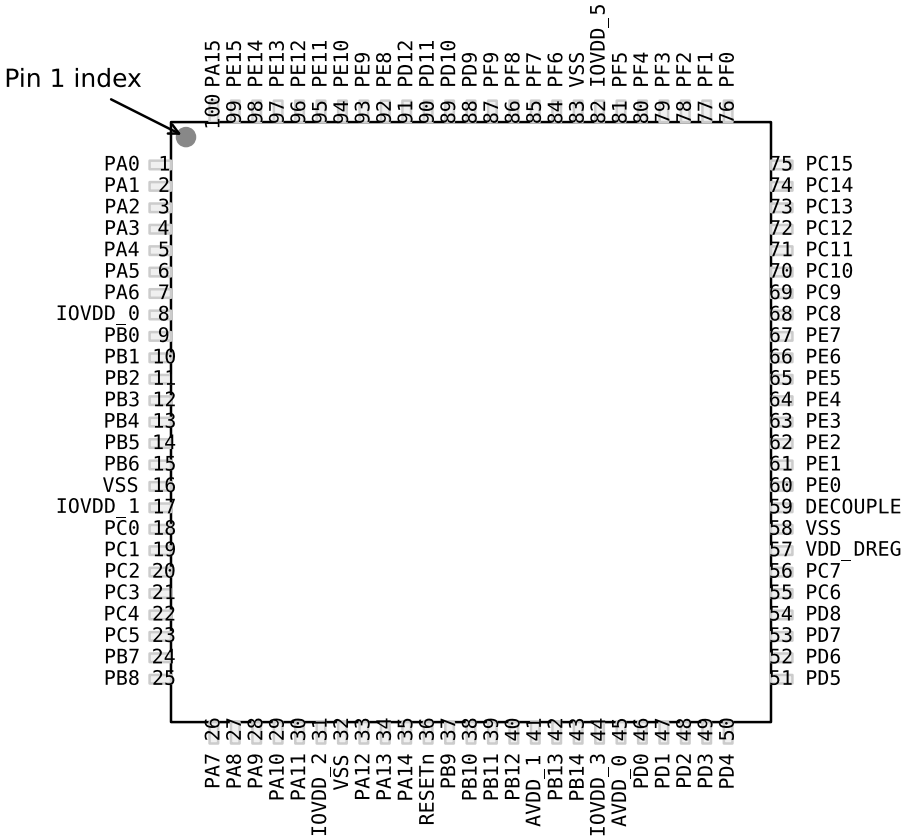

Figure 5.5. EFM32G280 Pinout (top view, not to scale)

Table 5.13. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0		EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3		EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
5	PA4		EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	

5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G280 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.15. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	—	—	—	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

Alternate	LOCATION				
Functionality	0	1	2	3	Description
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0	PF6	PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A4	PE9	LCD_SEG 5	EBI_AD01 #0	PCNT2_S1IN #1		
A5	PD10	LCD_SEG 29	EBI_CS1 #0			
A6	PF7	LCD_SEG 25		TIM0_CC1 #2	U0_RX #0	
A7	PF5	LCD_SEG 3	EBI_REn #0	TIM0_CDTI2 #2		
A8	PF4	LCD_SEG 2	EBI_WEn #0	TIM0_CDTI1 #2		
A9	PE4	LCD_COM 0			US0_CS #1	
A10	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
A11	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
B1	PA15	LCD_SEG 12	EBI_AD08 #0			
B2	PE13	LCD_SEG 9	EBI_AD05 #0		US0_CS #0	ACMP0_O #0
B3	PE11	LCD_SEG 7	EBI_AD03 #0	TIM1_CC1 #1	US0_RX #0	BOOT_RX
B4	PE8	LCD_SEG 4	EBI_AD00 #0	PCNT2_S0IN #1		
B5	PD11	LCD_SEG 30	EBI_CS2 #0			
B6	PF8	LCD_SEG 26		TIM0_CC2 #2		
B7	PF6	LCD_SEG 24		TIM0_CC0 #2	U0_TX #0	
B8	PF3	LCD_SEG 1	EBI_ALE #0	TIM0_CDTI0 #2		
B9	PE5	LCD_COM 1			US0_CLK #1	
B10	PC12	ACMP1_CH4				CMU_CLK0 #1
B11	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
C1	PA1	LCD_SEG 14	EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
C2	PA0	LCD_SEG 13	EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
E9	PE0			PCNT0_S0IN #1	U0_TX #1	
E10	PE1			PCNT0_S1IN #1	U0_RX #1	
E11	PE3					ACMP1_O #1
F1	PB1	LCD_SEG 33		TIM1_CC1 #2		
F2	PB2	LCD_SEG 34		TIM1_CC2 #2		
F3	PB3	LCD_SEG 20		PCNT1_S0IN #1	US2_TX #1	
F4	PB4	LCD_SEG 21		PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2					ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
G1	PB5	LCD_SEG 22			US2_CLK #1	
G2	PB6	LCD_SEG 23			US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				
G10	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
G11	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
H1	PC0	ACMP0_CH0		PCNT0_S0IN #2	US1_TX #0	
H2	PC2	ACMP0_CH2			US2_TX #0	
H3	PD14				I2C0_SDA #3	
H4	PA7	LCD_SEG 35				
H5	PA8	LCD_SEG 36		TIM2_CC0 #0		
H6	VSS	Ground.				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8					CMU_CLK1 #1

7. LQFP100 Package Specifications

7.1 LQFP100 Package Dimensions

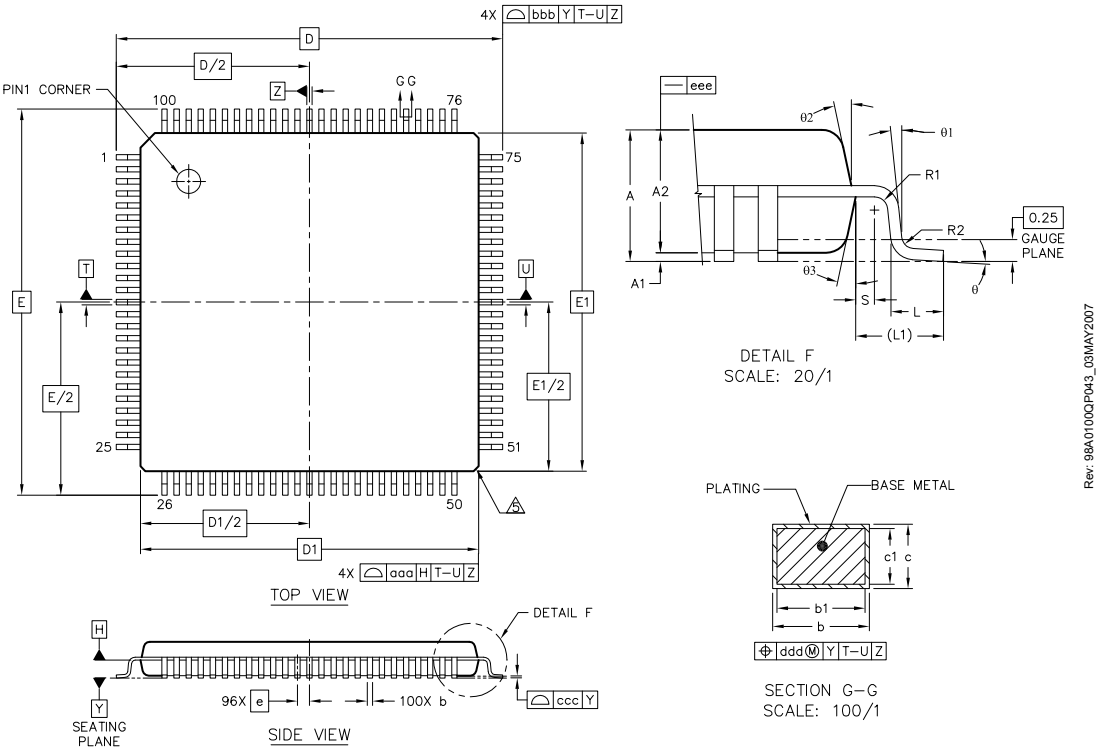

Figure 7.1. LQFP100

Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause thelead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be locatedon the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
5. Exact shape of each corner is optional.

Table 7.1. LQFP100 (Dimensions in mm)

	SYMBOL	MIN	NOM	MAX
total thickness	A	—	—	1.6
stand off	A1	0.05	—	0.15
mold thickness	A2	1.35	1.4	1.45
lead width (plating)	b	0.17	0.2	0.27
lead width	b1	0.17	—	0.23
L/F thickness (plating)	c	0.09	—	0.2
lead thickness	c1	0.09	—	0.16

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
D	0.170	—	0.270	S1	—	4.500 BSC	—
E	0.950	—	1.050	V	—	9.000 BSC	—
F	0.170	—	0.230	V1	—	4.5000 BSC	—
G	—	0.500 BSC	—	W	—	0.200 BSC	—
H	0.050	—	0.150	AA	—	1.000BSC	—
J	0.090	—	0.200				
K	0.500	—	0.700				
L	0DEG	—	7DEG				

The TQFP48 Package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

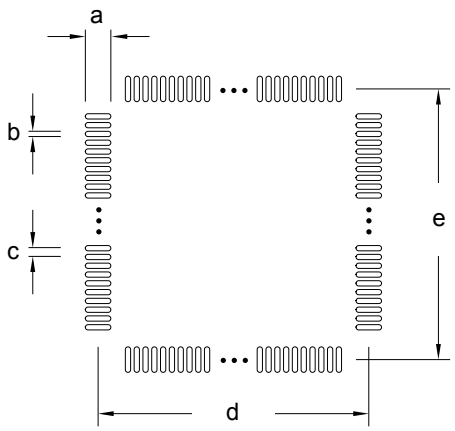

Figure 9.4. TQFP48 PCB Stencil Design

Table 9.4. TQFP48 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.50
b	0.20
c	0.50
d	8.50
e	8.50

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see 5. Pin Definitions.

10.2 QFN64 PCB Layout

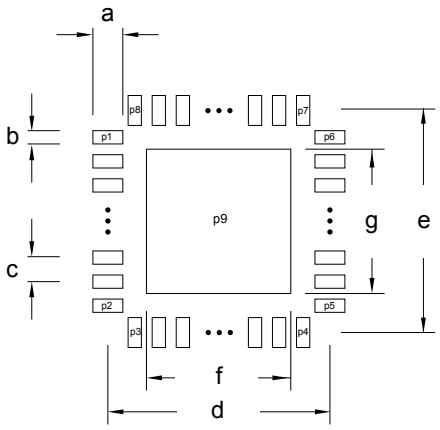

Figure 10.2. QFN64 PCB Land Pattern

Table 10.2. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.85	P1	1	P8	64
b	0.30	P2	16	P9	65
c	0.50	P3	17		
d	8.90	P4	32		
e	8.90	P5	33		
f	7.20	P6	48		
g	7.20	P7	49		

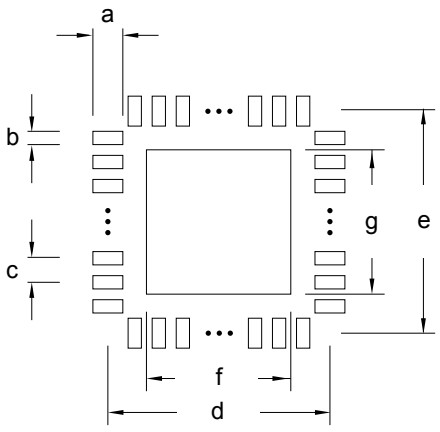

Figure 10.3. QFN64 PCB Solder Mask

Table 10.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.97	e	8.90
b	0.42	f	7.32
c	0.50	g	7.32

Symbol	Dim. (mm)	Symbol	Dim. (mm)
d	8.90	-	-

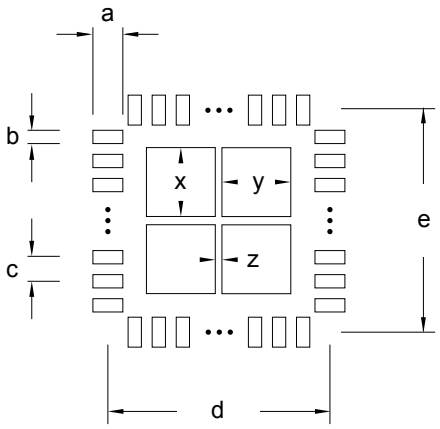

Figure 10.4. QFN64 PCB Stencil Design

Table 10.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.75	e	8.90
b	0.22	x	2.70
c	0.50	y	2.70
d	8.90	z	0.80

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

12. Chip Revision, Solder Information, Errata

12.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

12.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

12.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

13.5 Revision 1.71

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

For devices with a DAC, re-added missing DAC-data.

13.6 Revision 1.70

September 30th, 2013

For devices with an I2C, added I2C characterization data.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

For devices with an ADC, corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

For QFN64 devices, updated the Max V_{ESDCDM} value to 750 V.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

13.7 Revision 1.60

June 28th, 2013

For BGA devices, updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

13.8 Revision 1.50

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

For BGA devices, corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

Other minor corrections.

13.11 Revision 1.20

December 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Increased max storage temperature.

Added data for <150°C and <70°C on Flash data retention.

Changed latch-up sensitivity test description.

Added IO leakage current.

For LQFP100 devices, updated ESD CDM value.

Added Flash current consumption.

Updated HFRCO data.

Updated LFRCO data.

Added graph for ADC Absolute Offset over temperature.

Added graph for ADC Temperature sensor readout.

13.12 Revision 1.11

November 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Corrected maximum DAC clock speed for continuous mode.

Added DAC sample-hold mode voltage drift rate.

Added pulse widths detected by the HFXO glitch detector.

Added power sequencing information to Power Management section.