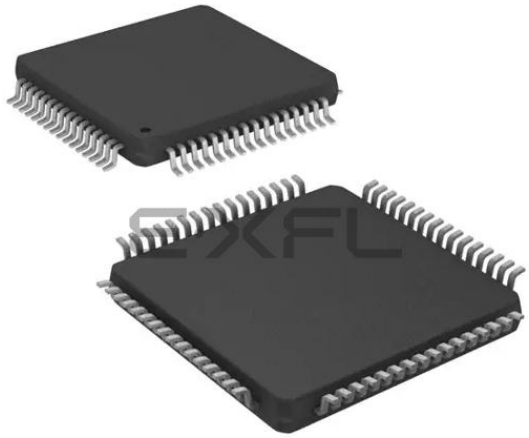

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g232f64g-e-qfp64

3.2.11 EFM32G890

The features of the EFM32G890 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.11. EFM32G890 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 57)

4.7 Flash

Table 4.6. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 ºC	10000	—	—	h
		T_{AMB}<85 ºC	10	—	—	years
		T_{AMB}<70 ºC	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time[2]	t_{P_ERASE}		20.7	22.0	24.8	ms
Device erase time[3]	t_{D_ERASE}		41.8	45.0	49.2	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

Note:

1. Measured at 25 °C.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.

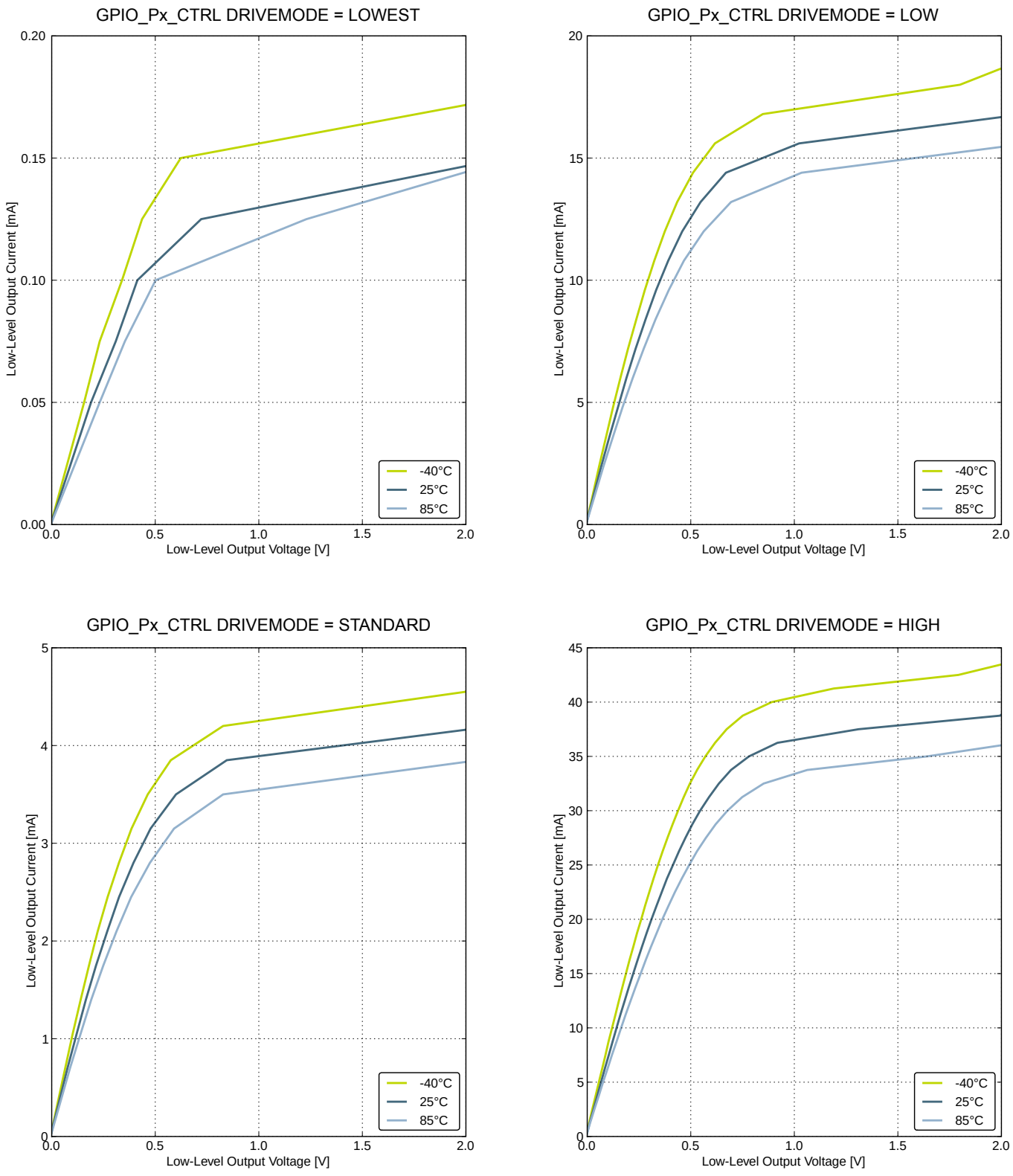

Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	200 kSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	68	79	—	dBc
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference,ADC_CLK = 7 MHz, BIASPROG = 0x747	—	79	—	dBc
Offset voltage	$V_{ADCOFFSET}$	After calibration, single-ended	—	0.3	—	mV
		After calibration, differential	-4	0.3	4	mV
Thermometer output gradient	$TGRAD_{ADCTH}$		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes/°C
Differential non-linearity (DNL)	DNL_{ADC}	V_{DD}= 3.0 V, external 2.5 V reference	-1	±0.7	4	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	V_{DD}= 3.0 V, external 2.5 V reference	—	±1.2	±3	LSB
Missing codes	MC_{ADC}		—	—	3	LSB
Gain error drift	$GAIN_{ED}$	1.25 V reference	—	0.01[2]	0.033[3]	%/°C
		2.5 V reference	—	0.01[2]	0.03[3]	%/°C
Offset error drift	$OFFSET_{ED}$	1.25 V reference	—	0.00[2]	0.06[3]	LSB/°C
		2.5 V reference	—	0.00[2]	0.04[3]	LSB/°C
VREF voltage	V_{REF}	1.25 V reference	1.2	1.25	1.3	V
		2.5 V reference	2.4	2.5	2.6	V
VREF voltage drift	V_{REF_VDRIFT}	1.25 V reference	-12.4	2.9	18.2	mV/V
		2.5 V reference, VDD > 2.5 V	-24.6	5.7	35.2	mV/V
VREF temperature drift	V_{REF_TDRIFT}	1.25 V reference	-132	272	677	µV/°C
		2.5 V reference	-231	545	1271	µV/°C
VREF current consumption	I_{VREF}	1.25 V reference	—	67	114	µA
		2.5 V reference	—	55	82	µA
ADC and DAC VREF matching	V_{REF_MATCH}	1.25 V reference	—	99.85	—	%
		2.5 V reference	—	100.01	—	%

Note:

1. Includes required contribution from the voltage reference.
2. Typical numbers given by abs(Mean) / (85 - 25).
3. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in the following figures.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise plus Distortion Ratio (SNDR)	$SNDR_{DAC}$	500 kSamples/s, 12 bit, single-ended, internal 1.25 V reference	—	57	—	dB
		500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference	—	54	—	dB
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	56	—	dB
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	53	—	dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	55	—	dB
Spurious-Free Dynamic Range (SFDR)	$SFDR_{DAC}$	500 kSamples/s, 12 bit, single-ended, internal 1.25V reference	—	62	—	dBc
		500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference	—	56	—	dBc
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	61	—	dBc
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	55	—	dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	60	—	dBc
Offset voltage	$V_{DACOFFSET}$	After calibration, single-ended	—	2	—	mV
		After calibration, differential	—	2	—	mV
Sample-hold mode voltage drift	$V_{DACSHMDRIFT}$		—	540	—	µV/ms
Differential non-linearity	DNL_{DAC}		—	±1	—	LSB
Integral non-linearity	INL_{DAC}		—	±5	—	LSB
No missing codes	MC_{DAC}		—	12	—	bits
Load current	I_{LOAD_DC}		—	—	11	mA
VREF voltage	V_{REF}	1.25 V reference	1.2	1.25	1.3	V
		2.5 V reference	2.4	2.5	2.6	V
VREF voltage drift	V_{REF_VDRIFT}	1.25 V reference	-12.4	2.9	18.2	mV/V
		2.5 V reference, VDD > 2.5 V	-24.6	5.7	35.2	mV/V
VREF temperature drift	V_{REF_TDRIFT}	1.25 V reference	-132	272	677	µV/°C
		2.5 V reference	-231	545	1271	µV/°C
VREF current consumption	I_{VREF}	1.25 V reference	—	67	114	µA
		2.5 V reference	—	55	82	µA
ADC and DAC VREF matching	V_{REF_MATCH}	1.25 V reference	—	99.85	—	%
		2.5 V reference	—	100.01	—	%

Note:

1. Measured with a static input code and no loading on the output. Includes required contribution from the voltage reference.

5. Pin Definitions

Note: Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32G.

5.1 EFM32G200 & EFM32G210 (QFN32)

5.1.1 Pinout

The EFM32G200 and EFM32G210 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

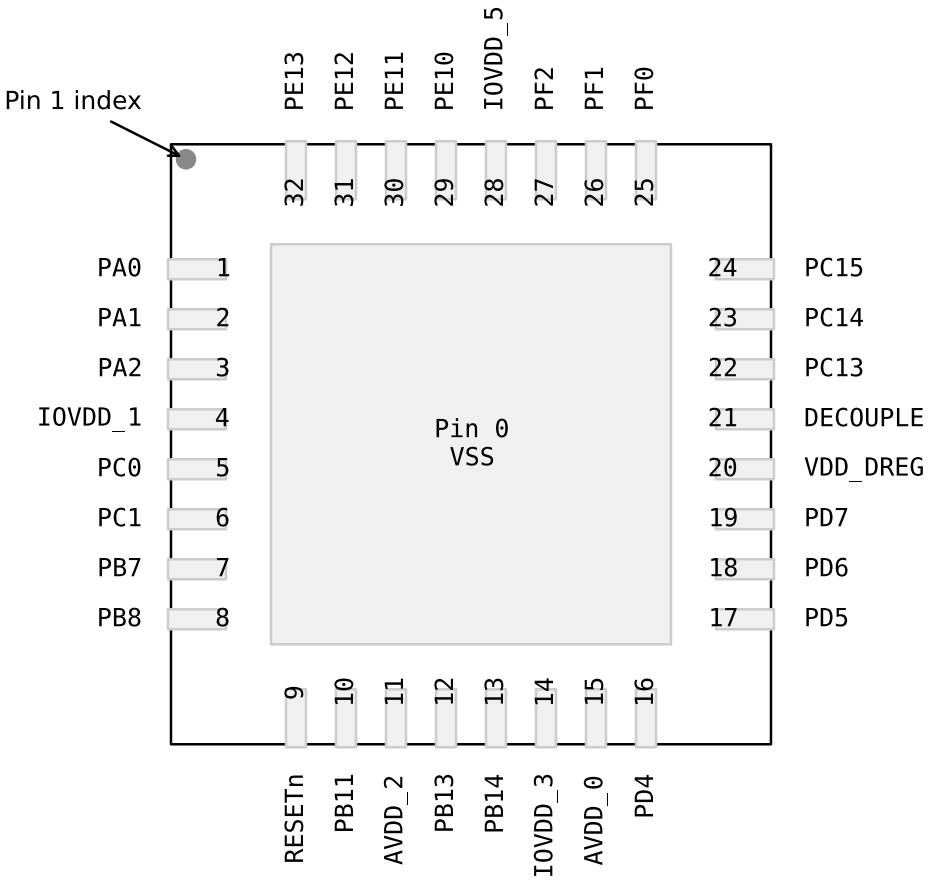

Figure 5.1. EFM32G200 & EFM32G210 Pinout (top view, not to scale)

Table 5.1. Device Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_1	Digital IO power supply 1.			
5	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
6	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
7	PB7	LFXTAL_P		US1_CLK #0	
8	PB8	LFXTAL_N		US1_CS #0	
9	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
10	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
11	AVDD_2	Analog power supply 2.			
12	PB13	HFXTAL_P		LEU0_TX #1	
13	PB14	HFXTAL_N		LEU0_RX #1	
14	IOVDD_3	Digital IO power supply 3.			
15	AVDD_0	Analog power supply 0.			
16	PD4	ADC0_CH4		LEU0_TX #0	
17	PD5	ADC0_CH5		LEU0_RX #0	
18	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
19	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
20	VDD_DREG	Power supply for on-chip voltage regulator.			
21	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
22	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
23	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
24	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
25	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
26	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
27	PF2				ACMP1_O #0 DBG_SWO #0
28	IOVDD_5	Digital IO power supply 5.			
29	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
30	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LETIM0_OUT1	PD7		PF1		Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14			LEUART0 Receive input.
LEU0_TX	PD4	PB13			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		Pulse Counter PCNT0 input number 1.
TIM0_CC0	PA0	PA0			Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0		PC13		PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14		PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15		PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12				USART0 clock input / output.
US0_CS	PE13				USART0 chip select input / output.
US0_RX	PE11				USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10				USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7				USART1 clock input / output.
US1_CS	PB8				USART1 chip select input / output.
US1_RX	PC1				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.5. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1				Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.17. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2			Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3			Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A4	PE9	LCD_SEG 5	EBI_AD01 #0	PCNT2_S1IN #1		
A5	PD10	LCD_SEG 29	EBI_CS1 #0			
A6	PF7	LCD_SEG 25		TIM0_CC1 #2	U0_RX #0	
A7	PF5	LCD_SEG 3	EBI_REn #0	TIM0_CDTI2 #2		
A8	PF4	LCD_SEG 2	EBI_WEn #0	TIM0_CDTI1 #2		
A9	PE4	LCD_COM 0			US0_CS #1	
A10	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
A11	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
B1	PA15	LCD_SEG 12	EBI_AD08 #0			
B2	PE13	LCD_SEG 9	EBI_AD05 #0		US0_CS #0	ACMP0_O #0
B3	PE11	LCD_SEG 7	EBI_AD03 #0	TIM1_CC1 #1	US0_RX #0	BOOT_RX
B4	PE8	LCD_SEG 4	EBI_AD00 #0	PCNT2_S0IN #1		
B5	PD11	LCD_SEG 30	EBI_CS2 #0			
B6	PF8	LCD_SEG 26		TIM0_CC2 #2		
B7	PF6	LCD_SEG 24		TIM0_CC0 #2	U0_TX #0	
B8	PF3	LCD_SEG 1	EBI_ALE #0	TIM0_CDTI0 #2		
B9	PE5	LCD_COM 1			US0_CLK #1	
B10	PC12	ACMP1_CH4				CMU_CLK0 #1
B11	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
C1	PA1	LCD_SEG 14	EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
C2	PA0	LCD_SEG 13	EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
C3	PE10	LCD_SEG 6	EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					
C5	PD12	LCD_SEG 31	EBI_CS3 #0			
C6	PF9	LCD_SEG 27				
C7	VSS	Ground.				
C8	PF2	LCD_SEG 0	EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
C9	PE6	LCD_COM 2			US0_RX #1	
C10	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
C11	PC11	ACMP1_CH3			US0_TX #2	
D1	PA3	LCD_SEG 16	EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
D2	PA2	LCD_SEG 15	EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0
D3	PB15					
D4	VSS	Ground.				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9	LCD_SEG 28	EBI_CS0 #0			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1
D9	PE7	LCD_COM 3			US0_TX #1	
D10	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
D11	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
E1	PA6	LCD_SEG 19	EBI_AD15 #0		LEU1_RX #1	
E2	PA5	LCD_SEG 18	EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
E3	PA4	LCD_SEG 17	EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
E4	PB0	LCD_SEG 32		TIM1_CC0 #2		
E8	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

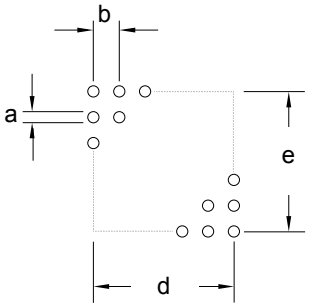

Figure 6.4. BGA112 PCB Stencil Design

Table 6.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.33
b	0.80
d	8.00
e	8.00

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
D	0.170	—	0.270	S1	—	4.500 BSC	—
E	0.950	—	1.050	V	—	9.000 BSC	—
F	0.170	—	0.230	V1	—	4.5000 BSC	—
G	—	0.500 BSC	—	W	—	0.200 BSC	—
H	0.050	—	0.150	AA	—	1.000BSC	—
J	0.090	—	0.200				
K	0.500	—	0.700				
L	0DEG	—	7DEG				

The TQFP48 Package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

9.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.

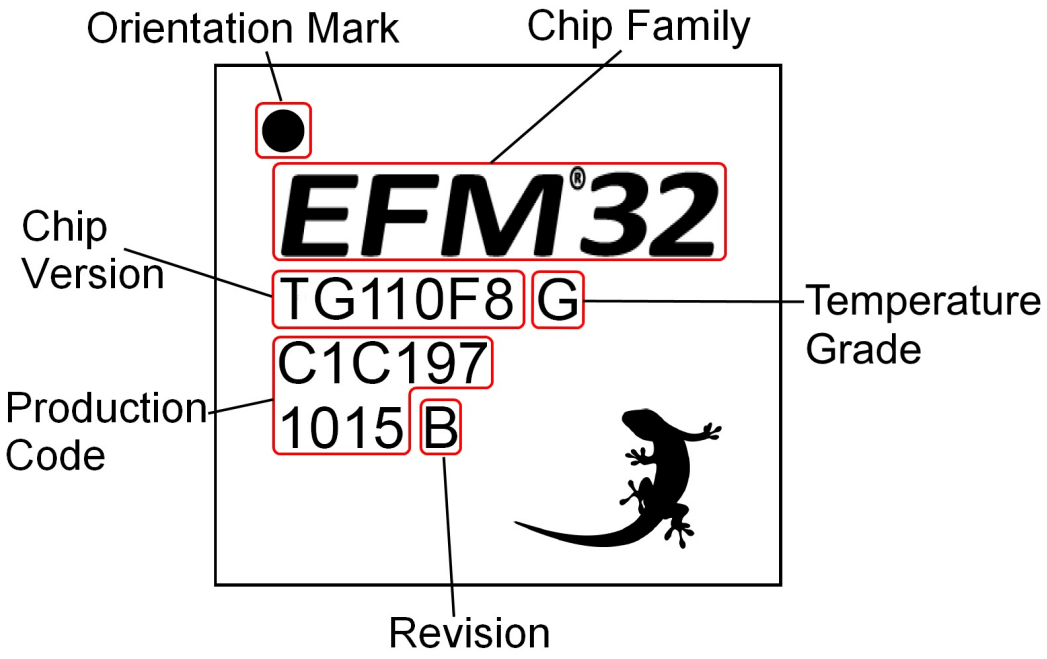

Figure 9.5. Example Chip Marking (Top View)

10.2 QFN64 PCB Layout

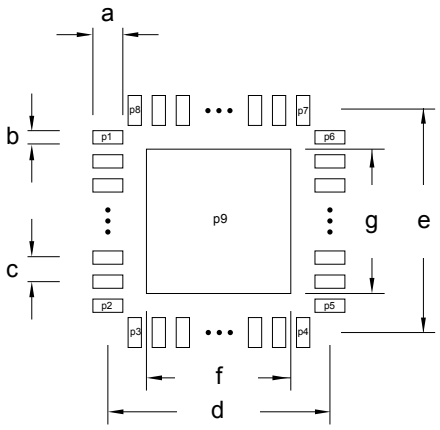

Figure 10.2. QFN64 PCB Land Pattern

Table 10.2. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.85	P1	1	P8	64
b	0.30	P2	16	P9	65
c	0.50	P3	17		
d	8.90	P4	32		
e	8.90	P5	33		
f	7.20	P6	48		
g	7.20	P7	49		

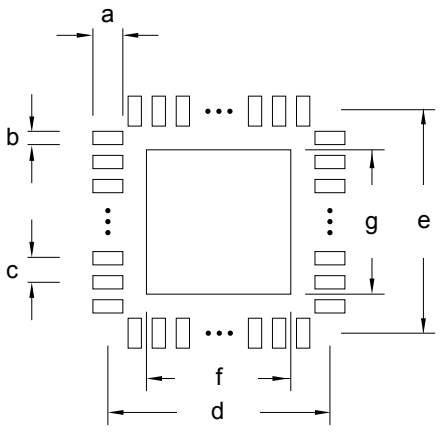

Figure 10.3. QFN64 PCB Solder Mask

Table 10.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.97	e	8.90
b	0.42	f	7.32
c	0.50	g	7.32

13.11 Revision 1.20

December 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Increased max storage temperature.

Added data for <150°C and <70°C on Flash data retention.

Changed latch-up sensitivity test description.

Added IO leakage current.

For LQFP100 devices, updated ESD CDM value.

Added Flash current consumption.

Updated HFRCO data.

Updated LFRCO data.

Added graph for ADC Absolute Offset over temperature.

Added graph for ADC Temperature sensor readout.

13.12 Revision 1.11

November 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Corrected maximum DAC clock speed for continuous mode.

Added DAC sample-hold mode voltage drift rate.

Added pulse widths detected by the HFXO glitch detector.

Added power sequencing information to Power Management section.