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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g280f128-qfp100t

3.2 Configuration Summary

3.2.1 EFM32G200

The features of the EFM32G200 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.1. EFM32G200 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:5], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:4]
DAC0	Full configuration	DAC0_OUT[0]
GPIO	24 pins	Available pins are shown in Table 4.3 (p. 57)

3.2.2 EFM32G210

The features of the EFM32G210 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.2. EFM32G210 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:5], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:4]
DAC0	Full configuration	DAC0_OUT[0]
AES	Full configuration	NA
GPIO	24 pins	Available pins are shown in Table 4.3 (p. 57)

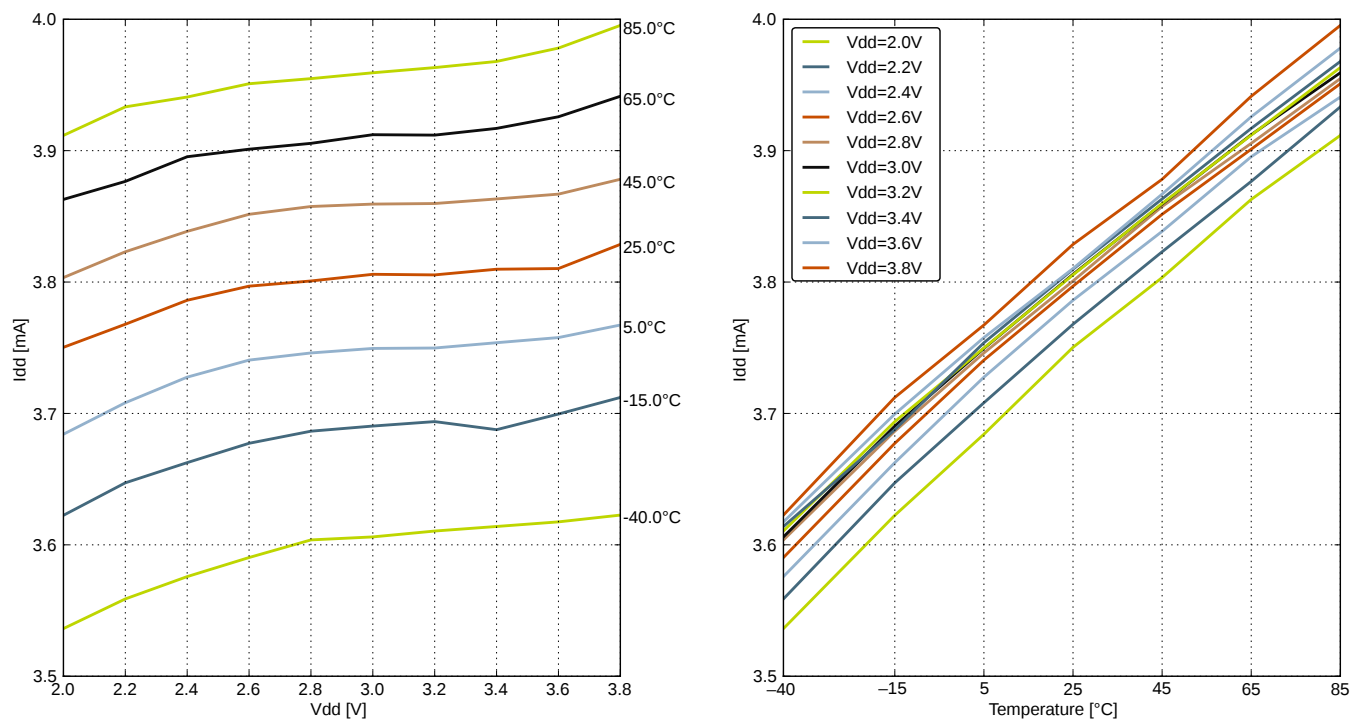


Figure 4.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz

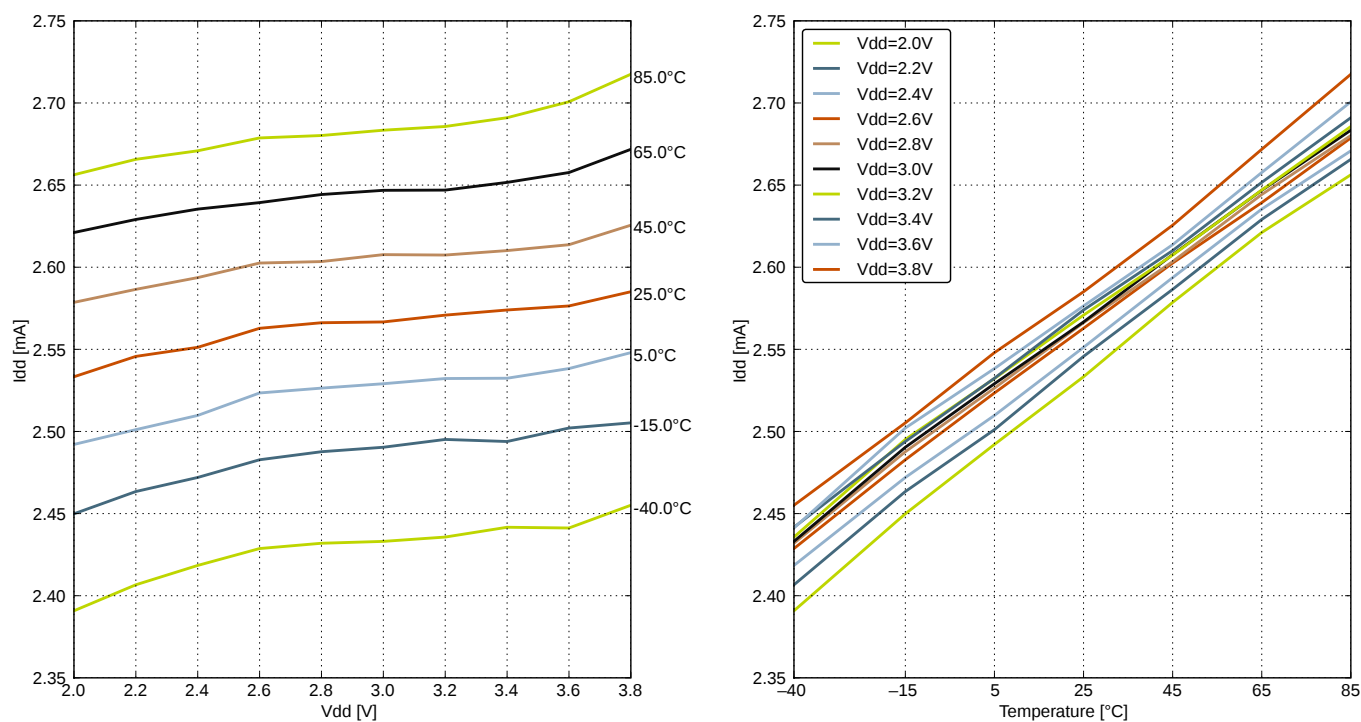


Figure 4.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

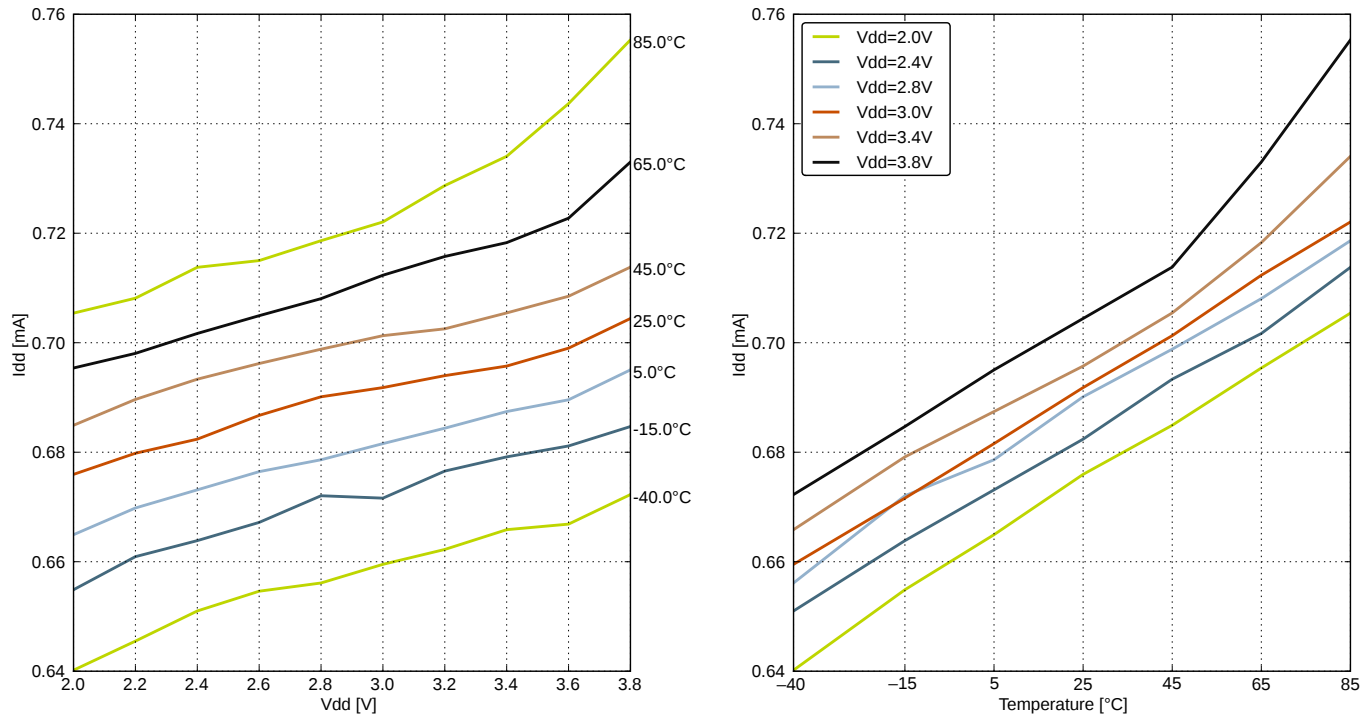


Figure 4.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz

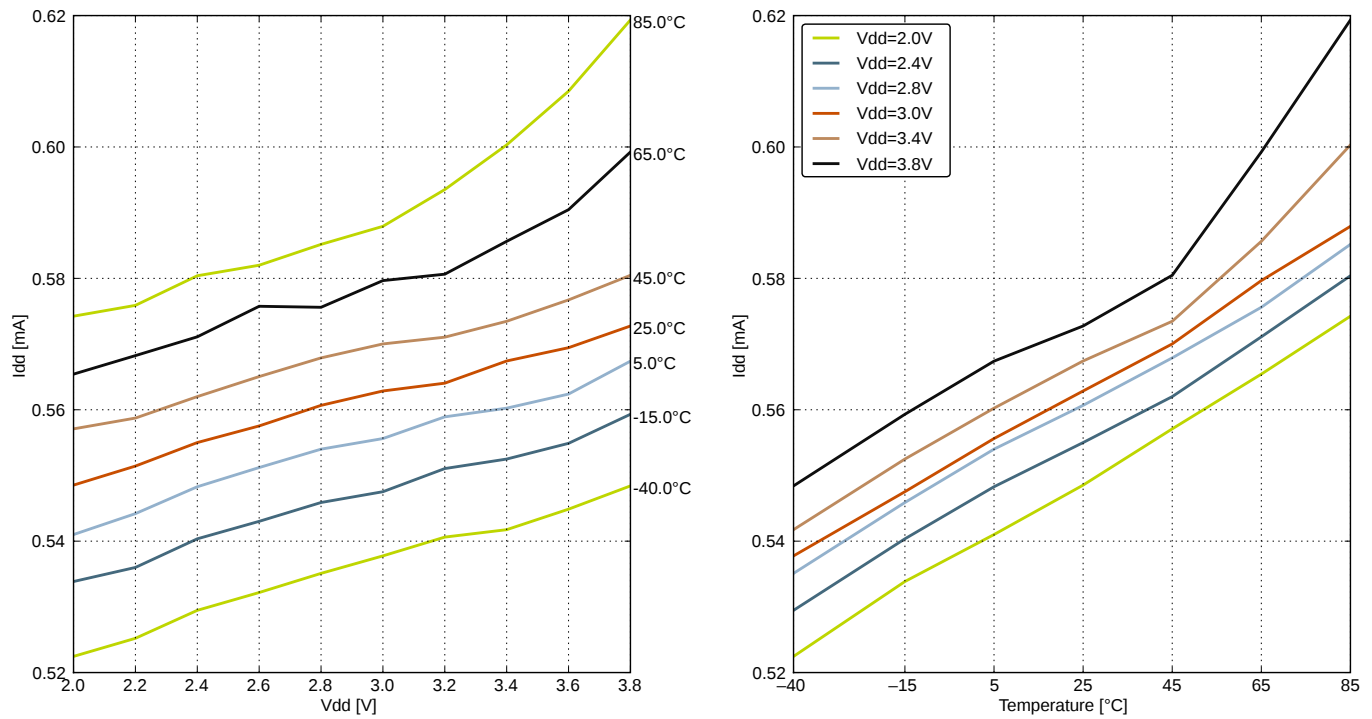


Figure 4.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

4.4.4 EM3 Current Consumption

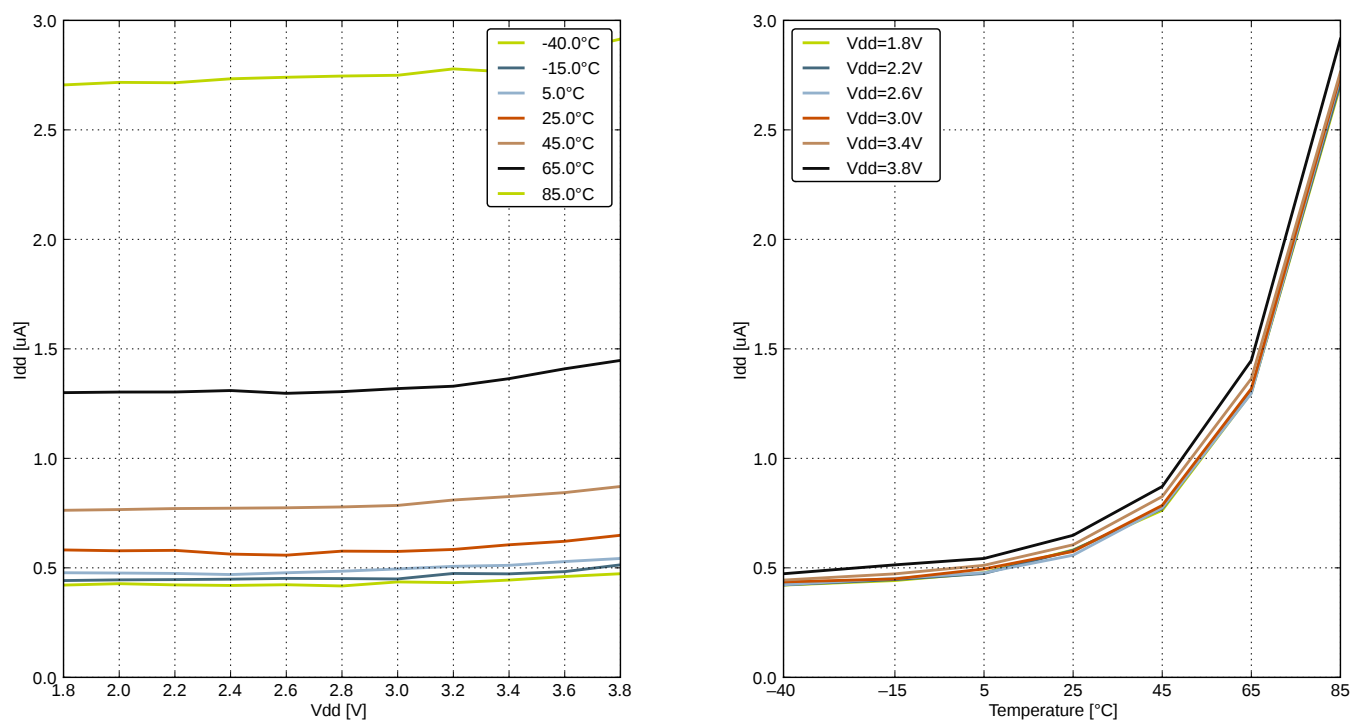


Figure 4.12. EM3 Current Consumption

4.6 Power Management

The EFM32G requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 4.5. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$	EM0	1.74	—	1.96	V
		EM1	1.74	—	1.96	V
		EM2	1.74	—	1.96	V
BOD threshold on rising external supply voltage	$V_{BODextthr+}$	EM0	—	1.85	—	V
Power-on Reset (POR) threshold on rising external supply voltage	$V_{PORthr+}$		—	—	1.98	V
Delay from reset is released until program execution starts	$t_{RESETdy}$	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	μ s
negative pulse length to ensure complete reset of device	t_{RESET}		50	—	—	ns
Voltage regulator decoupling capacitor.	$C_{DECOUPLE}$	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	μ F

4.9 Oscillators

4.9.1 LFXO

Table 4.8. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	30	120	kOhm
Supported crystal external load range	C_{LFXOL}		$\times^1$	—	25	pF
Current consumption for core and buffer after startup	I_{LFXO}	ESR=30 k Ω , C_L =10 pF, LFXO-BOOST in CMU_CTRL is 1	—	190	—	nA
Start-up time	t_{LFXO}	ESR=30 k Ω , C_L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1	—	400	—	ms
Note: 1. See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in Configurator in Simplicity Studio.						

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

4.9.5 AUXHFRCO

Table 4.12. AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, $V_{DD}=3.0$ V, $T_{AMB}=25$ °C	$f_{AUXHFRCO}$	14 MHz frequency band	13.580	14.0	14.420	MHz
Settling time after start-up	$t_{AUXHFRCO_settling}$	$f_{AUXHFRCO} = 14$ MHz	—	0.6	—	Cycles
Duty cycle	$DC_{AUXHFRCO}$	$f_{AUXHFRCO} = 14$ MHz	48.5	50	51	%
Frequency step for LSB change in TUNING value	$TUNESTEP_{AUXHFRCO}$		—	0.3 ¹	—	%

Note:

1. The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value in the 14 MHz range across operating conditions.

4.9.6 ULFRCO

Table 4.13. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}	25 °C, 3 V	0.7	—	1.75	kHz
Temperature coefficient	TC_{ULFRCO}		—	0.05	—	%/°C
Supply voltage coefficient	VC_{ULFRCO}		—	-18.2	—	%/V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise And Distortion Ratio (SINAD)	SINAD _{ADC}	1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	58	—	dB
		1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	62	—	dB
		1 MSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	62	68	—	dB
		1 MSamples/s, 12 bit, differential, 2xV _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	68	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	61	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	62	—	dB
		200 kSamples/s, 12 bit, single-ended, VDD reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise plus Distortion Ratio (SNDR)	SNDR _{DAC}	500 kSamples/s, 12 bit, single-ended, internal 1.25 V reference	—	57	—	dB
		500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference	—	54	—	dB
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	56	—	dB
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	53	—	dB
		500 kSamples/s, 12 bit, differential, V _{DD} reference	—	55	—	dB
Spurious-Free Dynamic Range (SFDR)	SFDR _{DAC}	500 kSamples/s, 12 bit, single-ended, internal 1.25V reference	—	62	—	dBc
		500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference	—	56	—	dBc
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	61	—	dBc
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	55	—	dBc
		500 kSamples/s, 12 bit, differential, V _{DD} reference	—	60	—	dBc
Offset voltage	V _{DACOFFSET}	After calibration, single-ended	—	2	—	mV
		After calibration, differential	—	2	—	mV
Sample-hold mode voltage drift	V _{DACSHMDRIFT}		—	540	—	μV/ms
Differential non-linearity	DNL _{DAC}		—	±1	—	LSB
Integral non-linearity	INL _{DAC}		—	±5	—	LSB
No missing codes	MC _{DAC}		—	12	—	bits
Load current	I _{LOAD_DC}		—	—	11	mA
VREF voltage	V _{REF}	1.25 V reference	1.2	1.25	1.3	V
		2.5 V reference	2.4	2.5	2.6	V
VREF voltage drift	V _{REF_VDRIFT}	1.25 V reference	-12.4	2.9	18.2	mV/V
		2.5 V reference, V _{DD} > 2.5 V	-24.6	5.7	35.2	mV/V
VREF temperature drift	V _{REF_TDRIFT}	1.25 V reference	-132	272	677	μV/°C
		2.5 V reference	-231	545	1271	μV/°C
VREF current consumption	I _{VREF}	1.25 V reference	—	67	114	μA
		2.5 V reference	—	55	82	μA
ADC and DAC VREF matching	V _{REF_MATCH}	1.25 V reference	—	99.85	—	%
		2.5 V reference	—	100.01	—	%

Note:

1. Measured with a static input code and no loading on the output. Includes required contribution from the voltage reference.

4.14 LCD

Table 4.18. LCD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frame rate	f_{LCDFR}		30	—	200	Hz
Number of segments supported	NUM_{SEG}		—	4×40	—	seg
LCD supply voltage range	V_{LCD}	Internal boost circuit enabled	2.0	—	3.8	V
Steady state current consumption.	I_{LCD}	Display disconnected, static mode, framerate 32 Hz, all segments on.	—	250	—	nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONE-THIRD in LCD_DISPCTRL register.	—	550	—	nA
Steady state Current contribution of internal boost.	I_{LCDBOOST}	Internal voltage boost off	—	0	—	μA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.	—	8.4	—	μA
Boost Voltage	V_{BOOST}	VBLEV of LCD_DISPCTRL register to LEVEL0	—	3.0	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL1	—	3.08	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL2	—	3.17	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL3	—	3.26	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL4	—	3.34	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL5	—	3.43	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL6	—	3.52	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL7	—	3.6	—	V

The total LCD current is given by the following equation. I_{LCDBOOST} is zero if internal boost is off.

$$I_{\text{LCDTOTAL}} = I_{\text{LCD}} + I_{\text{LCDBOOST}}$$

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
7	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
8	PC2	ACMP0_CH2			
9	PC3	ACMP0_CH3			
10	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0		
11	PB7	LFXTAL_P		US1_CLK #0	
12	PB8	LFXTAL_N		US1_CS #0	
13	PA8		TIM2_CC0 #0		
14	PA9		TIM2_CC1 #0		
15	PA10		TIM2_CC2 #0		
16	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
17	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
18	VSS	Ground.			
19	AVDD_1	Analog power supply 1.			
20	PB13	HFXTAL_P		LEU0_TX #1	
21	PB14	HFXTAL_N		LEU0_RX #1	
22	IOVDD_3	Digital IO power supply 3.			
23	AVDD_0	Analog power supply 0.			
24	PD4	ADC0_CH4		LEU0_TX #0	
25	PD5	ADC0_CH5		LEU0_RX #0	
26	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
27	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
28	VDD_DREG	Power supply for on-chip voltage regulator.			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
30	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
31	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
32	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
33	PC11	ACMP1_CH3		US0_TX #2	
34	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
35	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
36	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
37	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
HFX TAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		I2C0 Serial Data input / output.
LCD_BCAP_N	PA13				LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12				LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14				LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4				LCD driver common line number 0.
LCD_COM1	PE5				LCD driver common line number 1.
LCD_COM2	PE6				LCD driver common line number 2.
LCD_COM3	PE7				LCD driver common line number 3.
LCD_SEG0	PF2				LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3				LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4				LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5				LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8				LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9				LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10				LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11				LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12				LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.

5.8 EFM32G842 (TQFP64)

5.8.1 Pinout

The EFM32G842 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

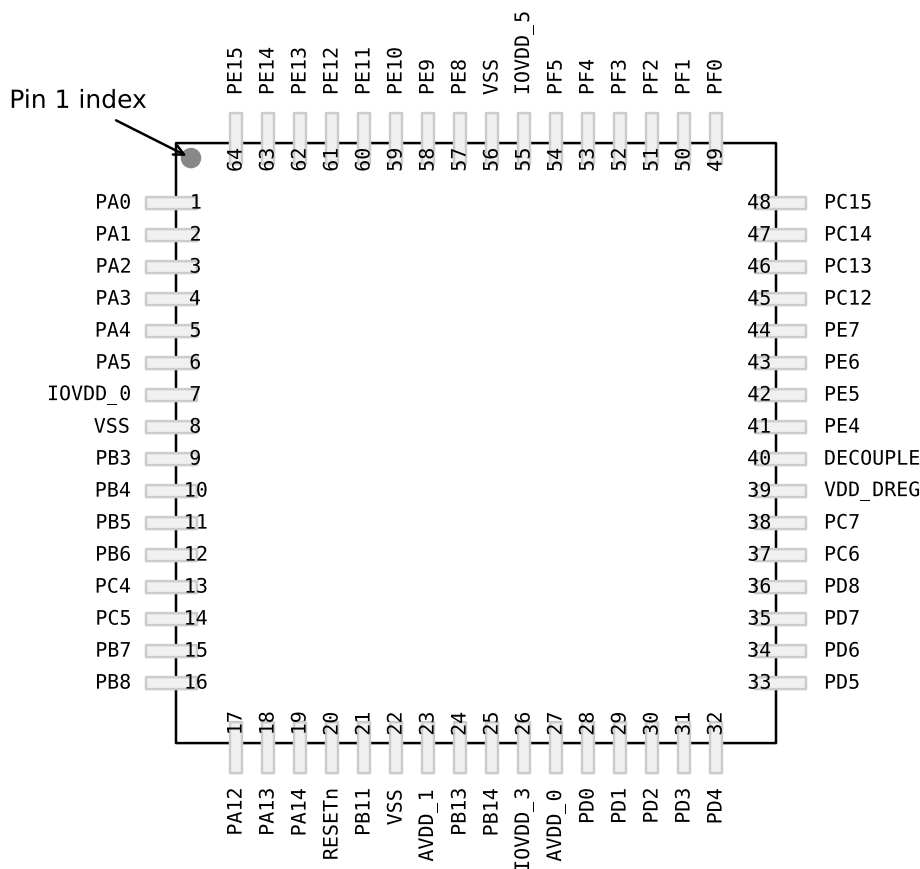


Figure 5.8. EFM32G842 Pinout (top view, not to scale)

Table 5.22. Device Pinout

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0	LCD_SEG13	TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1	LCD_SEG14	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2	LCD_SEG15	TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3	LCD_SEG16	TIM0_CDTI0 #0		
5	PA4	LCD_SEG17	TIM0_CDTI1 #0		

5.8.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G842 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.24. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	PA14	PA13	PA12	—	—	—	—	—	—	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	PB6	PB5	PB4	PB3	—	—	—
Port C	PC15	PC14	PC13	PC12	—	—	—	—	PC7	PC6	PC5	PC4	—	—	—	—
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

5.10.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G890 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.30. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	—	—	—	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

		SYMBOL	MIN	NOM	MAX
	x	D	16 BSC		
	y	E	16 BSC		
body size	x	D1	14 BSC		
	y	E1	14 BSC		
lead pitch		e	0.5 BSC		
		L	0.45	0.6	0.75
footprint		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	—	—
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	—	—
		R1	0.08	—	0.2
		S	0.2	—	—
package edge tolerance		aaa	0.2		
lead edge tolerance		bbb	0.2		
coplanarity		ccc	0.08		
lead offset		ddd	0.08		
mold flatness		eee	0.05		

The LQFP100 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>

Symbol	Min	Nom	Max
e	0.50 BSC		
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

The QFN64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

12. Chip Revision, Solder Information, Errata

12.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

12.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

12.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and on-line at: <http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

13.21 Revision 0.80

October 19th, 2009

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Initial preliminary revision