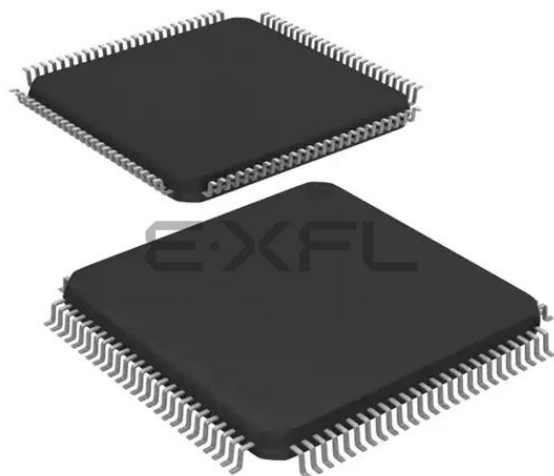




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g280f64g-e-qfp100

2. Ordering Information

The following table shows the available EFM32G devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32G200F16G-E-QFN32	16	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F32G-E-QFN32	32	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F64G-E-QFN32	64	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G210F128G-E-QFN32	128	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G222F32G-E-QFP48	32	8	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F64G-E-QFP48	64	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F128G-E-QFP48	128	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G230F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G232F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G280F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G290F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G840F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G842F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G880F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G890F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112

3.2.8 EFM32G840

The features of the EFM32G840 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.8. EFM32G840 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:4], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:4], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 57)
LCD	Full configuration	LCD_SEG[23:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

4.4 Current Consumption

Table 4.3. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	32 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	180	—	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	181	206	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	183	207	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	185	211	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	186	215	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	191	218	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	220	—	$\mu\text{A}/\text{MHz}$
EM1 current (Production test condition = 14 MHz)	I_{EM1}	32 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	45	—	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	47	62	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	48	64	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	50	69	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	51	72	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	56	83	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	103	—	$\mu\text{A}/\text{MHz}$
EM2 current	I_{EM2}	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25\text{ }^{\circ}\text{C}$	—	0.9	1.5	μA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85\text{ }^{\circ}\text{C}$	—	3.0	6.0	μA
EM3 current	I_{EM3}	$V_{DD}=3.0\text{ V}$, $T_{AMB}=25\text{ }^{\circ}\text{C}$	—	0.59	1.0	μA
		$V_{DD}=3.0\text{ V}$, $T_{AMB}=85\text{ }^{\circ}\text{C}$	—	2.75	5.8	μA
EM4 current	I_{EM4}	$V_{DD}=3.0\text{ V}$, $T_{AMB}=25\text{ }^{\circ}\text{C}$	—	0.02	0.045	μA
		$V_{DD}=3.0\text{ V}$, $T_{AMB}=85\text{ }^{\circ}\text{C}$	—	0.25	0.7	μA

4.4.1 EM0 Current Consumption

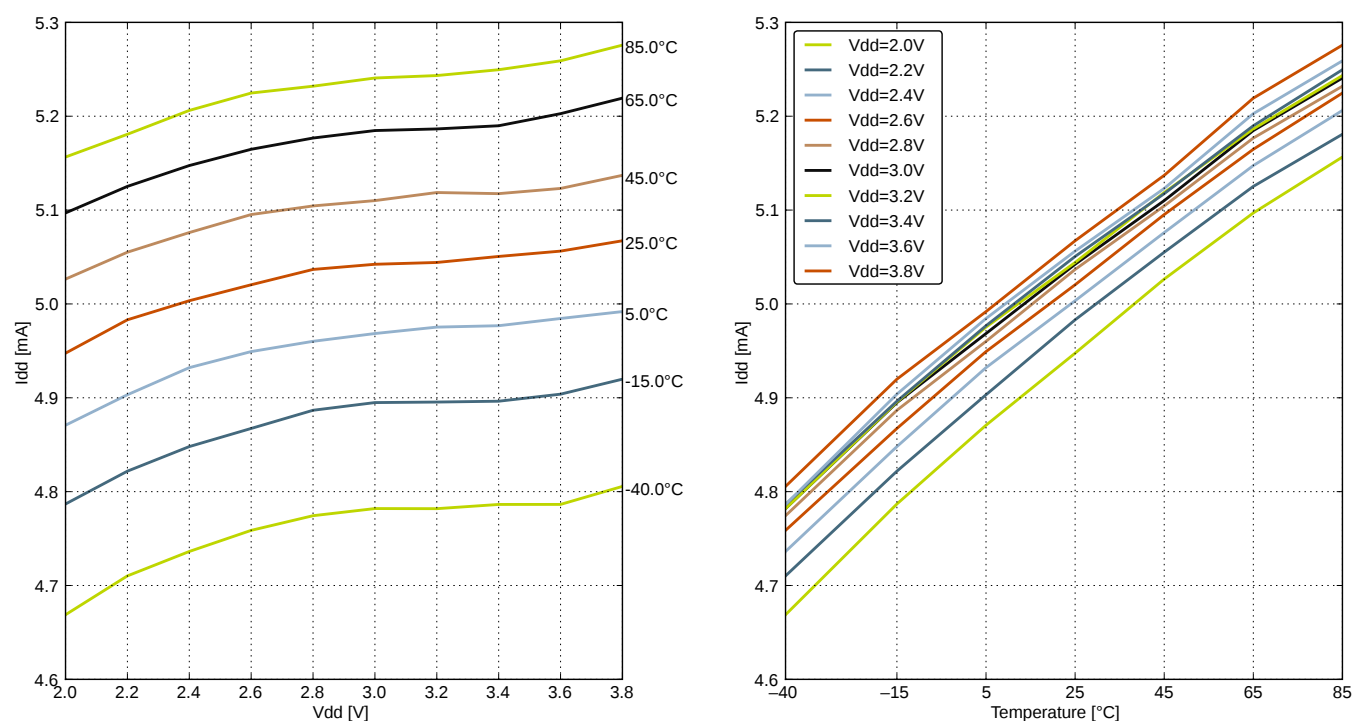


Figure 4.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28 MHz

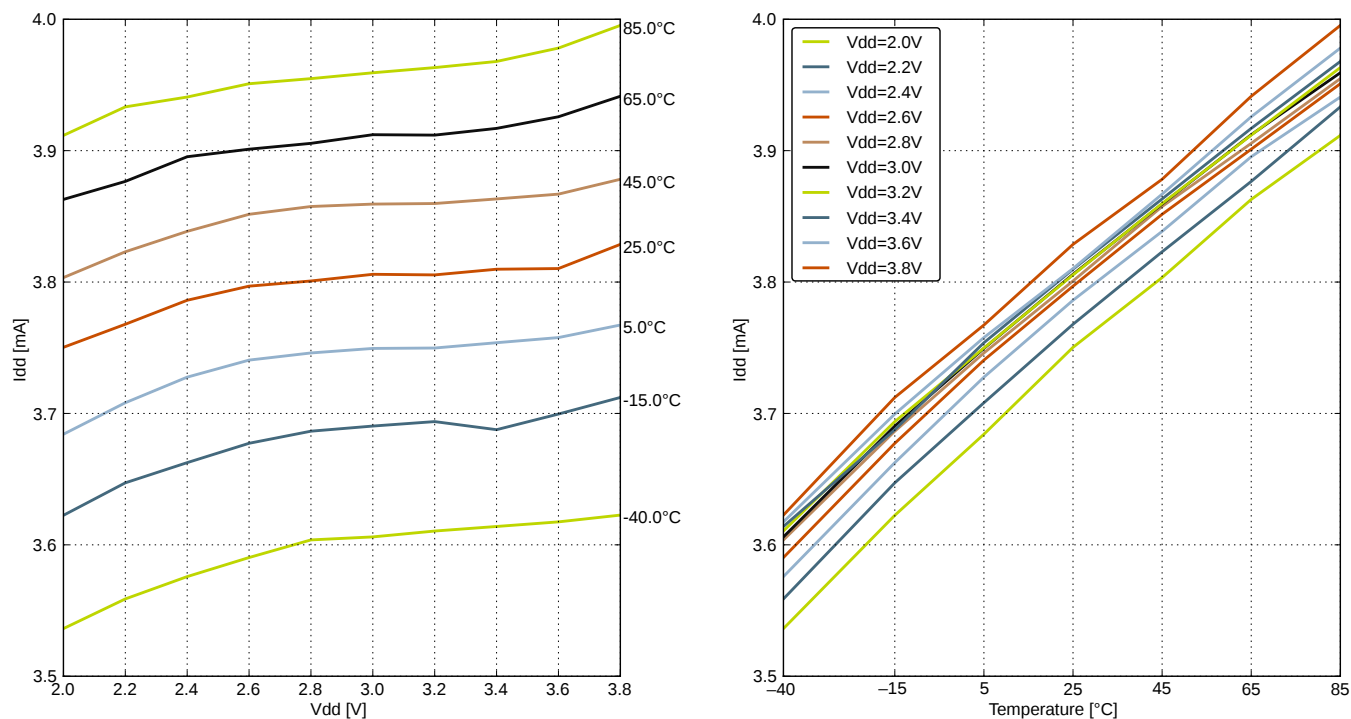


Figure 4.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz

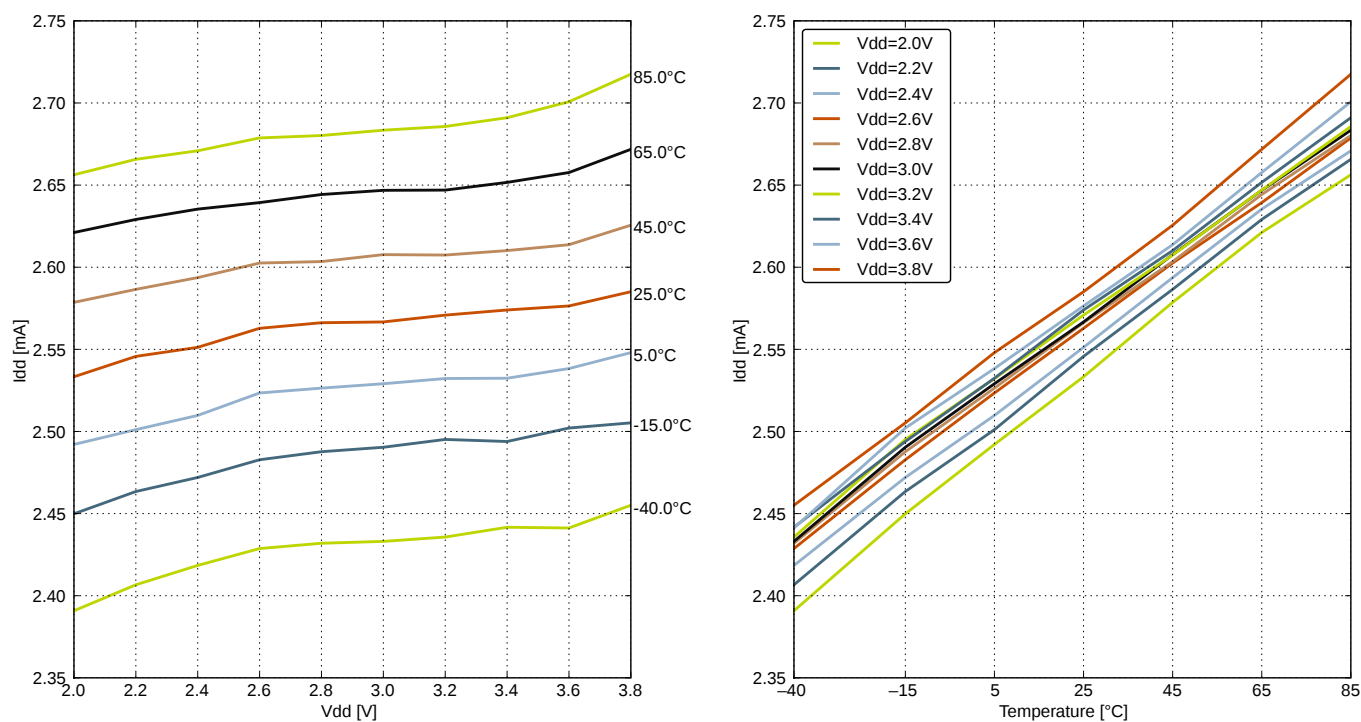


Figure 4.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

4.4.4 EM3 Current Consumption

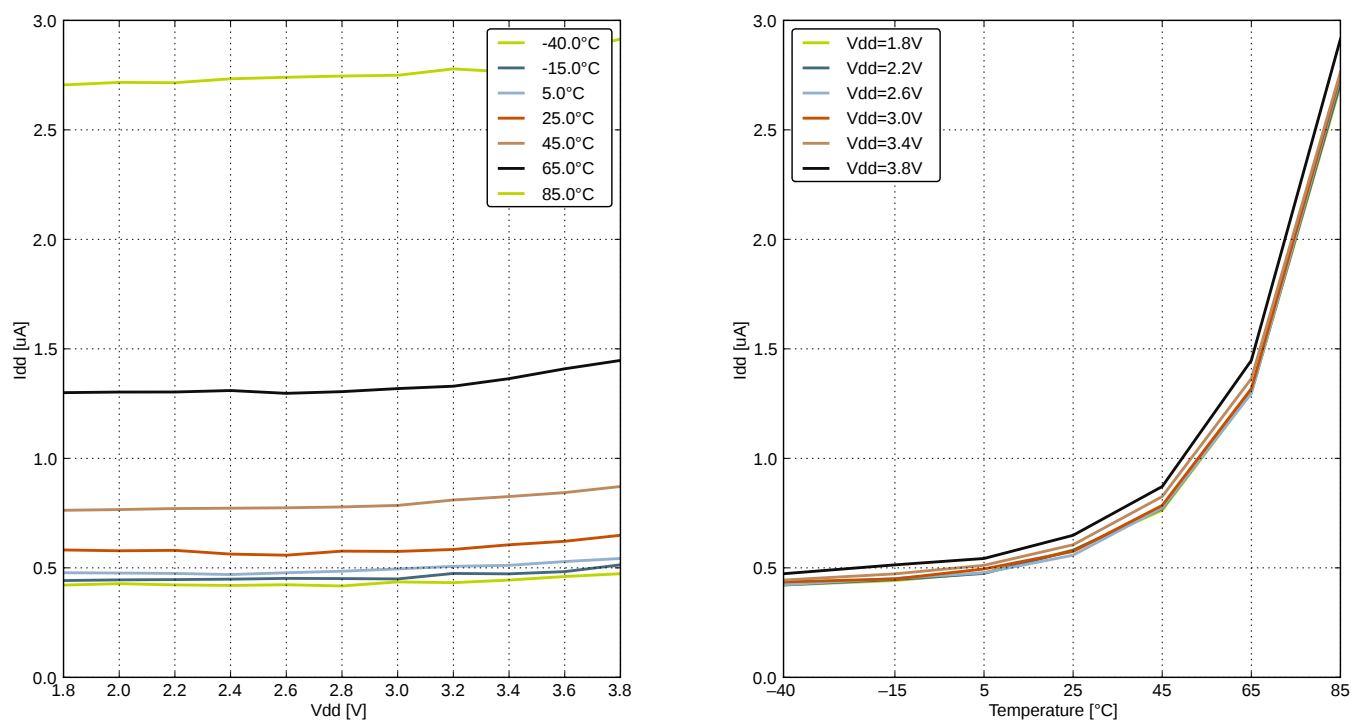


Figure 4.12. EM3 Current Consumption

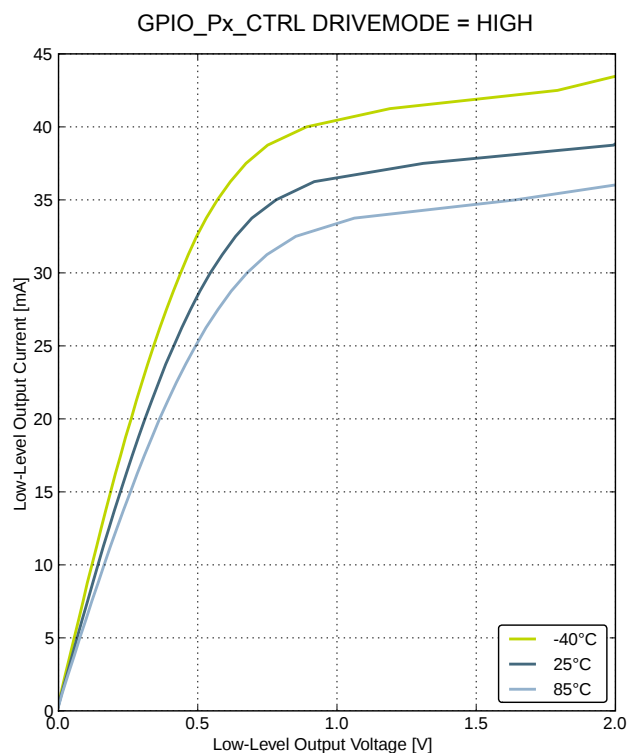
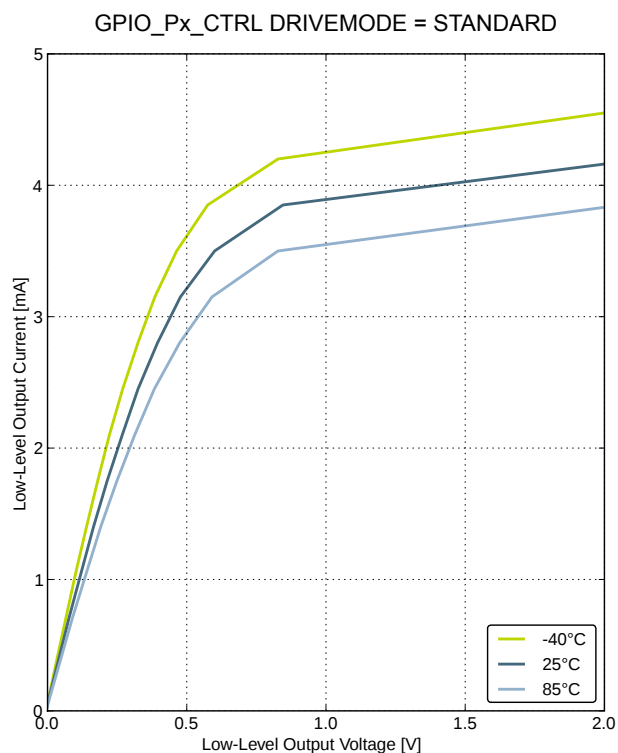
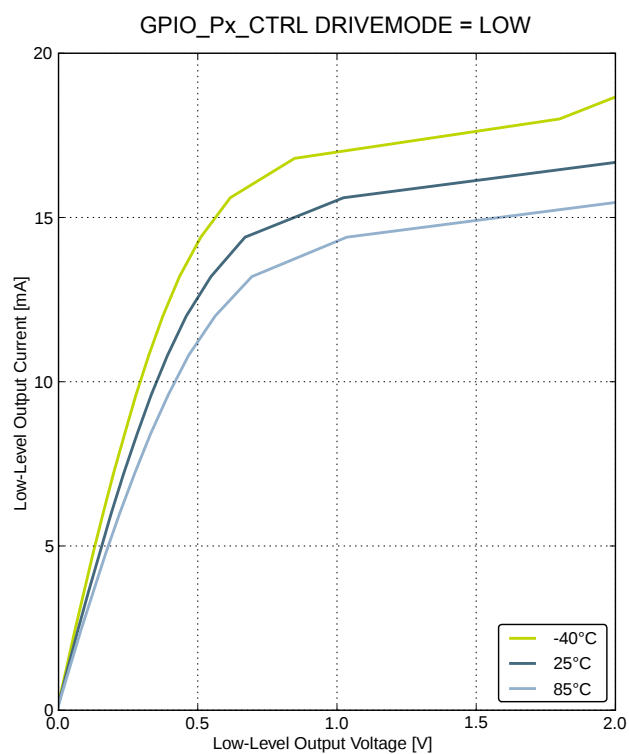
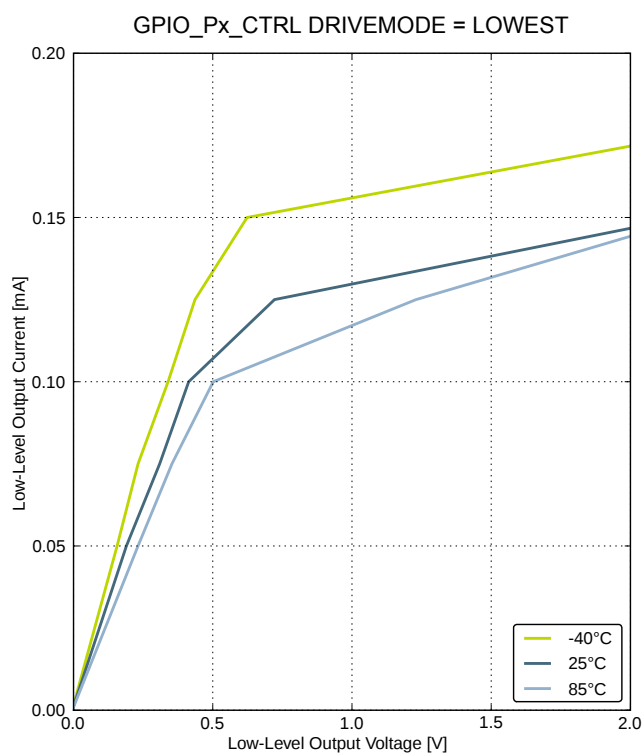


Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage

4.10 Analog Digital Converter (ADC)

Table 4.14. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ADCIN}	Single-ended	0	—	V_{REF}	V
		Differential	$-V_{\text{REF}}/2$	—	$V_{\text{REF}}/2$	V
Input range of external reference voltage, single-ended and differential	V_{ADCREFIN}		1.25	—	V_{DD}	V
Input range of external negative reference voltage on channel 7	$V_{\text{ADCREFIN_CH7}}$	See V_{ADCREFIN}	0	—	$V_{\text{DD}} - 1.1$	V
Input range of external positive reference voltage on channel 6	$V_{\text{ADCREFIN_CH6}}$	See V_{ADCREFIN}	0.625	—	V_{DD}	V
Common mode input range	V_{ADCCMIN}		0	—	V_{DD}	V
Input current	I_{ADCIN}	2 pF sampling capacitors	—	<100	—	nA
Analog input common mode rejection ratio	CMRR_{ADC}		—	65	—	dB
Average active current	I_{ADC}	1 Msamples/s, 12 bit, external reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	735 ¹	—	μA
		1 Msamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	760 ¹	—	μA
		500 Ksamples/s, 12 bit, external reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	346 ¹	—	μA
		500 Ksamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	354 ¹	—	μA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 00b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	52 ¹	—	μA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 01b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	50 ¹	—	μA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 10b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	54 ¹	—	μA
Input capacitance	C_{ADCIN}		—	2	—	pF
Input ON resistance	R_{ADCIN}		1	—	—	MΩ
Input RC filter resistance	R_{ADCFILT}		—	10	—	kΩ
Input RC filter/decoupling capacitance	C_{ADCFILT}		—	250	—	fF
Input bias current	$I_{\text{ADCBIASIN}}$	$V_{\text{SS}} < V_{\text{IN}} < V_{\text{DD}}$	-40	—	40	nA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input offset current	$I_{ADCOFFSETIN}$	$VSS < VIN < VDD$	-40	—	40	nA
ADC Clock Frequency	f_{ADCCLK}	BIASPROG=0x747	—	—	7	MHz
		BIASPROG=0xF4B	—	—	13	MHz
Conversion time	$t_{ADCCONV}$	6 bit	7	—	—	ADCCLK Cycles
		8 bit	11	—	—	ADCCLK Cycles
		12 bit	13	—	—	ADCCLK Cycles
Acquisition time	t_{ADCACQ}	Programmable	1	—	256	ADCCLK Cycles
Required acquisition time for VDD/3 reference	$t_{ADCACQVDD3}$		2	—	—	μs
Startup time of reference generator and ADC core	$t_{ADCSTART}$	NORMAL mode	—	5	—	μs
		KEEPADCWARM mode	—	1	—	μs

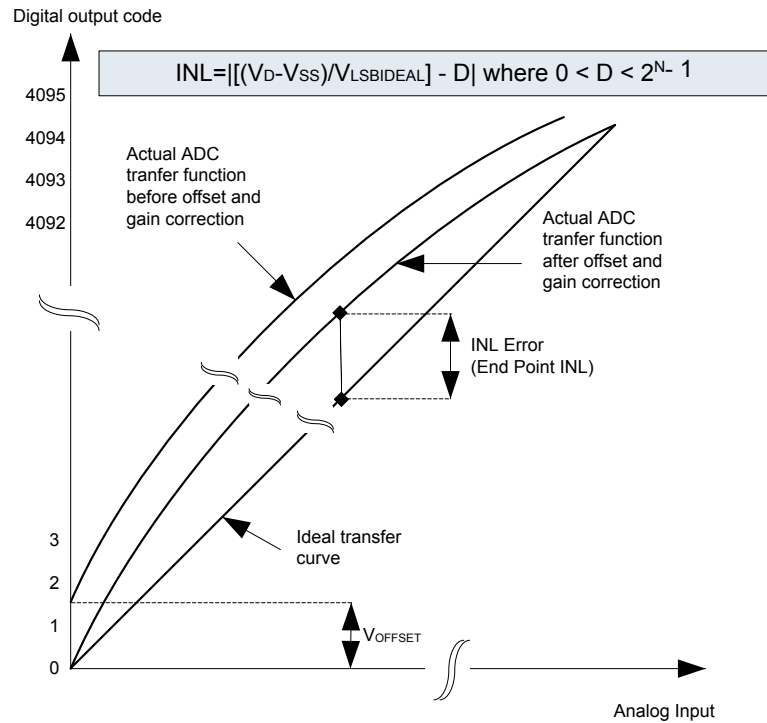


Figure 4.27. Integral Non-Linearity (INL)

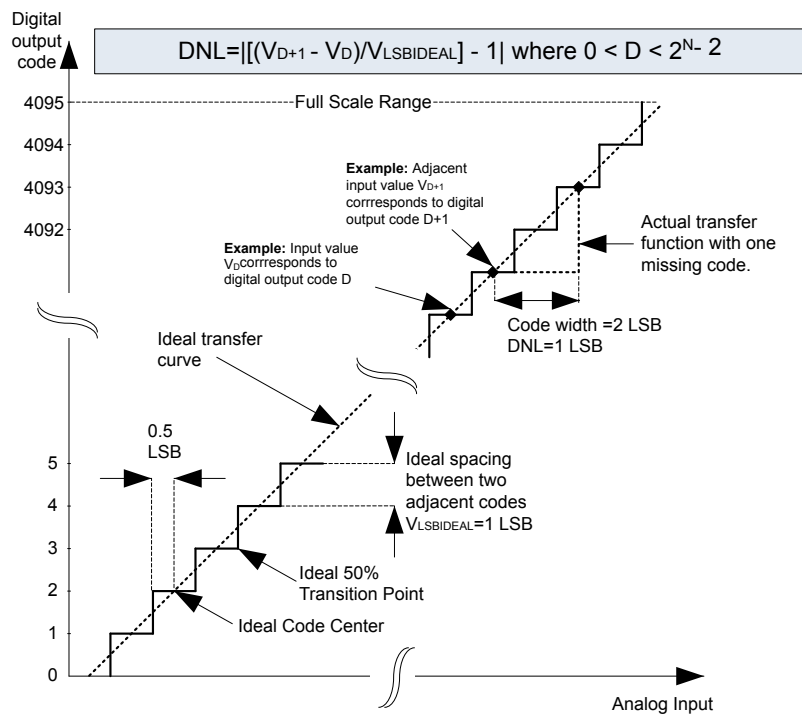


Figure 4.28. Differential Non-Linearity (DNL)

4.10.1 Typical Performance

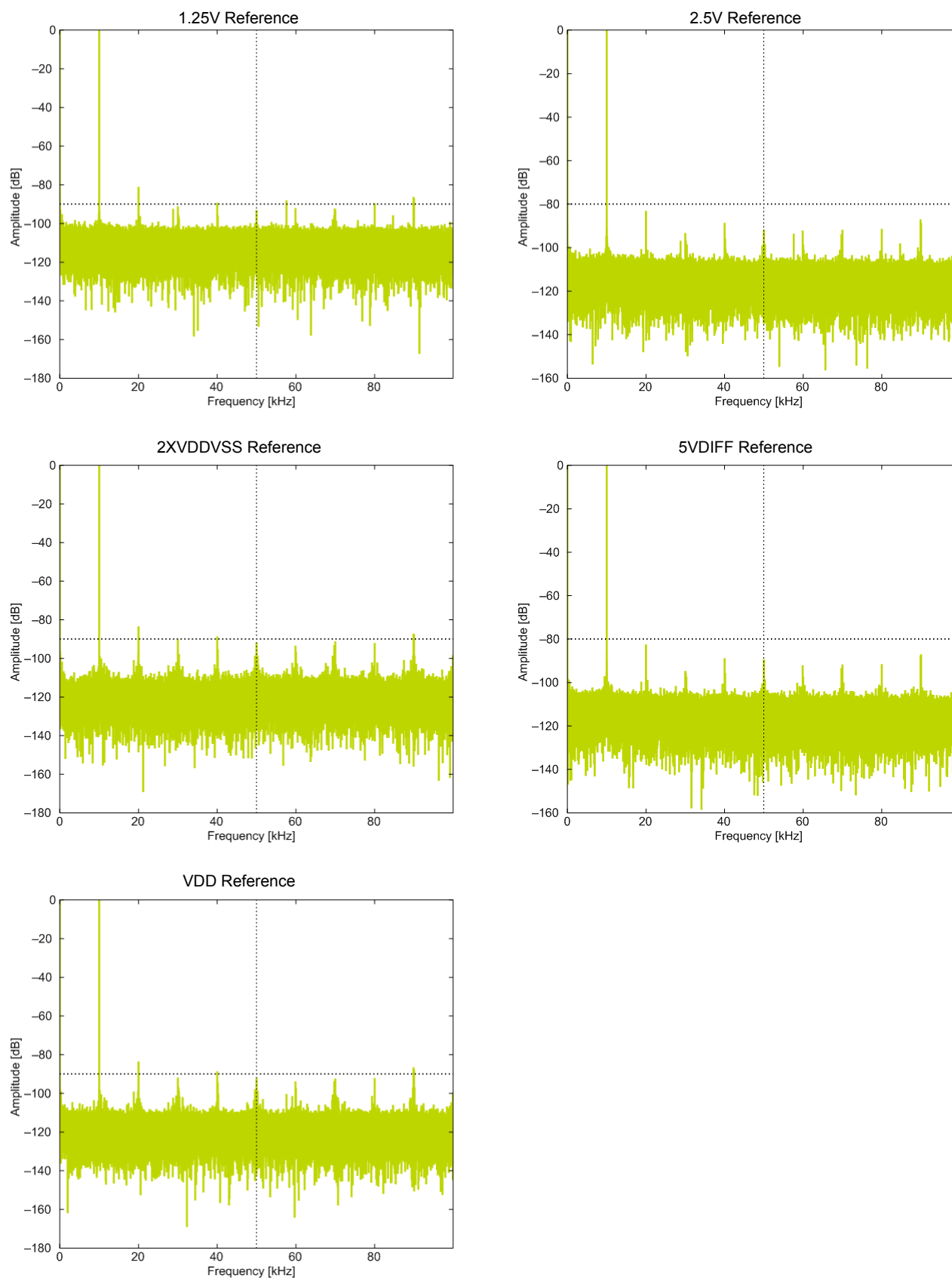


Figure 4.29. ADC Frequency Spectrum, VDD = 3V, Temp = 25°C

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
31	PE12		TIM1_CC2 #1	US0_CLK #0	
32	PE13			US0_CS #0	ACMP0_O #0

5.1.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.2. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1				Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
HFX TAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7			I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0		Low Energy Timer LETIM0, output channel 0.

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2	LCD_SEG0			ACMP1_O #0 DBG_SWO #0
52	PF3	LCD_SEG1	TIM0_CDTI0 #2		
53	PF4	LCD_SEG2	TIM0_CDTI1 #2		
54	PF5	LCD_SEG3	TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	PE8	LCD_SEG4	PCNT2_S0IN #1		
57	PE9	LCD_SEG5	PCNT2_S1IN #1		
58	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	BOOT_RX
60	PE12	LCD_SEG8	TIM1_CC2 #1	US0_CLK #0	
61	PE13	LCD_SEG9		US0_CS #0	ACMP0_O #0
62	PE14	LCD_SEG10		LEU0_TX #2	
63	PE15	LCD_SEG11		LEU0_RX #2	
64	PA15	LCD_SEG12			

5.9.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.26. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2			Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3			Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.

5.10 EFM32G890 (BGA112)

5.10.1 Pinout

The EFM32G890 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

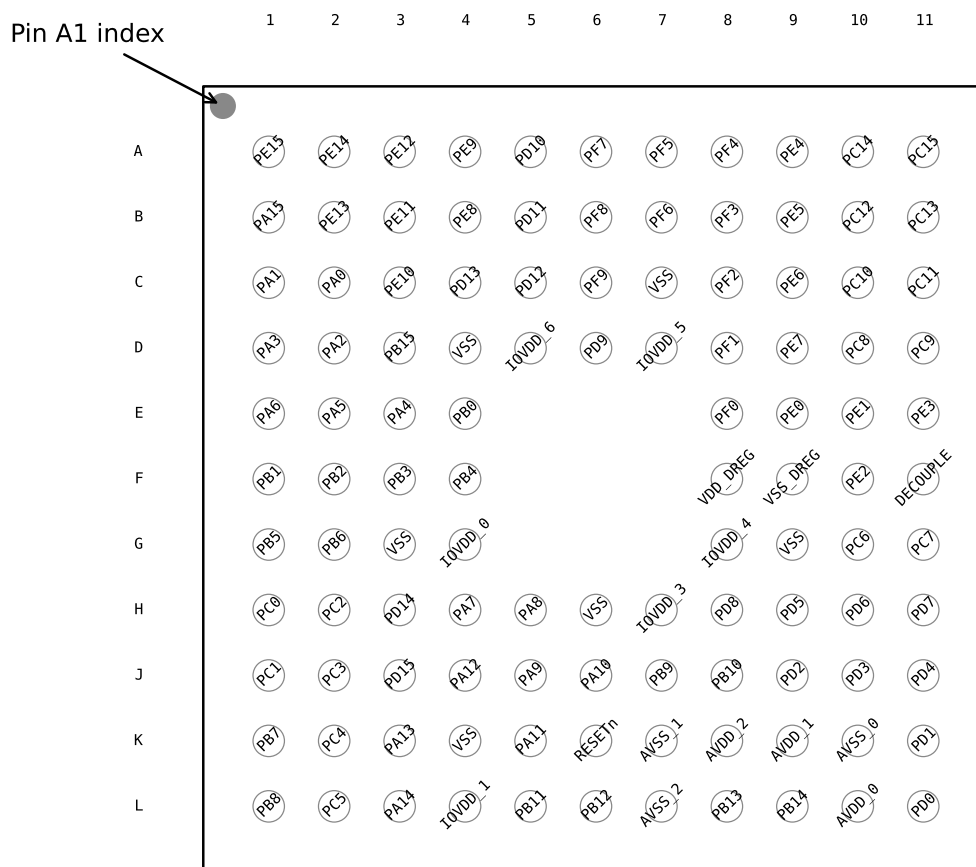


Figure 5.10. EFM32G890 Pinout (top view, not to scale)

Table 5.28. Device Pinout

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15	LCD_SEG_11	EBI_AD07 #0		LEU0_RX #2	
A2	PE14	LCD_SEG_10	EBI_AD06 #0		LEU0_TX #2	
A3	PE12	LCD_SEG_8	EBI_AD04 #0	TIM1_CC2 #1	US0_CLK #0	

5.10.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G890 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.30. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	—	—	—	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

9.2 TQFP48 PCB Layout

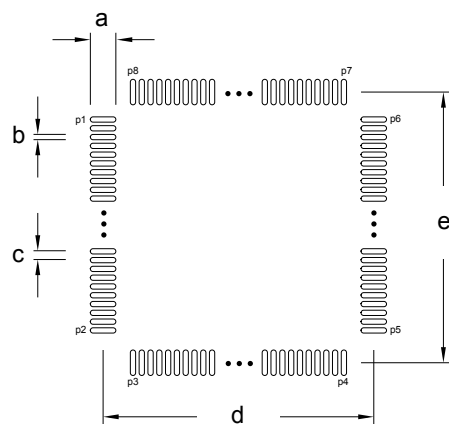


Figure 9.2. TQFP48 PCB Land Pattern

Table 9.2. TQFP48 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	1.60	P1	1	P6	36
b	0.30	P2	12	P7	37
c	0.50	P3	13	P8	48
d	8.50	P4	24		
e	8.50	P5	25		

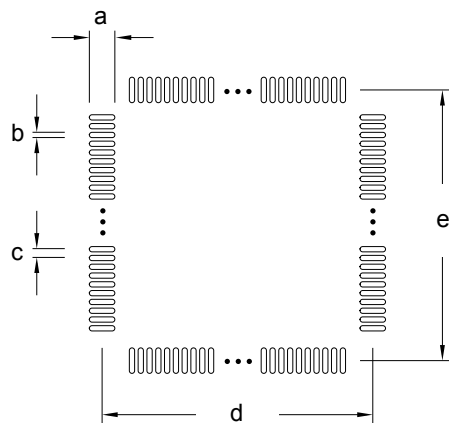


Figure 9.3. TQFP48 PCB Solder Mask

Table 9.3. TQFP48 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	8.50
e	8.50

13.21 Revision 0.80

October 19th, 2009

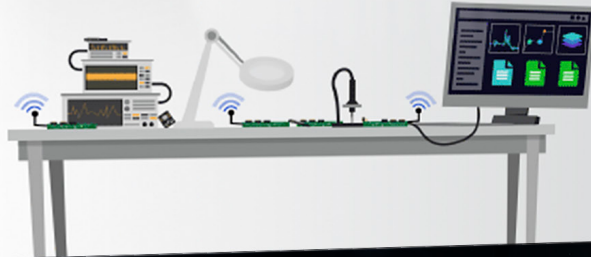
This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Initial preliminary revision

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