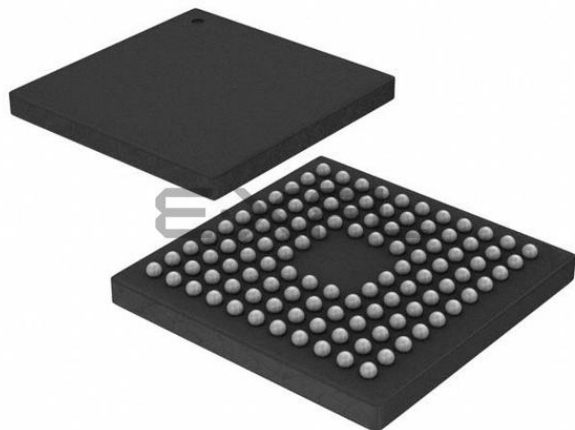




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	90
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g290f128-bga112

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4.4 Current Consumption

Table 4.3. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	32 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	180	—	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	181	206	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	183	207	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	185	211	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	186	215	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	191	218	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	220	—	$\mu\text{A}/\text{MHz}$
EM1 current (Production test condition = 14 MHz)	I_{EM1}	32 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	45	—	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	47	62	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	48	64	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	50	69	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	51	72	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	56	83	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$	—	103	—	$\mu\text{A}/\text{MHz}$
EM2 current	I_{EM2}	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25\text{ }^{\circ}\text{C}$	—	0.9	1.5	μA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85\text{ }^{\circ}\text{C}$	—	3.0	6.0	μA
EM3 current	I_{EM3}	$V_{DD}=3.0\text{ V}$, $T_{AMB}=25\text{ }^{\circ}\text{C}$	—	0.59	1.0	μA
		$V_{DD}=3.0\text{ V}$, $T_{AMB}=85\text{ }^{\circ}\text{C}$	—	2.75	5.8	μA
EM4 current	I_{EM4}	$V_{DD}=3.0\text{ V}$, $T_{AMB}=25\text{ }^{\circ}\text{C}$	—	0.02	0.045	μA
		$V_{DD}=3.0\text{ V}$, $T_{AMB}=85\text{ }^{\circ}\text{C}$	—	0.25	0.7	μA

4.4.5 EM4 Current Consumption

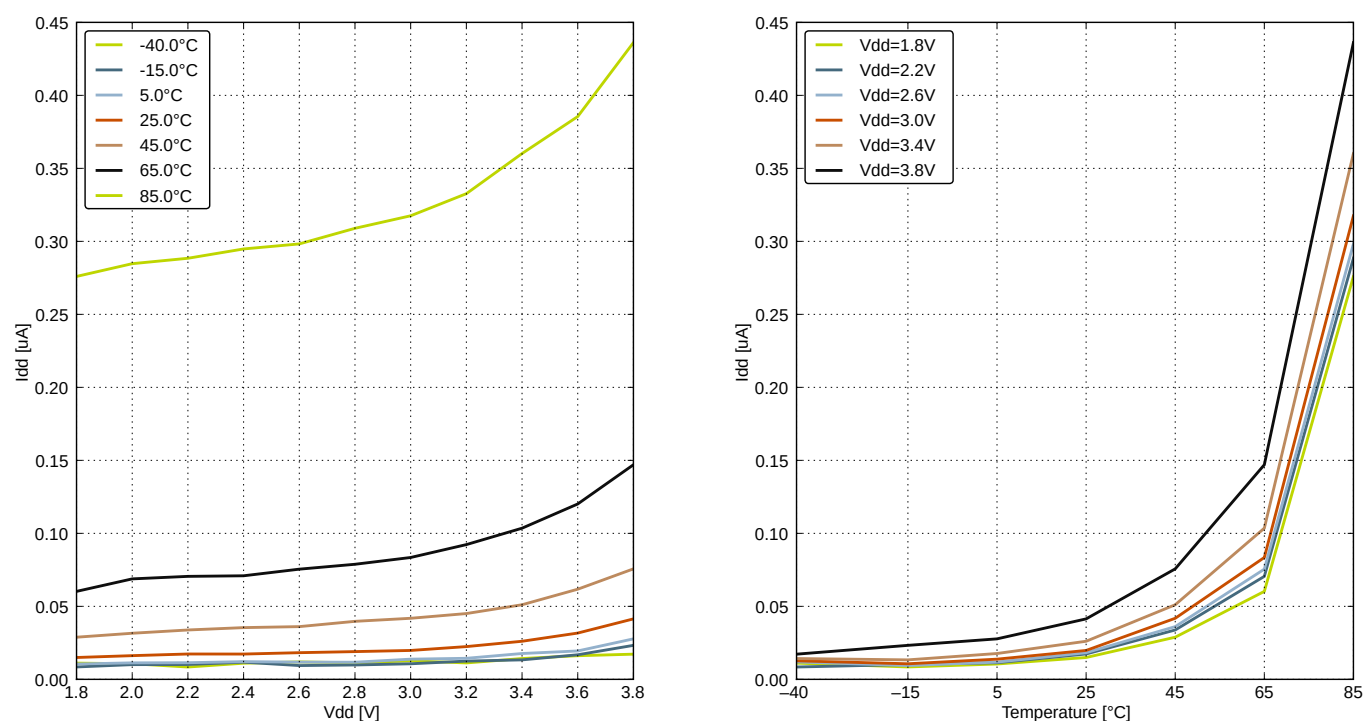


Figure 4.13. EM4 Current Consumption

4.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.4. Energy Modes Transitions

Parameter	Symbol	Min	Typ	Max	Unit
Transition time from EM1 to EM0	t_{EM10}	—	0	—	HFCORECLK cycles
Transition time from EM2 to EM0	t_{EM20}	—	2	—	μs
Transition time from EM3 to EM0	t_{EM30}	—	2	—	μs
Transition time from EM4 to EM0	t_{EM40}	—	163	—	μs

4.6 Power Management

The EFM32G requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 4.5. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$	EM0	1.74	—	1.96	V
		EM1	1.74	—	1.96	V
		EM2	1.74	—	1.96	V
BOD threshold on rising external supply voltage	$V_{BODextthr+}$	EM0	—	1.85	—	V
Power-on Reset (POR) threshold on rising external supply voltage	$V_{PORthr+}$		—	—	1.98	V
Delay from reset is released until program execution starts	$t_{RESETdy}$	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	μ s
negative pulse length to ensure complete reset of device	t_{RESET}		50	—	—	ns
Voltage regulator decoupling capacitor.	$C_{DECOUPLE}$	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	μ F

4.9 Oscillators

4.9.1 LFXO

Table 4.8. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	30	120	kOhm
Supported crystal external load range	C_{LFXOL}		$\times^1$	—	25	pF
Current consumption for core and buffer after startup	I_{LFXO}	ESR=30 k Ω , C_L =10 pF, LFXO-BOOST in CMU_CTRL is 1	—	190	—	nA
Start-up time	t_{LFXO}	ESR=30 k Ω , C_L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1	—	400	—	ms
Note: 1. See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in Configurator in Simplicity Studio.						

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

4.10.1 Typical Performance

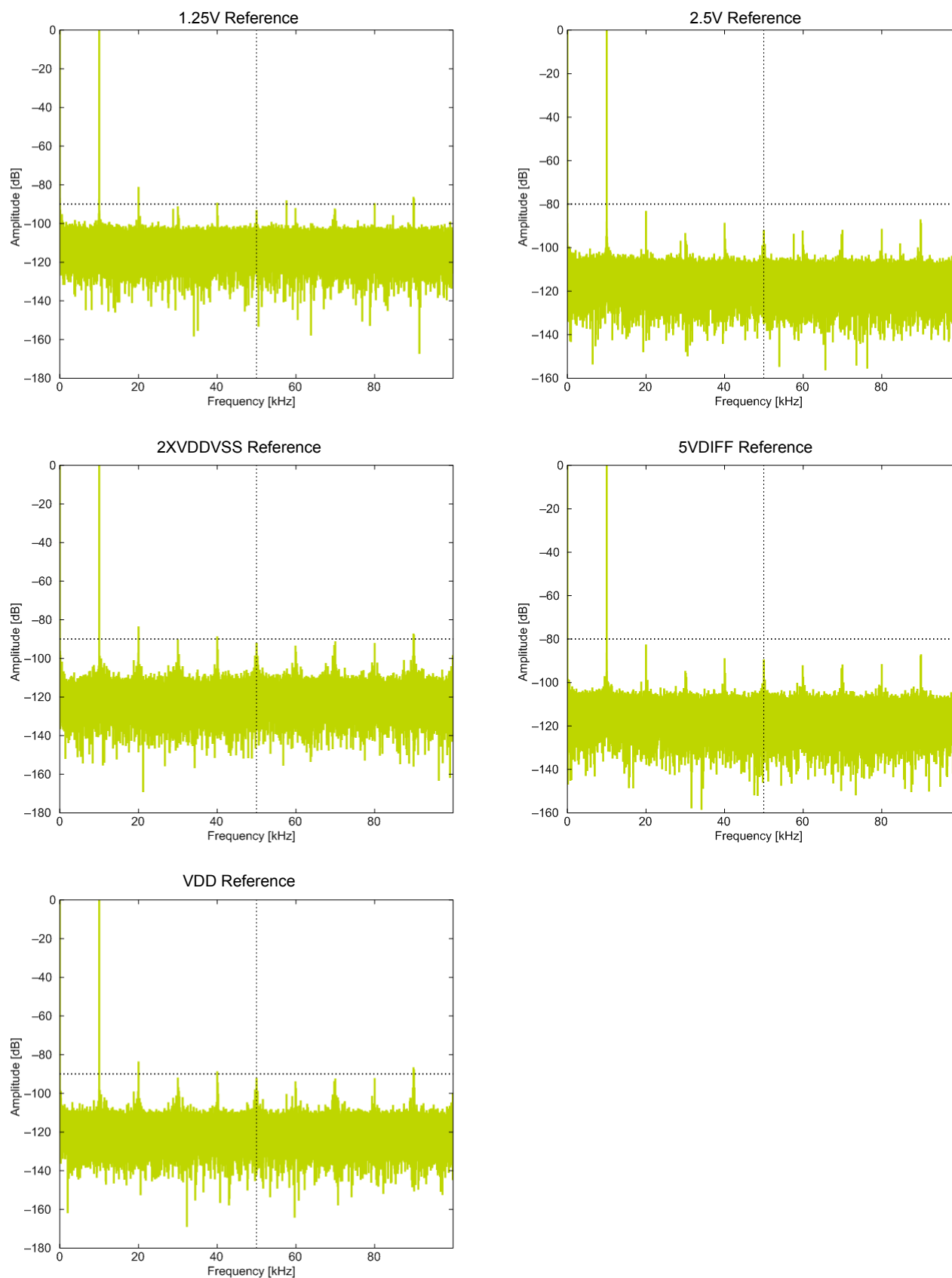


Figure 4.29. ADC Frequency Spectrum, VDD = 3V, Temp = 25°C

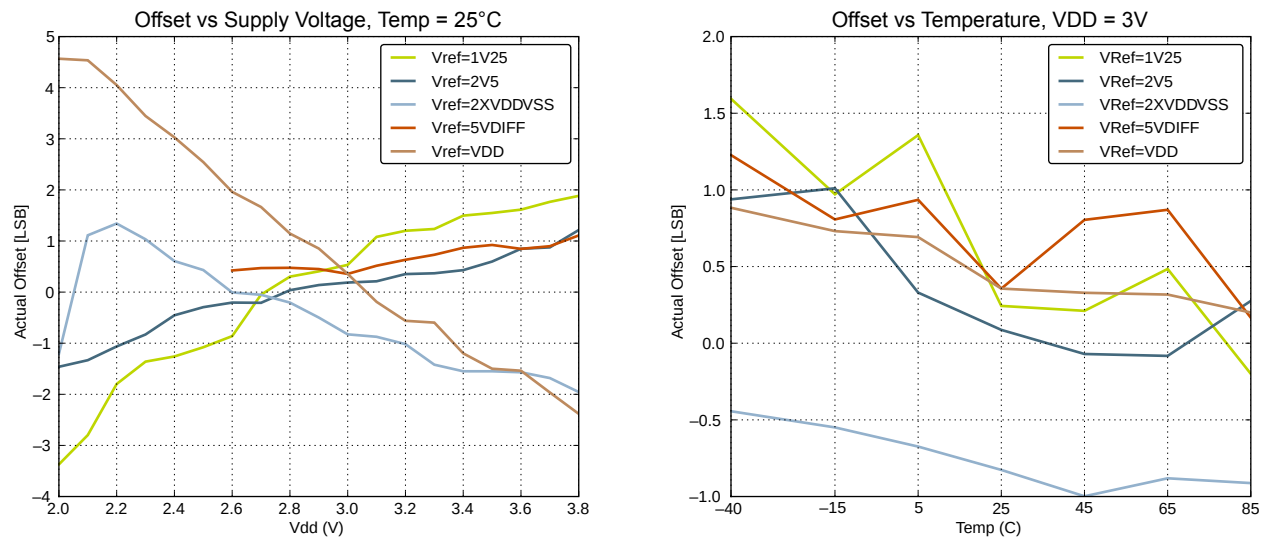


Figure 4.32. ADC Absolute Offset, Common Mode = VDD/2

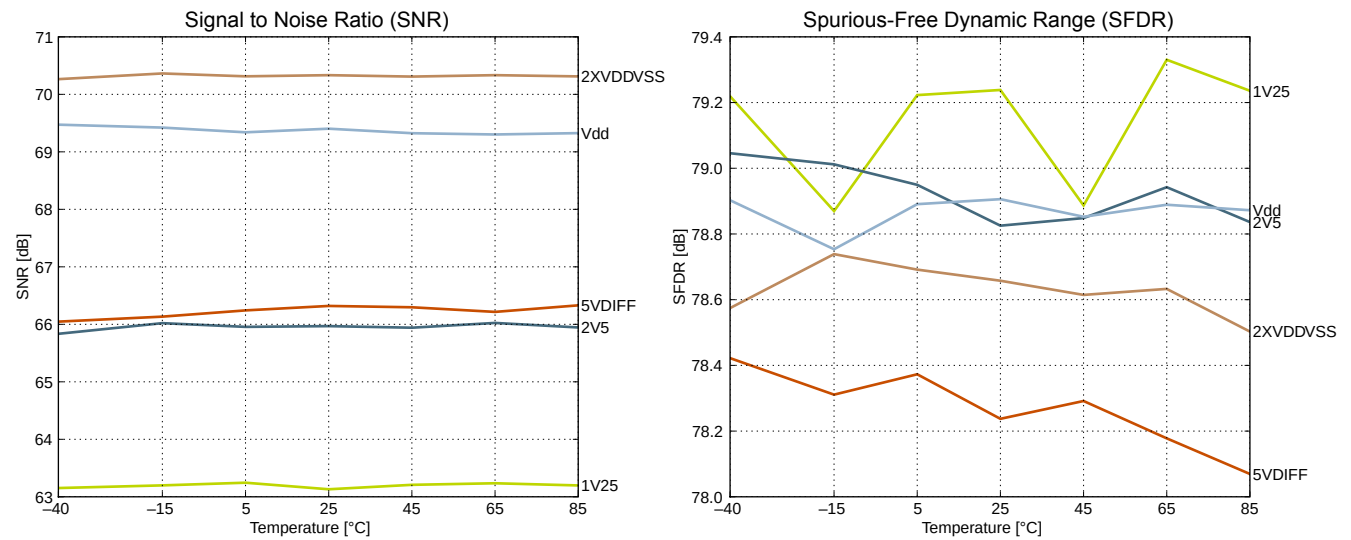


Figure 4.33. ADC Dynamic Performance vs Temperature for all ADC References, VDD = 3V

Table 4.21. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	1000 ¹	kHz
SCL clock low time	t_{LOW}	0.5	—	—	μs
SCL clock high time	t_{HIGH}	0.26	—	—	μs
SDA set-up time	$t_{SU,DAT}$	50	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26	—	—	μs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26	—	—	μs
STOP condition set-up time	$t_{SU,STO}$	0.26	—	—	μs
Bus free time between a STOP and a START condition	t_{BUF}	0.5	—	—	μs

Note:

1. For the minimum HPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32G Reference Manual.

4.16 Digital Peripherals

Table 4.22. Digital Peripherals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	7.5	—	$\mu A/MHz$
UART current	I_{UART}	UART idle current, clock enabled	—	5.63	—	$\mu A/MHz$
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	150	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	6.25	—	$\mu A/MHz$
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	8.75	—	$\mu A/MHz$
LETIMER current	$I_{LETIMER}$	LETIMER idle current, clock enabled	—	150	—	nA
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	100	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	100	—	nA
LCD current	I_{LCD}	LCD idle current, clock enabled	—	100	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	2.5	—	$\mu A/MHz$
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	5.31	—	$\mu A/MHz$
EBI current	I_{EBI}	EBI idle current, clock enabled	—	1.56	—	$\mu A/MHz$
PRS current	I_{PRS}	PRS idle current	—	2.81	—	$\mu A/MHz$
DMA current	I_{DMA}	Clock enable	—	8.12	—	$\mu A/MHz$

Note: Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32G.

Table 5.1. Device Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_1	Digital IO power supply 1.			
5	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
6	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
7	PB7	LFXTAL_P		US1_CLK #0	
8	PB8	LFXTAL_N		US1_CS #0	
9	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
10	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
11	AVDD_2	Analog power supply 2.			
12	PB13	HFXTAL_P		LEU0_TX #1	
13	PB14	HFXTAL_N		LEU0_RX #1	
14	IOVDD_3	Digital IO power supply 3.			
15	AVDD_0	Analog power supply 0.			
16	PD4	ADC0_CH4		LEU0_TX #0	
17	PD5	ADC0_CH5		LEU0_RX #0	
18	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
19	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
20	VDD_DREG	Power supply for on-chip voltage regulator.			
21	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
22	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
23	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
24	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
25	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
26	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
27	PF2				ACMP1_O #0 DBG_SWO #0
28	IOVDD_5	Digital IO power supply 5.			
29	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
30	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX

5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.5. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1				Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PA5	LCD_SEG18	TIM0_CDTI2 #0	LEU1_TX #1	
6	PA6	LCD_SEG19		LEU1_RX #1	
8	IOVDD_0	Digital IO power supply 0.			
9	PB3	LCD_SEG20	PCNT1_S0IN #1	US2_TX #1	
10	PB4	LCD_SEG21	PCNT1_S1IN #1	US2_RX #1	
11	PB5	LCD_SEG22		US2_CLK #1	
12	PB6	LCD_SEG23		US2_CS #1	
13	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
14	PC5	ACMP0_CH5	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
15	PB7	LFXTAL_P		US1_CLK #0	
16	PB8	LFXTAL_N		US1_CS #0	
17	PA12	LCD_BCAP_P	TIM2_CC0 #1		
18	PA13	LCD_BCAP_N	TIM2_CC1 #1		
19	PA14	LCD_BEXT	TIM2_CC2 #1		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
22	PB12	DAC0_OUT1	LETIM0_OUT1 #1		
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		LEU0_TX #1	
25	PB14	HFXTAL_N		LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	
31	PD3	ADC0_CH3	TIM0_CC2 #3	US1_CS #1	
32	PD4	ADC0_CH4		LEU0_TX #0	
33	PD5	ADC0_CH5		LEU0_RX #0	
34	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
35	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
36	PD8				CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG9	PE13				LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14				LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15				LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG13	PA0				LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1				LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2				LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3				LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4				LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5				LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20	PB3				LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG21	PB4				LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG22	PB5				LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG23	PB6				LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7				LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

7. LQFP100 Package Specifications

7.1 LQFP100 Package Dimensions

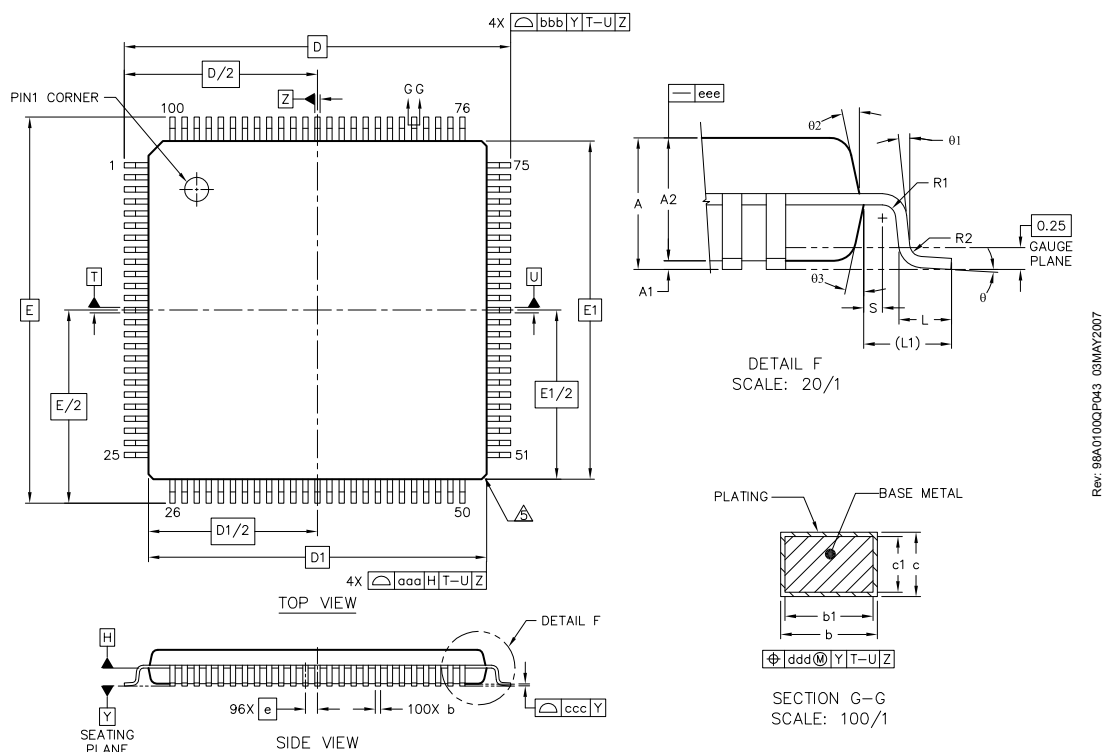


Figure 7.1. LQFP100

Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
5. Exact shape of each corner is optional.

Table 7.1. LQFP100 (Dimensions in mm)

	SYMBOL	MIN	NOM	MAX
total thickness	A	—	—	1.6
stand off	A1	0.05	—	0.15
mold thickness	A2	1.35	1.4	1.45
lead width (plating)	b	0.17	0.2	0.27
lead width	b1	0.17	—	0.23
L/F thickness (plating)	c	0.09	—	0.2
lead thickness	c1	0.09	—	0.16

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
b	0.17	0.22	0.27	S	0.20	—	—
b1	0.17	0.20	0.23	θ	0°	3.5°	7°
c	0.09	—	0.20	θ1	0°	—	—
C1	0.09	—	0.16	θ2	11°	12°	13°
D	12.0 BSC			θ3	11°	12°	13°
D1	10.0 BSC						
e	0.50 BSC						
E	12.0 BSC						
E1	10.0 BSC						
L	0.45	0.60	0.75				

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

8.2 TQFP64 PCB Layout

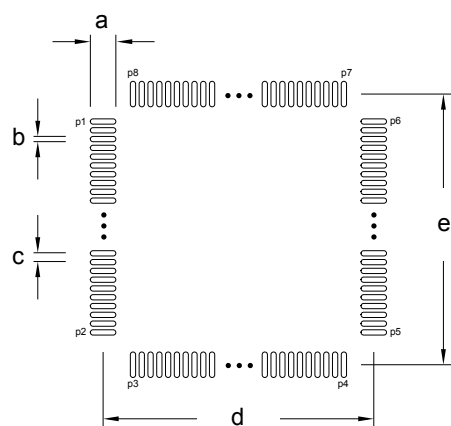


Figure 8.2. TQFP64 PCB Land Pattern

Table 8.2. TQFP64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	1.60	P1	1	P6	48
b	0.30	P2	16	P7	49
c	0.50	P3	17	P8	64
d	11.50	P4	32		
e	11.50	P5	33		

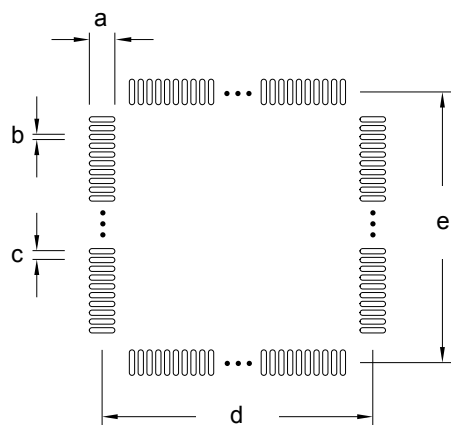


Figure 8.3. TQFP64 PCB Solder Mask

Table 8.3. TQFP64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	11.50
e	11.50

11.3 QFN32 Package Marking

In the illustration below package fields and position are shown.

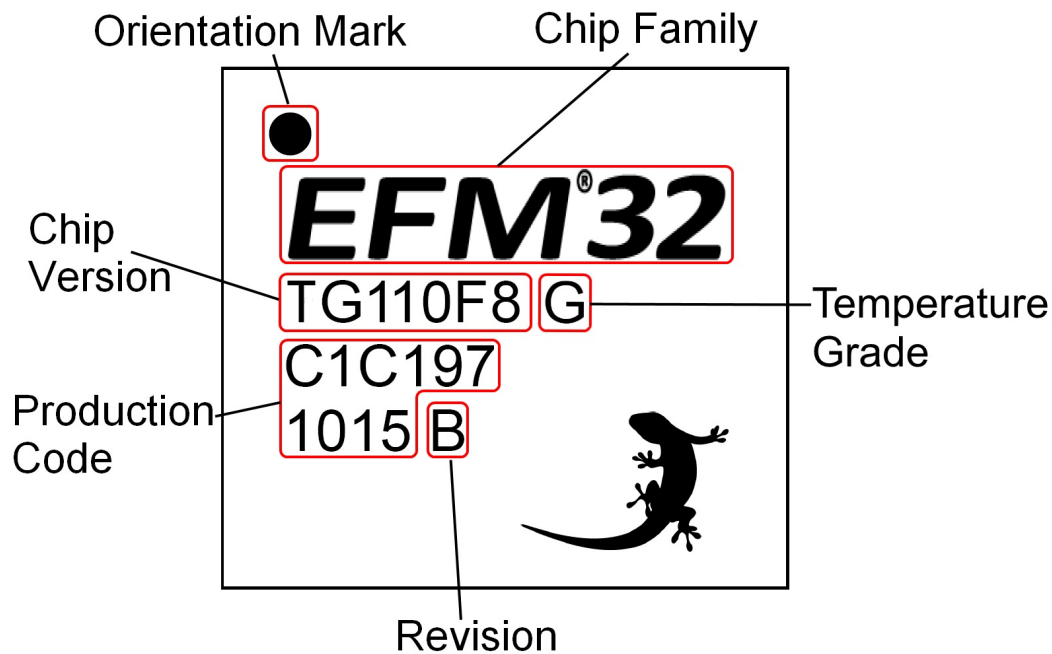


Figure 11.5. Example Chip Marking (Top View)

13. Revision History

13.1 Revision 2.10

July 19, 2017

In [4.8 General Purpose Input Output](#):

- Added missing multiply symbols.

In [4.10 Analog Digital Converter \(ADC\)](#):

- Updated average active current.
- Updated SNR.
- Updated SINAD.
- Updated SFDR.
- Renamed VREF Output Voltage to VREF Voltage.

In [4.11 Digital Analog Converter \(DAC\)](#):

- Renamed VREF Output Voltage to VREF Voltage.