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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	90
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g290f32-bga112

2. Ordering Information

The following table shows the available EFM32G devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32G200F16G-E-QFN32	16	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F32G-E-QFN32	32	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F64G-E-QFN32	64	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G210F128G-E-QFN32	128	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G222F32G-E-QFP48	32	8	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F64G-E-QFP48	64	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F128G-E-QFP48	128	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G230F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G232F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G280F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G290F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G840F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G842F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G880F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G890F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112

3.1.24 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

3.1.25 General Purpose Input/Output (GPIO)

General Purpose Input/Output (GPIO) pins are organized into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

3.1.26 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 4x40 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.2.6 EFM32G280

The features of the EFM32G280 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.6. EFM32G280 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	86 pins	Available pins are shown in Table 4.3 (p. 57)

3.2.8 EFM32G840

The features of the EFM32G840 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.8. EFM32G840 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:4], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:4], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 57)
LCD	Full configuration	LCD_SEG[23:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

3.2.11 EFM32G890

The features of the EFM32G890 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.11. EFM32G890 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 57)

0x400e0400			0xfffffffffe
0x400e0000	AES		0xe0100000
0x400cc400			0xe00fffff
0x400cc000	PRS		CM3 Peripherals
0x400ca400			0xe0000000
0x400ca000	RMU		0xdfffffff
0x400c8400			0x90000000
0x400c8000	CMU		0x8fffffff
0x400c6400			0x8c000000
0x400c6000	EMU		EBI Region 3
0x400c4000	DMA		0x8bfffffff
0x400c2000			EBI Region 2
0x400c0400	MSC		0x87fffffff
0x400c0000			EBI Region 1
0x4008a400	LCD		0x84000000
0x4008a000			0x83fffffff
0x40088400	WDOG		EBI Region 0
0x40088000			0x80000000
0x40086c00	PCNT2		0x7fffffff
0x40086800	PCNT1		0x44000000
0x40086400	PCNT0		0x43fffffff
0x40086000			Peripherals (bit-band)
0x40084800	LEUART1		0x42000000
0x40084400	LEUART0		0x41fffffff
0x40084000			0x41000000
0x40082400	LETIMER0		Peripherals
0x40082000			0x40fffffff
0x40080400	RTC		0x40000000
0x40080000			0x3fffffff
0x40010c00	TIMER2		0x22200000
0x40010800	TIMER1		0x221fffff
0x40010400	TIMER0		SRAM (bit-band)
0x40010000			0x22000000
0x4000e400	UART0		0x21fffffff
0x4000e000			0x20004000
0x4000cc00	USART2		SRAM (16 kB)
0x4000c800	USART1		(data space)
0x4000c400	USART0		0x20003fff
0x4000c000			0x20000000
0x4000a400	I2C0		0x1fffffff
0x4000a000			Code
0x40008400	EBI		
0x40008000			
0x40007000	GPIO		
0x40006000			
0x40004400	DAC0		
0x40004000			
0x40002400	ADC0		
0x40002000			
0x40001800	ACMP1		
0x40001400	ACMP0		
0x40001000			
0x40000400	VCMP		
0x40000000			0x00000000

Figure 3.3. System Address Space with Peripheral Listing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise Ratio (SNR)	SNR _{ADC}	1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	59	—	dB
		1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	67	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	63	69	—	dB
		1 MSamples/s, 12 bit, differential, 2xV _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	70	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	62	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	67	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB

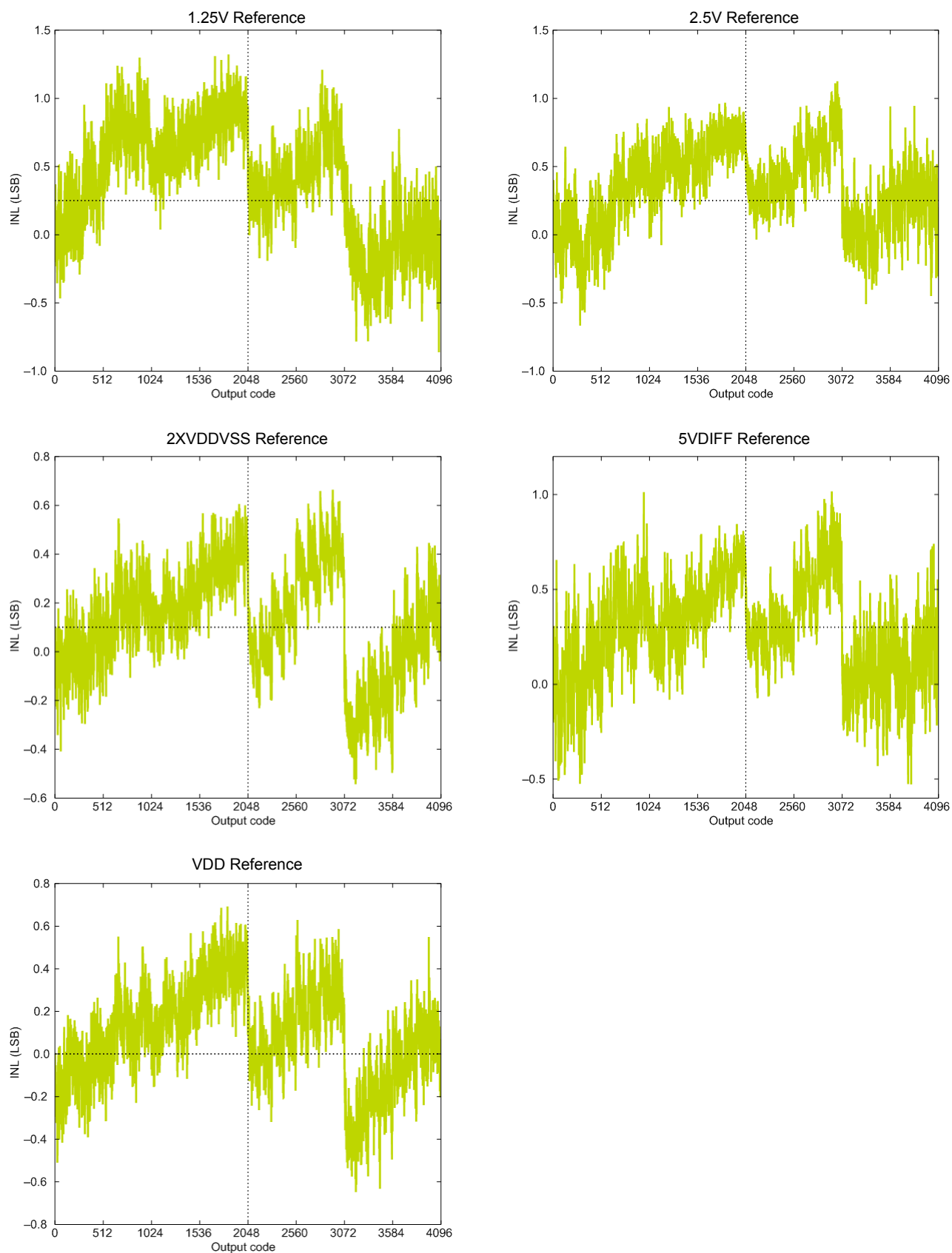


Figure 4.30. ADC Integral Linearity Error vs Code, VDD = 3V, Temp = 25°C

4.14 LCD

Table 4.18. LCD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frame rate	f_{LCDFR}		30	—	200	Hz
Number of segments supported	NUM_{SEG}		—	4×40	—	seg
LCD supply voltage range	V_{LCD}	Internal boost circuit enabled	2.0	—	3.8	V
Steady state current consumption.	I_{LCD}	Display disconnected, static mode, framerate 32 Hz, all segments on.	—	250	—	nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONE-THIRD in LCD_DISPCTRL register.	—	550	—	nA
Steady state Current contribution of internal boost.	I_{LCDBOOST}	Internal voltage boost off	—	0	—	μA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.	—	8.4	—	μA
Boost Voltage	V_{BOOST}	VBLEV of LCD_DISPCTRL register to LEVEL0	—	3.0	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL1	—	3.08	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL2	—	3.17	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL3	—	3.26	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL4	—	3.34	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL5	—	3.43	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL6	—	3.52	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL7	—	3.6	—	V

The total LCD current is given by the following equation. I_{LCDBOOST} is zero if internal boost is off.

$$I_{\text{LCDTOTAL}} = I_{\text{LCD}} + I_{\text{LCDBOOST}}$$

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LETIM0_OUT1	PD7		PF1		Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14			LEUART0 Receive input.
LEU0_TX	PD4	PB13			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		Pulse Counter PCNT0 input number 1.
TIM0_CC0	PA0	PA0			Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0		PC13		PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14		PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15		PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12				USART0 clock input / output.
US0_CS	PE13				USART0 chip select input / output.
US0_RX	PE11				USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10				USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7				USART1 clock input / output.
US1_CS	PB8				USART1 chip select input / output.
US1_RX	PC1				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0				USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG9	PE13				LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14				LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15				LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15				LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0				LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1				LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2				LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3				LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4				LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5				LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6				LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20	PB3				LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG21	PB4				LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG22	PB5				LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG23	PB6				LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14				Pulse Counter PCNT0 input number 1.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
HFX TAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		I2C0 Serial Data input / output.
LCD_BCAP_N	PA13				LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12				LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14				LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4				LCD driver common line number 0.
LCD_COM1	PE5				LCD driver common line number 1.
LCD_COM2	PE6				LCD driver common line number 2.
LCD_COM3	PE7				LCD driver common line number 3.
LCD_SEG0	PF2				LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3				LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4				LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5				LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8				LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9				LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10				LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11				LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12				LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
C3	PE10	LCD_SEG 6	EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					
C5	PD12	LCD_SEG 31	EBI_CS3 #0			
C6	PF9	LCD_SEG 27				
C7	VSS	Ground.				
C8	PF2	LCD_SEG 0	EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
C9	PE6	LCD_COM 2			US0_RX #1	
C10	PC10	ACMP1_C H2		TIM2_CC2 #2	US0_RX #2	
C11	PC11	ACMP1_C H3			US0_TX #2	
D1	PA3	LCD_SEG 16	EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
D2	PA2	LCD_SEG 15	EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0
D3	PB15					
D4	VSS	Ground.				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9	LCD_SEG 28	EBI_CS0 #0			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1
D9	PE7	LCD_COM 3			US0_TX #1	
D10	PC8	ACMP1_C H0		TIM2_CC0 #2	US0_CS #2	
D11	PC9	ACMP1_C H1		TIM2_CC1 #2	US0_CLK #2	
E1	PA6	LCD_SEG 19	EBI_AD15 #0		LEU1_RX #1	
E2	PA5	LCD_SEG 18	EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
E3	PA4	LCD_SEG 17	EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
E4	PB0	LCD_SEG 32		TIM1_CC0 #2		
E8	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MI-SO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MI-SO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MI-SO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

8.2 TQFP64 PCB Layout

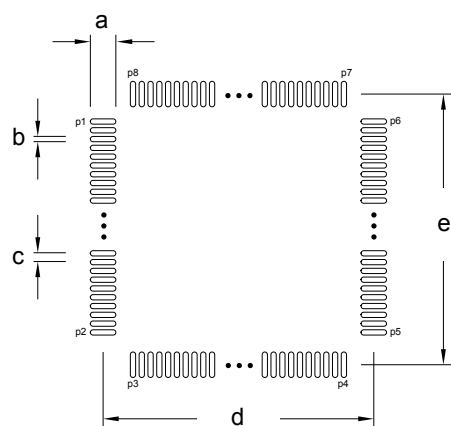


Figure 8.2. TQFP64 PCB Land Pattern

Table 8.2. TQFP64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	1.60	P1	1	P6	48
b	0.30	P2	16	P7	49
c	0.50	P3	17	P8	64
d	11.50	P4	32		
e	11.50	P5	33		

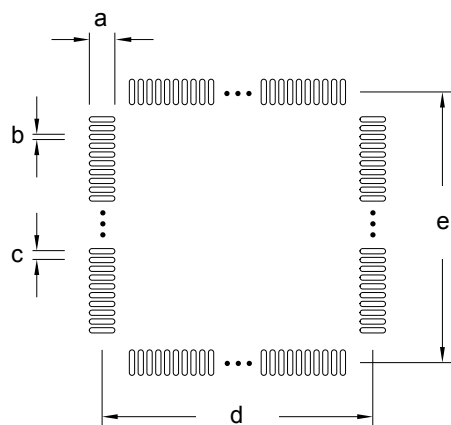


Figure 8.3. TQFP64 PCB Solder Mask

Table 8.3. TQFP64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	11.50
e	11.50

12. Chip Revision, Solder Information, Errata

12.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

12.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

12.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and on-line at: <http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

13.15 Revision 0.90

This revision applies the following devices:

- EFM32G222

Initial preliminary revision, April 14th, 2011

This revision applies the following devices:

- EFM32G232
- EFM32G842

Initial preliminary revision, June 30th, 2011

13.16 Revision 0.85

February 19th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Renamed DBG_SWV pin to DBG_SWO.

13.17 Revision 0.84

February 11th, 2010

This revision applies the following devices:

- EFM32G230
- EFM32G840

Corrected pinout tables.

13.18 Revision 0.83

January 25th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Updated errata section.

Specified flash word width in Flash Electrical Characteristics.

Added Capacitive Sense Internal Resistor values in ACMP Electrical Characteristics.

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