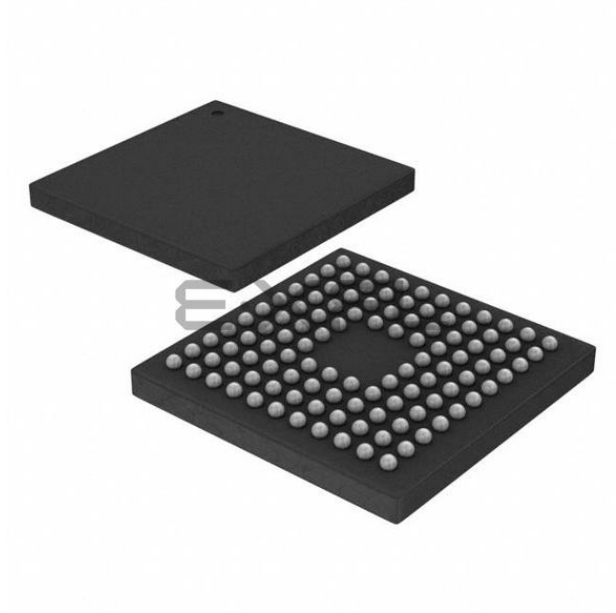

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	90
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g290f64-bga112

3.3 Memory Map

The EFM32G memory map is shown in the figure below. RAM and Flash sizes are for the largest memory configuration.

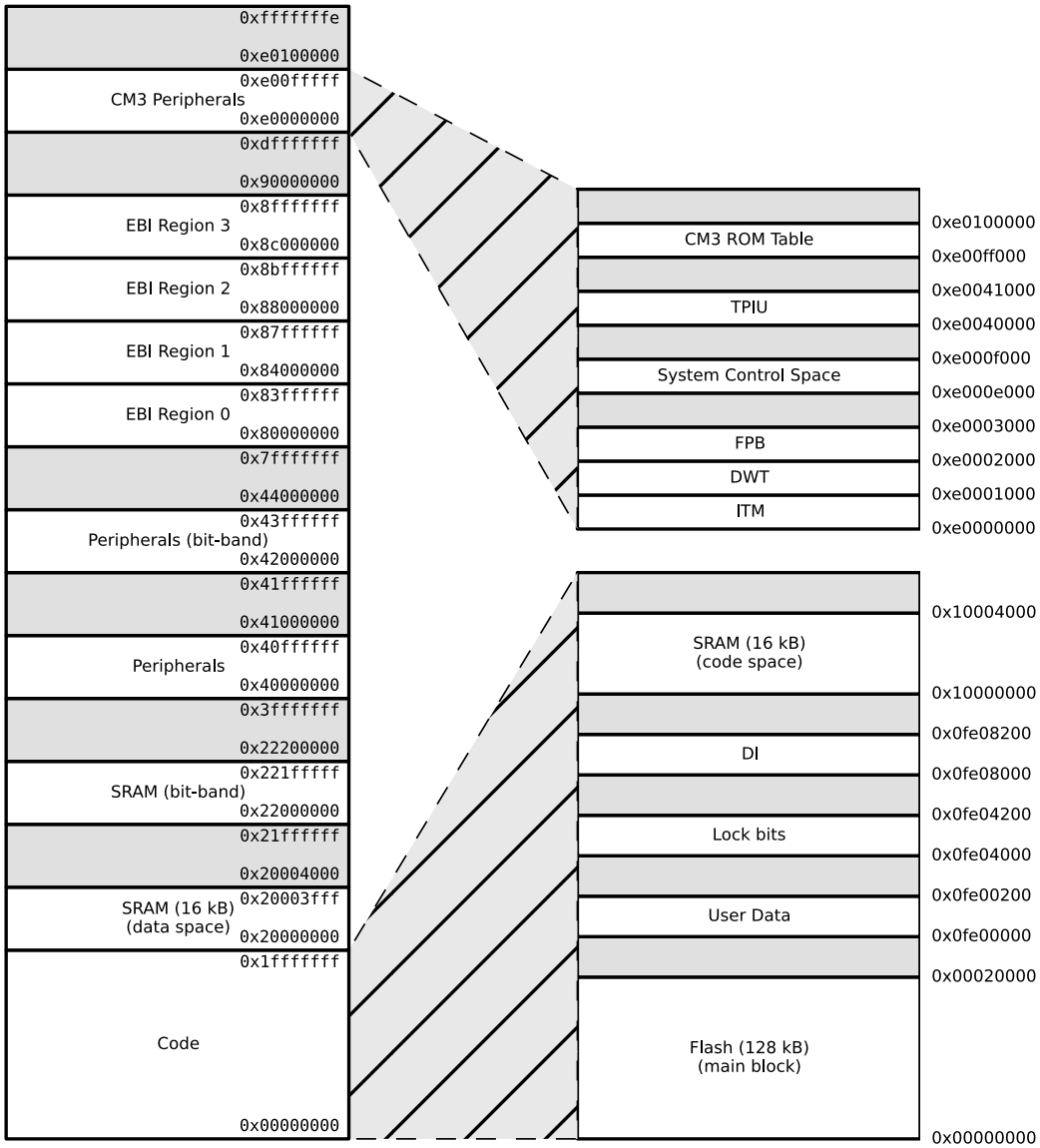


Figure 3.2. System Address Space with Core and Code Space Listing

4. Electrical Characteristics

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 4.2 General Operating Conditions on page 29, unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 4.2 General Operating Conditions on page 29, unless otherwise specified.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the following table may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 4.2 General Operating Conditions on page 29.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	150	°C
Maximum soldering temperature	T_S	Latest IPC/JEDEC J-STD-020 Standard	—	—	260	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
Voltage on any I/O pin	V_{IOPIN}		-0.3	—	V_{DD}+0.3	V
Current per I/O pin (sink)	I_{IOMAX_SINK}		—	—	100	mA
Current per I/O pin (source)	I_{IOMAX_SOURCE}		—	—	-100	mA

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}	-40	—	85	°C
Operating supply voltage	V_{DDOP}	1.98	—	3.8	V
Internal APB clock frequency	f_{APB}	—	—	32	MHz
Internal AHB clock frequency	f_{AHB}	—	—	32	MHz

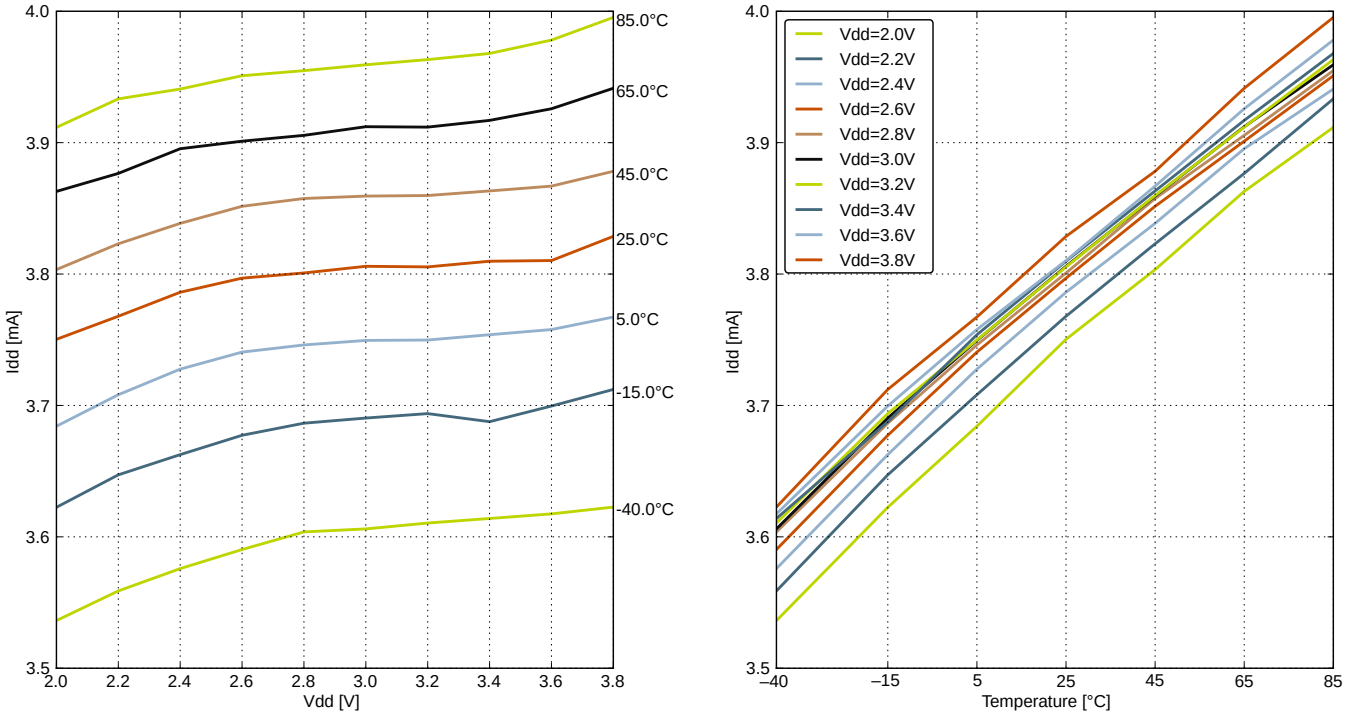


Figure 4.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz

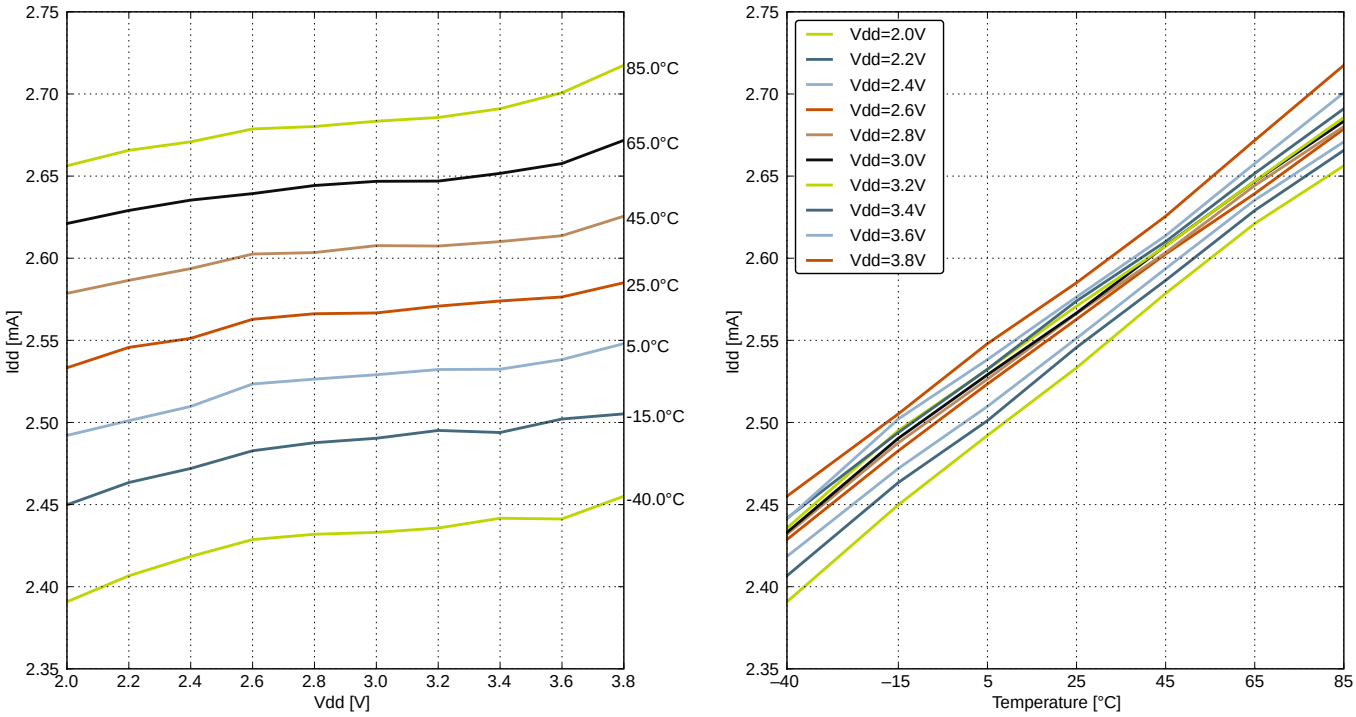


Figure 4.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

4.4.3 EM2 Current Consumption

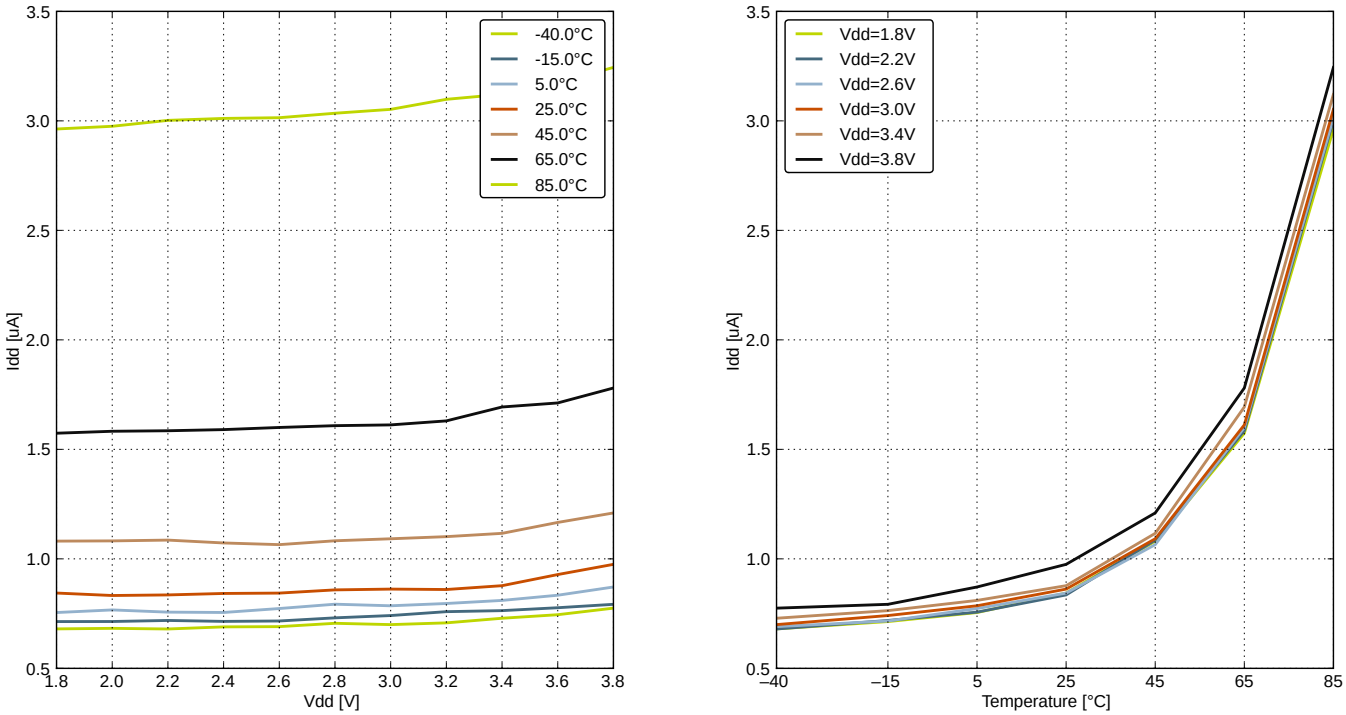


Figure 4.11. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO

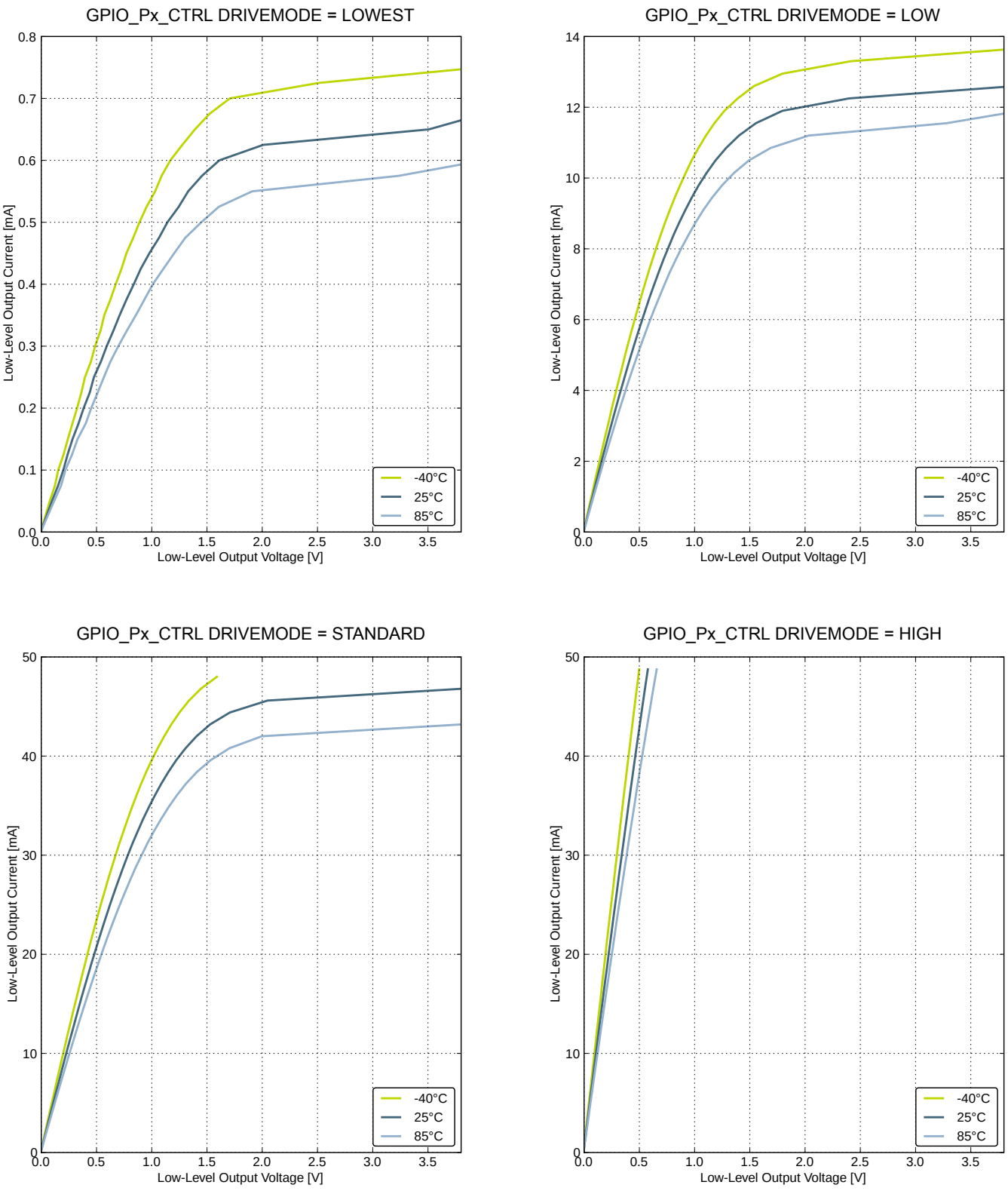


Figure 4.18. Typical Low-Level Output Current, 3.8V Supply Voltage

4.9.2 HFXO

Table 4.9. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal Frequency	f_{HFXO}		4	—	32	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 32 MHz	—	30	60	Ω
		Crystal frequency 4 MHz	—	400	1500	Ω
The transconductance of the HFXO input transistor at crystal startup	g_{mHFXO}	HFXOBOOST in CMU_CTRL equals 0b11	20	—	—	mS
Supported crystal external load range	C_{HFXOL}		5	—	25	pF
Current consumption for HFXO after startup	I_{HFXO}	4 MHz: ESR=400 Ω, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	85	—	µA
		32 MHz: ESR=30 Ω, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	165	—	µA
Startup time	t_{HFXO}	32 MHz: ESR=30 Ω, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	400	—	µs
Pulse width removed by glitch detector			1	—	4	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise Ratio (SNR)	SNR_{ADC}	1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	59	—	dB
		1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	67	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK =13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK= 13 MHz, BIASPROG =0xF4B	63	69	—	dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	70	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	62	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	67	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB

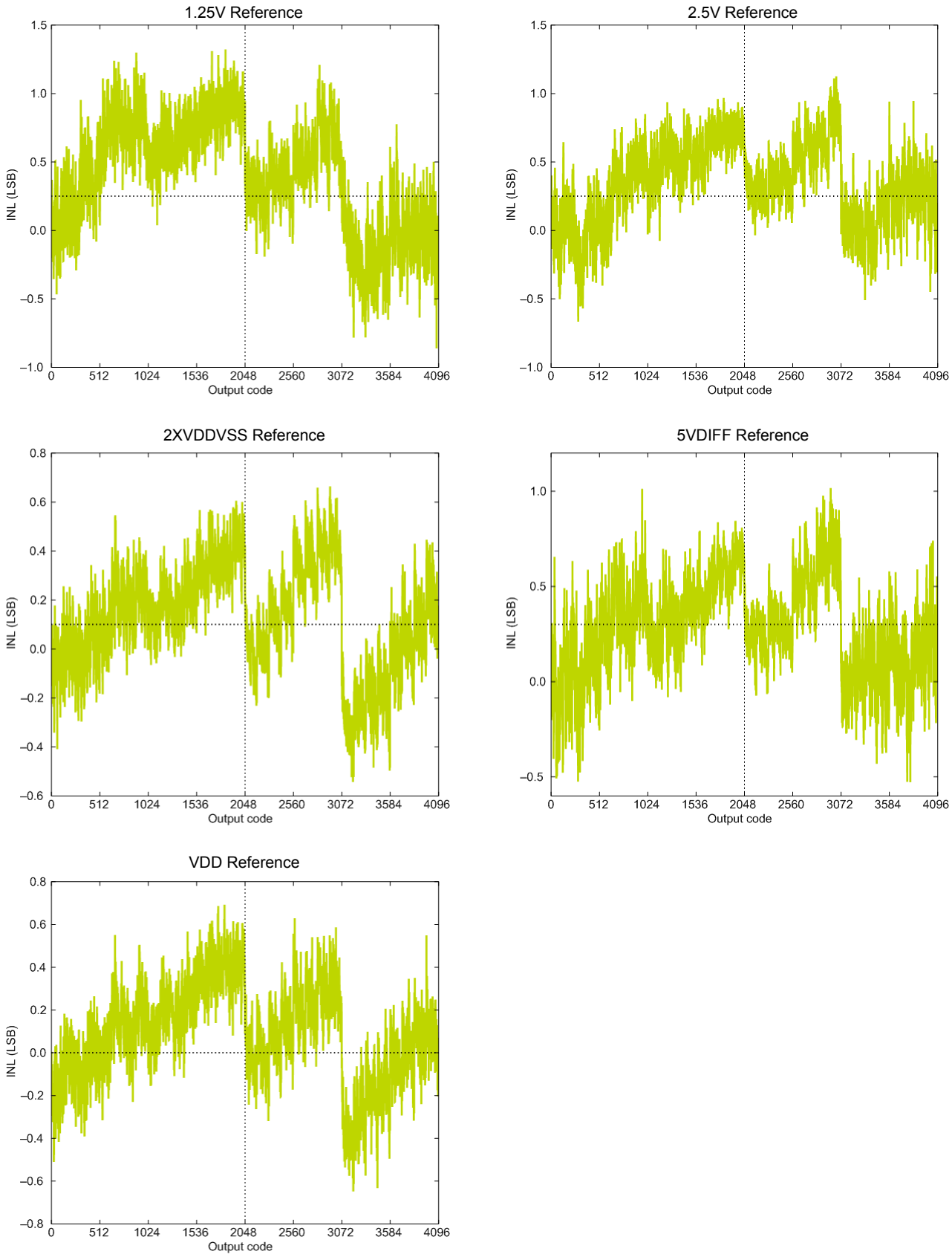


Figure 4.30. ADC Integral Linearity Error vs Code, VDD = 3V, Temp = 25°C

4.11 Digital Analog Converter (DAC)

Table 4.15. DAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage range	V_{DACOUT}	VDD voltage reference, single-ended	0	—	V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$	—	V_{DD}	V
Output common mode voltage range	V_{DACCM}		0	—	V_{DD}	V
Average active current	I_{DAC}	500 kSamples/s, 12 bit, internal 1.25 V reference, Continuous Mode	—	400[1]	650[1]	µA
		100 kSamples/s, 12 bit, internal 1.25 V reference, Sample/Hold Mode	—	200[1]	250[1]	µA
		1 kSamples/s 12 bit, internal 1.25 V reference, Sample/Off Mode	—	17[1]	25[1]	µA
Sample rate	SR_{DAC}		—	—	500	ksamples/s
DAC clock frequency	f_{DAC}	Continuous Mode	—	—	1000	kHz
		Sample/Hold Mode	—	—	250	kHz
		Sample/Off Mode	—	—	250	kHz
Clock cycles per conversion	$CYC_{DACCONV}$		—	2	—	cycles
Conversion time	$t_{DACCONV}$		2	—	—	µs
Settling time	$t_{DACSETTLE}$		—	5	—	µs
Signal-to-Noise Ratio (SNR)	SNR_{DAC}	500 kSamples/s, 12 bit, single-ended, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference	—	59	—	dB
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	59	—	dB

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
44	PC11	ACMP1_CH3		US0_TX #2	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2				ACMP1_O #0 DBG_SWO #0
52	PF3		TIM0_CDTI0 #2		
53	PF4		TIM0_CDTI1 #2		
54	PF5		TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	PE8		PCNT2_S0IN #1		
57	PE9		PCNT2_S1IN #1		
58	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX
60	PE12		TIM1_CC2 #1	US0_CLK #0	
61	PE13			US0_CS #0	ACMP0_O #0
62	PE14			LEU0_TX #2	
63	PE15			LEU0_RX #2	
64	PA15				

5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G230 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.9. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	—	—	—	—	PA10	PA8	PA8 —	—	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	—	—	PB8	PB7	—	—	—	—	—	—	—
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	—	—	—	—	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A6	PF7			TIM0_CC1 #2	U0_RX #0	
A7	PF5		EBI_REn #0	TIM0_CDTI2 #2		
A8	PF4		EBI_WEn #0	TIM0_CDTI1 #2		
A9	PE4				US0_CS #1	
A10	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
A11	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
B1	PA15		EBI_AD08 #0			
B2	PE13		EBI_AD05 #0		US0_CS #0	ACMP0_O #0
B3	PE11		EBI_AD03 #0	TIM1_CC1 #1	US0_RX #0	BOOT_RX
B4	PE8		EBI_AD00 #0	PCNT2_S0IN #1		
B5	PD11		EBI_CS2 #0			
B6	PF8			TIM0_CC2 #2		
B7	PF6			TIM0_CC0 #2	U0_TX #0	
B8	PF3		EBI_ALE #0	TIM0_CDTI0 #2		
B9	PE5				US0_CLK #1	
B10	PC12	ACMP1_CH4				CMU_CLK0 #1
B11	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
C1	PA1		EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
C2	PA0		EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	
C3	PE10		EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					
C5	PD12		EBI_CS3 #0			
C6	PF9					
C7	VSS	Ground.				
C8	PF2		EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
C9	PE6				US0_RX #1	
C10	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
C11	PC11	ACMP1_CH3			US0_TX #2	
D1	PA3		EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
D2	PA2		EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
D3	PB15					
D4	VSS	Ground.				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9	LCD_SEG 28	EBI_CS0 #0			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1
D9	PE7				US0_TX #1	
D10	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
D11	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
E1	PA6		EBI_AD15 #0		LEU1_RX #1	
E2	PA5		EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
E3	PA4		EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
E4	PB0			TIM1_CC0 #2		
E8	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1
E9	PE0			PCNT0_S0IN #1	U0_TX #1	
E10	PE1			PCNT0_S1IN #1	U0_RX #1	
E11	PE3					ACMP1_O #1
F1	PB1			TIM1_CC1 #2		
F2	PB2			TIM1_CC2 #2		
F3	PB3			PCNT1_S0IN #1	US2_TX #1	
F4	PB4			PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2					ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
G1	PB5				US2_CLK #1	
G2	PB6				US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG9	PE13				LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14				LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15				LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15				LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0				LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1				LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2				LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3				LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4				LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5				LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6				LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20	PB3				LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG21	PB4				LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG22	PB5				LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG23	PB6				LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14				Pulse Counter PCNT0 input number 1.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG7	PE11				LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12				LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13				LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14				LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15				LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15				LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0				LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1				LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2				LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3				LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4				LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5				LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6				LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20	PB3				LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG21	PB4				LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG22	PB5				LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG23	PB6				LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG24	PF6				LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG25	PF7				LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG26	PF8				LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG27	PF9				LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG28	PD9				LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG29	PD10				LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
E9	PE0			PCNT0_S0IN #1	U0_TX #1	
E10	PE1			PCNT0_S1IN #1	U0_RX #1	
E11	PE3					ACMP1_O #1
F1	PB1	LCD_SEG 33		TIM1_CC1 #2		
F2	PB2	LCD_SEG 34		TIM1_CC2 #2		
F3	PB3	LCD_SEG 20		PCNT1_S0IN #1	US2_TX #1	
F4	PB4	LCD_SEG 21		PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2					ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
G1	PB5	LCD_SEG 22			US2_CLK #1	
G2	PB6	LCD_SEG 23			US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				
G10	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
G11	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
H1	PC0	ACMP0_CH0		PCNT0_S0IN #2	US1_TX #0	
H2	PC2	ACMP0_CH2			US2_TX #0	
H3	PD14				I2C0_SDA #3	
H4	PA7	LCD_SEG 35				
H5	PA8	LCD_SEG 36		TIM2_CC0 #0		
H6	VSS	Ground.				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8					CMU_CLK1 #1

11.3 QFN32 Package Marking

In the illustration below package fields and position are shown.

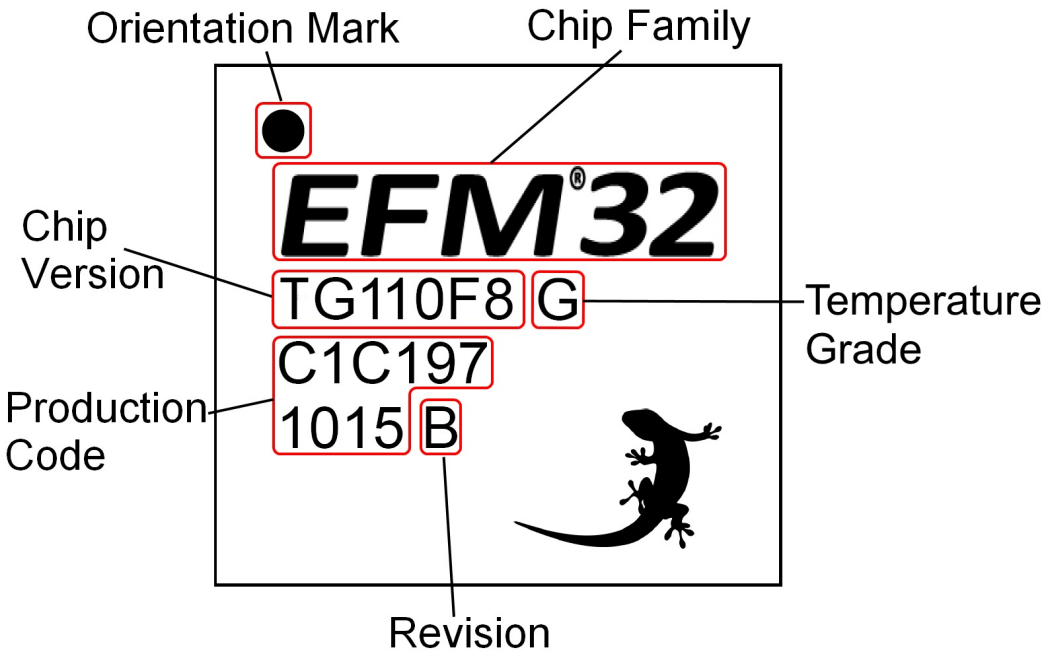


Figure 11.5. Example Chip Marking (Top View)

Corrected pin number for symbol P3 in Table 11.2 QFN32 PCB Land Pattern Dimensions (Dimensions in mm) on page 191.

Updated package marking figures to include temperature grade.

13.3 Revision 1.90

May 22nd, 2015

For devices with an ADC, Added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Updated HFRCO table in the Electrical Characteristics section.

Updated EM0, EM2, EM3, and EM4 maximum current specifications in the Electrical Characteristics section.

Updated the Output Low Voltage maximum for sinking 20 mA with VDD = 3.0 V in the Electrical Characteristics section.

Updated the Input Leakage Current maximum in the Electrical Characteristics section.

Updated the minimum and maximum frequency specifications for the LFRCO, HFRCO, and AUXHFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Added some minimum ADC SNR, SNDR, and SFDR specifications in the Electrical Characteristics section.

Added some minimum and maximum ADC offset voltage, DNL, and INL specifications in the Electrical Characteristics section.

Added maximum DAC current specifications in the Electrical Characteristics section.

Added maximum ACMP current and maximum and minimum offset voltage specifications in the Electrical Characteristics section.

Added maximum VCMP current and updated typical VCMP current specifications in the Electrical Characteristics section.

Updated references to energyAware Designer to Configurator.

13.4 Revision 1.80

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated current consumption.

Updated transition between energy modes.

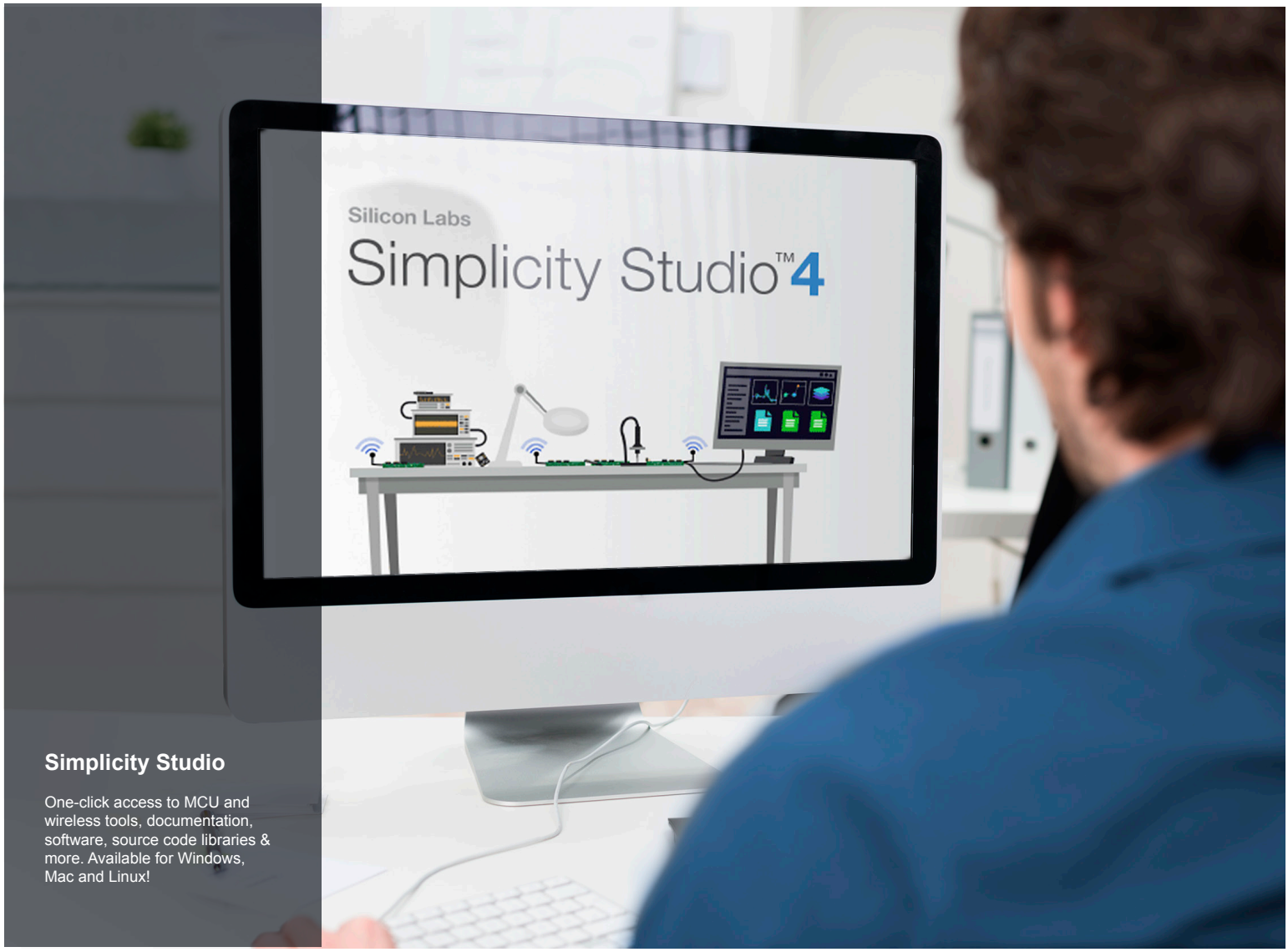
Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

For devices with an ACMP, updated ACMP data.



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