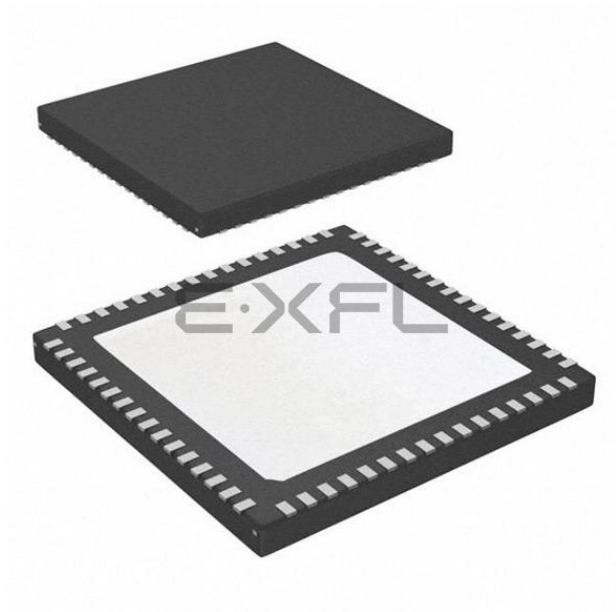
# Silicon Labs - EFM32G840F128G-E-QFN64R Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 56 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32g840f128g-e-qfn64r |

# 1. Feature List

- ARM Cortex-M3 CPU platform
  - High Performance 32-bit processor @ up to 32 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
  - SysTick System Timer
- Flexible Energy Management System
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 45 µA/MHz @ 3 V Sleep Mode
  - 180 µA/MHz @ 3 V Run Mode, with code executed from flash
- 128/64/32 KB Flash
- 16/8 KB RAM
- Up to 90 General Purpose I/O pins
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- 8 Channel DMA Controller
- 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- Hardware AES with 128/256-bit keys in 54/75 cycles
- Timers/Counters
  - 3 × 16-bit Timer/Counter
    - 3×3 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 16-bit Low Energy Timer
  - 1× 24-bit Real-Time Counter
  - 3× 8-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- Integrated LCD Controller for up to 4×40 segments
  - Voltage boost, adjustable contrast and autonomous animation
- External Bus Interface for up to 4x64 MB of external memory mapped space
  - TFT Controller with Direct Drive
- Communication interfaces
  - Up to 3× Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
    - Triple buffered full/half-duplex operation
  - 1× Universal Asynchronous Receiver/Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - $I^2C$ Interface with SMBus support
    - Address recognition in Stop Mode
- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 8 single-ended channels/4 differential channels
    - On-chip temperature sensor
  - 12-bit 500 ksamples/s Digital to Analog Converter
    - 2 single-ended channels/1 differential channel
  - 2× Analog Comparator
    - Capacitive sensing with up to 16 inputs

# 3. System Overview

## 3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32G devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32G Reference Manual.

The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

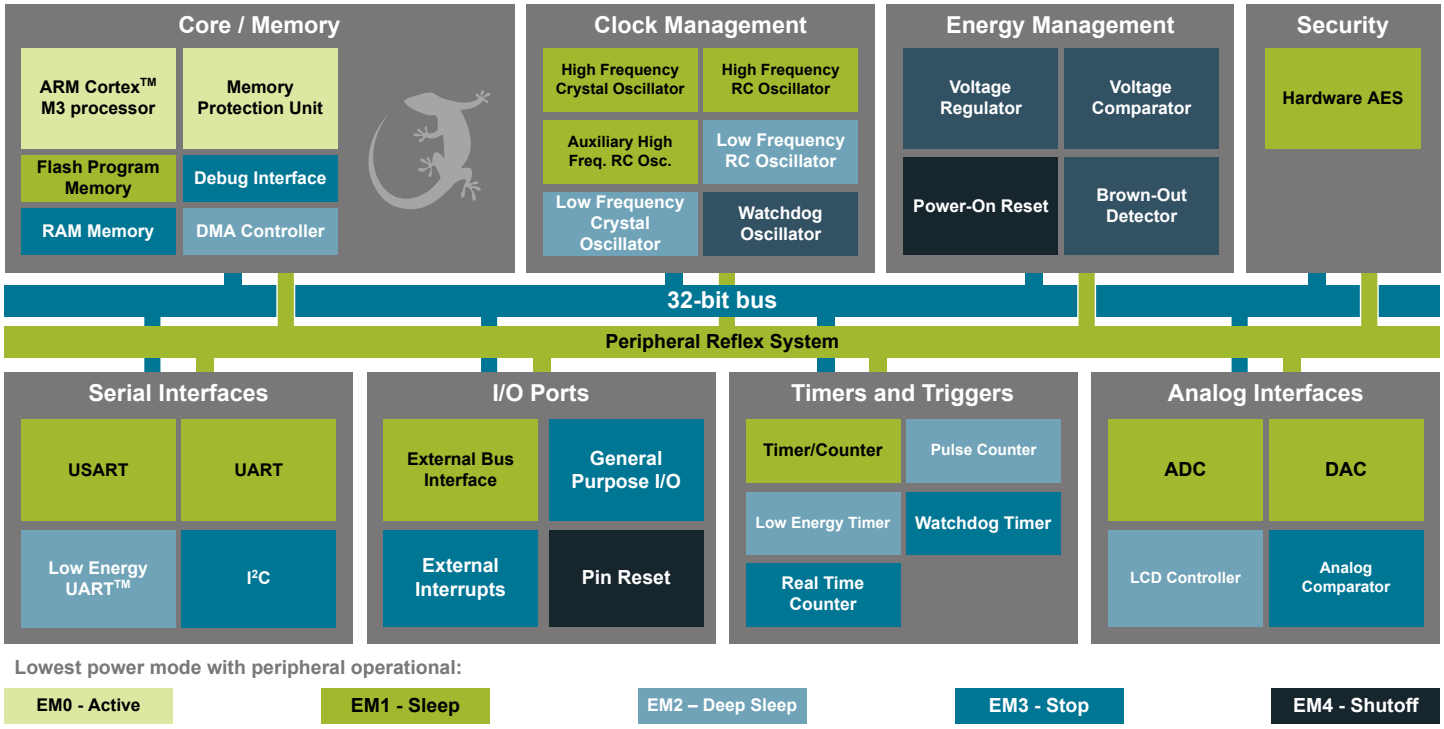


**Figure 3.1. Block Diagram**

### 3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32G Reference Manual.

### 3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

### 3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 4.4.1 EM0 Current Consumption

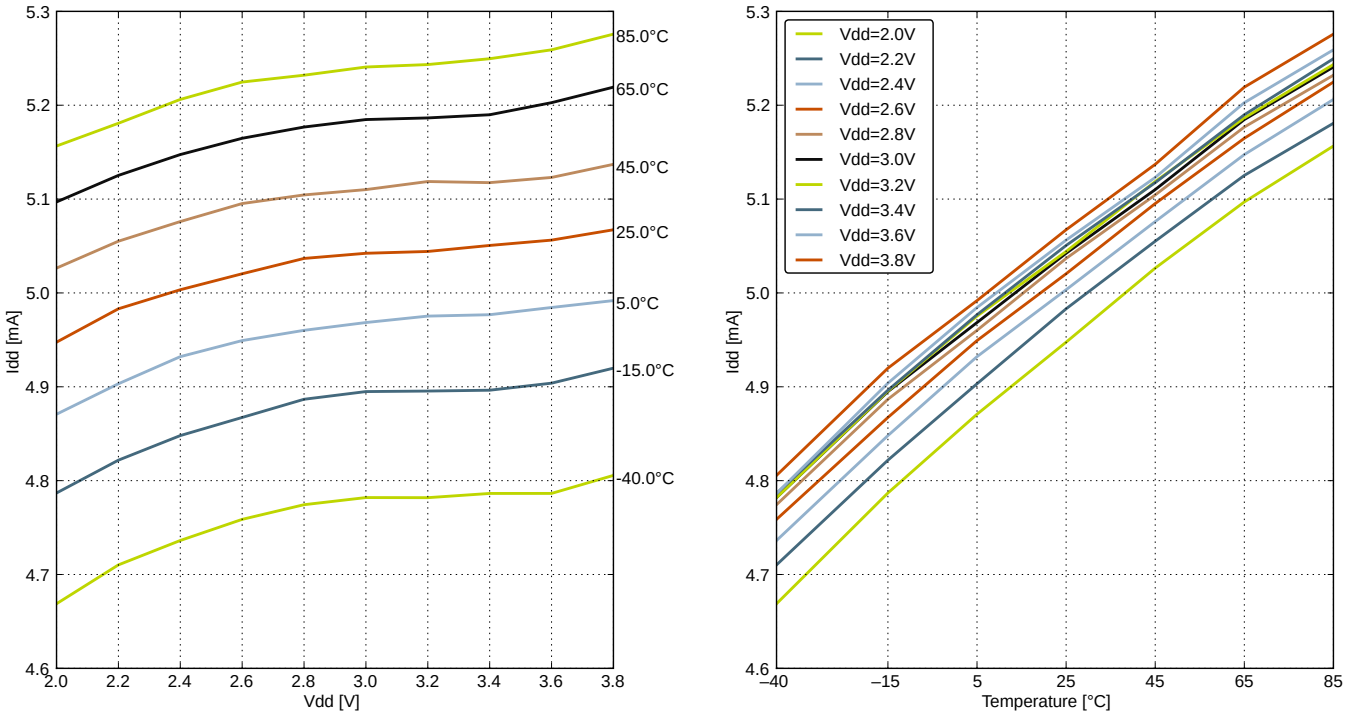


**Figure 4.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28 MHz**

## 4.7 Flash

**Table 4.6. Flash**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Flash erase cycles before failure | $EC_{FLASH}$ | | 20000 | — | — | cycles |
| Flash data retention | $RET_{FLASH}$ | $T_{AMB}$<150 ºC | 10000 | — | — | h |
| | | $T_{AMB}$<85 ºC | 10 | — | — | years |
| | | $T_{AMB}$<70 ºC | 20 | — | — | years |
| Word (32-bit) programming time | $t_{W\_PROG}$ | | 20 | — | — | µs |
| Page erase time[2] | $t_{P\_ERASE}$ | | 20.7 | 22.0 | 24.8 | ms |
| Device erase time[3] | $t_{D\_ERASE}$ | | 41.8 | 45.0 | 49.2 | ms |
| Erase current | $I_{ERASE}$ | | — | — | 7[1] | mA |
| Write current | $I_{WRITE}$ | | — | — | 7[1] | mA |
| Supply voltage during flash erase and write | $V_{FLASH}$ | | 1.98 | — | 3.8 | V |

**Note:**

1. Measured at 25 °C.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.

### 4.9.2 HFXO

**Table 4.9. HFXO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supported nominal crystal Frequency | $f_{HFXO}$ | | 4 | — | 32 | MHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{HFXO}$ | Crystal frequency 32 MHz | — | 30 | 60 | Ω |
| | | Crystal frequency 4 MHz | — | 400 | 1500 | Ω |
| The transconductance of the HFXO input transistor at crystal startup | $g_{mHFXO}$ | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | — | — | mS |
| Supported crystal external load range | $C_{HFXOL}$ | | 5 | — | 25 | pF |
| Current consumption for HFXO after startup | $I_{HFXO}$ | 4 MHz: ESR=400 Ω, $C_L$=20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 85 | — | µA |
| | | 32 MHz: ESR=30 Ω, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 165 | — | µA |
| Startup time | $t_{HFXO}$ | 32 MHz: ESR=30 Ω, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 400 | — | µs |
| Pulse width removed by glitch detector | | | 1 | — | 4 | ns |

## 4.10 Analog Digital Converter (ADC)

**Table 4.14. ADC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{ADCIN}$ | Single-ended | 0 | — | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | — | $V_{REF}/2$ | V |
| Input range of external reference voltage, single-ended and differential | $V_{ADCREFIN}$ | | 1.25 | — | $V_{DD}$ | V |
| Input range of external negative reference voltage on channel 7 | $V_{ADCREFIN\_CH7}$ | See $V_{ADCREFIN}$ | 0 | — | $V_{DD}$ - 1.1 | V |
| Input range of external positive reference voltage on channel 6 | $V_{ADCREFIN\_CH6}$ | See $V_{ADCREFIN}$ | 0.625 | — | $V_{DD}$ | V |
| Common mode input range | $V_{ADCCMIN}$ | | 0 | — | $V_{DD}$ | V |
| Input current | $I_{ADCIN}$ | 2 pF sampling capacitors | — | <100 | — | nA |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | | — | 65 | — | dB |
| Average active current | $I_{ADC}$ | 1 Msamples/s, 12 bit, external reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 735[1] | — | µA |
| | | 1 Msamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 760[1] | — | µA |
| | | 500 Ksamples/s, 12 bit, external reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 346[1] | — | µA |
| | | 500 Ksamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 354[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 00b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 52[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 01b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 50[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 10b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 54[1] | — | µA |
| Input capacitance | $C_{ADCIN}$ | | — | 2 | — | pF |
| Input ON resistance | $R_{ADCIN}$ | | 1 | — | — | MΩ |
| Input RC filter resistance | $R_{ADCFILT}$ | | — | 10 | — | kΩ |
| Input RC filter/decoupling capacitance | $C_{ADCFILT}$ | | — | 250 | — | fF |
| Input bias current | $I_{ADCBIASIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input offset current | $I_{ADCOFFSETIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| ADC Clock Frequency | $f_{ADCCLK}$ | BIASPROG=0x747 | — | — | 7 | MHz |
| | | BIASPROG=0xF4B | — | — | 13 | MHz |
| Conversion time | $t_{ADCCONV}$ | 6 bit | 7 | — | — | ADCCLK Cycles |
| | | 8 bit | 11 | — | — | ADCCLK Cycles |
| | | 12 bit | 13 | — | — | ADCCLK Cycles |
| Acquisition time | $t_{ADCACQ}$ | Programmable | 1 | — | 256 | ADCCLK Cycles |
| Required acquisition time for VDD/3 reference | $t_{ADCACQVDD3}$ | | 2 | — | — | µs |
| Startup time of reference generator and ADC core | $t_{ADCSTART}$ | NORMAL mode | — | 5 | — | µs |
| | | KEEPADCWARM mode | — | 1 | — | µs |

**Table 5.1. Device Pinout**

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_1 | Digital IO power supply 1. | | | |
| 5 | PC0 | ACMP0_CH0 | PCNT0_S0IN #2 | US1_TX #0 | |
| 6 | PC1 | ACMP0_CH1 | PCNT0_S1IN #2 | US1_RX #0 | |
| 7 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 8 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 9 | RESETn | Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 10 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 11 | AVDD_2 | Analog power supply 2. | | | |
| 12 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 13 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 14 | IOVDD_3 | Digital IO power supply 3. | | | |
| 15 | AVDD_0 | Analog power supply 0. | | | |
| 16 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 17 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 18 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 19 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 20 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 21 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 22 | PC13 | ACMP1_CH5 | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 23 | PC14 | ACMP1_CH6 | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | | |
| 24 | PC15 | ACMP1_CH7 | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | | DBG_SWO #1 |
| 25 | PF0 | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |
| 26 | PF1 | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 27 | PF2 | | | | ACMP1_O #0 DBG_SWO #0 |
| 28 | IOVDD_5 | Digital IO power supply 5. | | | |
| 29 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 30 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DAC0_OUT1 | PB12 | | | | Digital to Analog Converter DAC0 output channel number 1. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |

| TQFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 6 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PC0 | ACMP0_CH0 | PCNT0_S0IN #1 | US1_TX #1 | |
| 10 | PC1 | ACMP0_CH1 | PCNT0_S1IN #1 | US1_RX #1 | |
| 11 | PC2 | ACMP0_CH2 | | US1_CLK #1 | |
| 12 | PC3 | ACMP0_CH3 | | US1_CS #1 | |
| 13 | PC4 | ACMP0_CH4 | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| 14 | PC5 | ACMP0_CH5 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| 15 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 17 | PA8 | | TIM2_CC0 #0 | | |
| 18 | PA9 | | TIM2_CC1 #0 | | |
| 19 | PA10 | | TIM2_CC2 #0 | | |
| 20 | RESETn | Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 35 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | |

## 5.6 EFM32G290 (BGA112)

### 5.6.1 Pinout

The EFM32G290 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

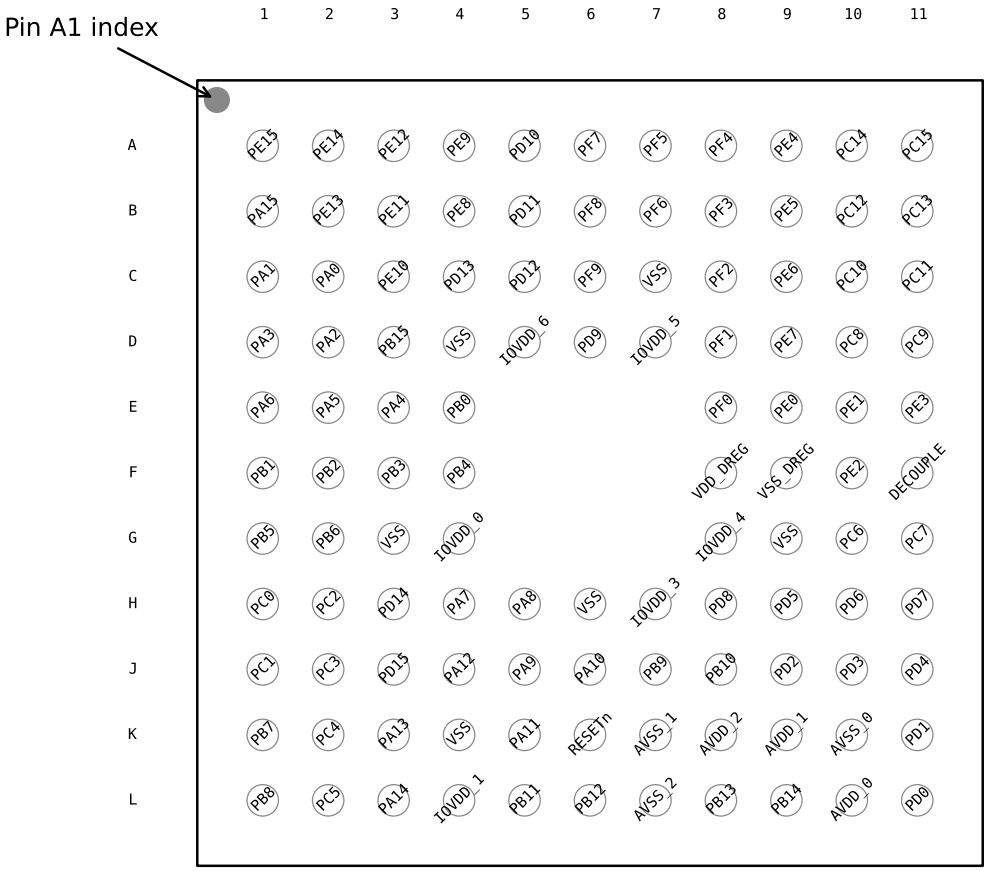


**Figure 5.6. EFM32G280 Pinout (top view, not to scale)**

**Table 5.16. Device Pinout**

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | | EBI_AD07 #0 | | LEU0_RX #2 | |
| A2 | PE14 | | EBI_AD06 #0 | | LEU0_TX #2 | |
| A3 | PE12 | | EBI_AD04 #0 | TIM1_CC2 #1 | US0_CLK #0 | |
| A4 | PE9 | | EBI_AD01 #0 | PCNT2_S1IN #1 | | |
| A5 | PD10 | | EBI_CS1 #0 | | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| G10 | PC6 | ACMP0_CH6 | | | LEU1_TX #0<br>I2C0_SDA #2 | |
| G11 | PC7 | ACMP0_CH7 | | | LEU1_RX #0<br>I2C0_SCL #2 | |
| H1 | PC0 | ACMP0_CH0 | | PCNT0_S0IN #2 | US1_TX #0 | |
| H2 | PC2 | ACMP0_CH2 | | | US2_TX #0 | |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | | | | | |
| H5 | PA8 | | | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | | | | | CMU_CLK1 #1 |
| H9 | PD5 | ADC0_CH5 | | | LEU0_RX #0 | |
| H10 | PD6 | ADC0_CH6 | | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| H11 | PD7 | ADC0_CH7 | | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| J1 | PC1 | ACMP0_CH1 | | PCNT0_S1IN #2 | US1_RX #0 | |
| J2 | PC3 | ACMP0_CH3 | | | US2_RX #0 | |
| J3 | PD15 | | | | I2C0_SCL #3 | |
| J4 | PA12 | | | TIM2_CC0 #1 | | |
| J5 | PA9 | | | TIM2_CC1 #0 | | |
| J6 | PA10 | | | TIM2_CC2 #0 | | |
| J7 | PB9 | | | | | |
| J8 | PB10 | | | | | |
| J9 | PD2 | ADC0_CH2 | | TIM0_CC1 #3 | US1_CLK #1 | |
| J10 | PD3 | ADC0_CH3 | | TIM0_CC2 #3 | US1_CS #1 | |
| J11 | PD4 | ADC0_CH4 | | | LEU0_TX #0 | |
| K1 | PB7 | LFXTAL_P | | | US1_CLK #0 | |
| K2 | PC4 | ACMP0_CH4 | | LETIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0 | |
| K3 | PA13 | | | TIM2_CC1 #1 | | |
| K4 | VSS | Ground. | | | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| K5 | PA11 | | | | | |
| K6 | RESETn | Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |
| K11 | PD1 | ADC0_CH 1 | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| L1 | PB8 | LFXTAL_N | | | US1_CS #0 | |
| L2 | PC5 | ACMP0_C H5 | | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| L3 | PA14 | | | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OU T0 | | LETIM0_OUT0 #1 | | |
| L6 | PB12 | DAC0_OU T1 | | LETIM0_OUT1 #1 | | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_ P | | | LEU0_TX #1 | |
| L9 | PB14 | HFXTAL_ N | | | LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |
| L11 | PD0 | ADC0_CH 0 | | PCNT2_S0IN #0 | US1_TX #1 | |

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |

### 5.8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.23. Alternate functionality overview**

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| E9 | PE0 | | | PCNT0_S0IN #1 | U0_TX #1 | |
| E10 | PE1 | | | PCNT0_S1IN #1 | U0_RX #1 | |
| E11 | PE3 | | | | | ACMP1_O #1 |
| F1 | PB1 | LCD_SEG 33 | | TIM1_CC1 #2 | | |
| F2 | PB2 | LCD_SEG 34 | | TIM1_CC2 #2 | | |
| F3 | PB3 | LCD_SEG 20 | | PCNT1_S0IN #1 | US2_TX #1 | |
| F4 | PB4 | LCD_SEG 21 | | PCNT1_S1IN #1 | US2_RX #1 | |
| F8 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| F9 | VSS_DREG | Ground for on-chip voltage regulator. | | | | |
| F10 | PE2 | | | | | ACMP0_O #1 |
| F11 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| G1 | PB5 | LCD_SEG 22 | | | US2_CLK #1 | |
| G2 | PB6 | LCD_SEG 23 | | | US2_CS #1 | |
| G3 | VSS | Ground. | | | | |
| G4 | IOVDD_0 | Digital IO power supply 0. | | | | |
| G8 | IOVDD_4 | Digital IO power supply 4. | | | | |
| G9 | VSS | Ground. | | | | |
| G10 | PC6 | ACMP0_CH6 | | | LEU1_TX #0<br>I2C0_SDA #2 | |
| G11 | PC7 | ACMP0_CH7 | | | LEU1_RX #0<br>I2C0_SCL #2 | |
| H1 | PC0 | ACMP0_CH0 | | PCNT0_S0IN #2 | US1_TX #0 | |
| H2 | PC2 | ACMP0_CH2 | | | US2_TX #0 | |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | LCD_SEG 35 | | | | |
| H5 | PA8 | LCD_SEG 36 | | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | | | | | CMU_CLK1 #1 |

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| EBI_ARDY | PF2 | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_CS0 | PD9 | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_REn | PF5 | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_WEn | PF4 | | | | External Bus Interface (EBI) Write Enable output. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |

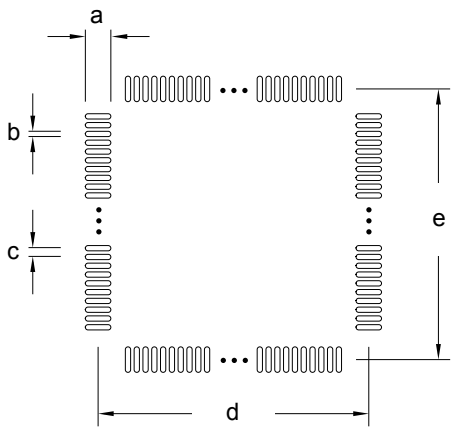


**Figure 8.4. TQFP64 PCB Stencil Design**

**Table 8.4. TQFP64 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 1.50 |
| b | 0.20 |
| c | 0.50 |
| d | 11.50 |
| e | 11.50 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 10.2 QFN64 PCB Layout

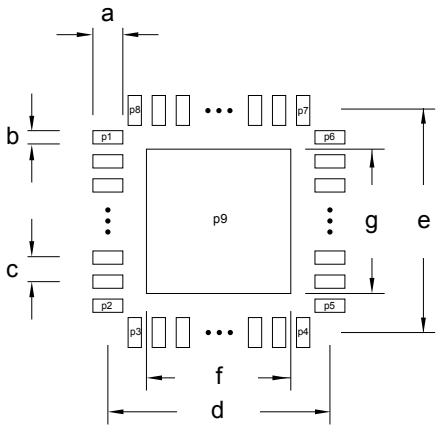


**Figure 10.2. QFN64 PCB Land Pattern**

**Table 10.2. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 0.85 | P1 | 1 | P8 | 64 |
| b | 0.30 | P2 | 16 | P9 | 65 |
| c | 0.50 | P3 | 17 | | |
| d | 8.90 | P4 | 32 | | |
| e | 8.90 | P5 | 33 | | |
| f | 7.20 | P6 | 48 | | |
| g | 7.20 | P7 | 49 | | |

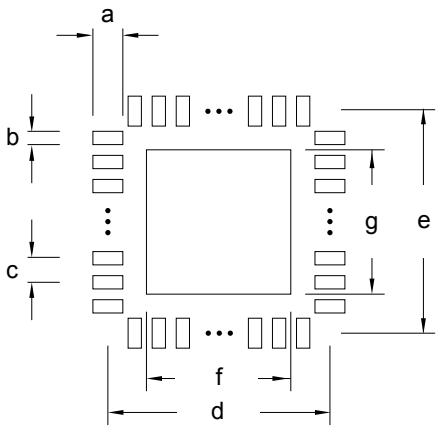


**Figure 10.3. QFN64 PCB Solder Mask**

**Table 10.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|---|---|---|---|
| a | 0.97 | e | 8.90 |
| b | 0.42 | f | 7.32 |
| c | 0.50 | g | 7.32 |

### 10.3 QFN64 Package Marking

In the illustration below package fields and position are shown.

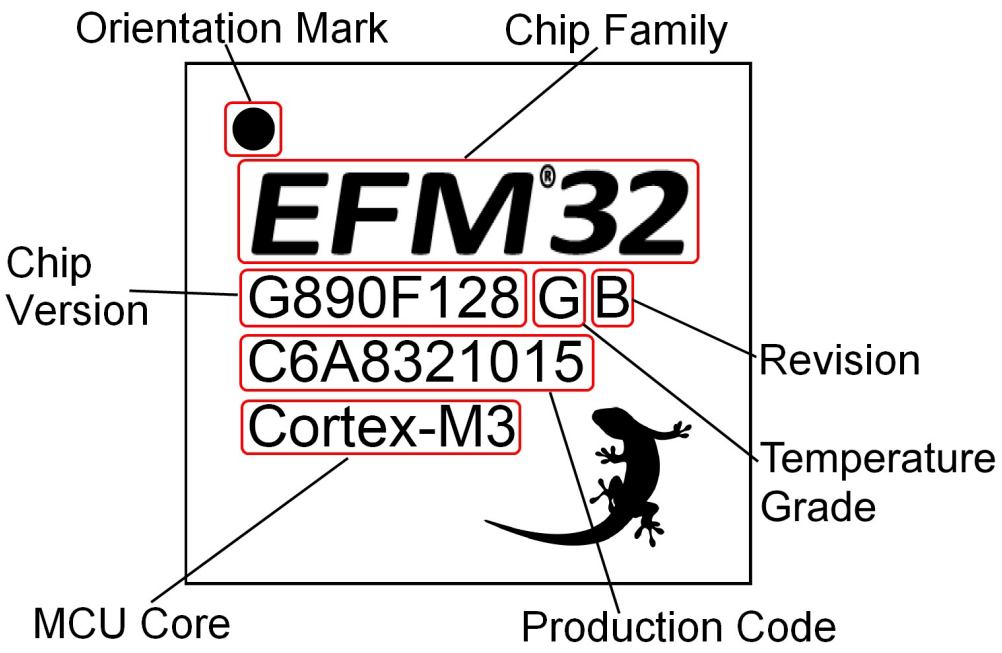


**Figure 10.5. Example Chip Marking (Top View)**