# Silicon Labs - EFM32G842F128-QFP64T Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32g842f128-qfp64t |

### 3.2.3 EFM32G222

The features of the EFM32G222 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

**Table 3.3. EFM32G222 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[1] |
| AES | Full configuration | NA |
| GPIO | 37 pins | Available pins are shown in Table 4.3 (p. 57) |

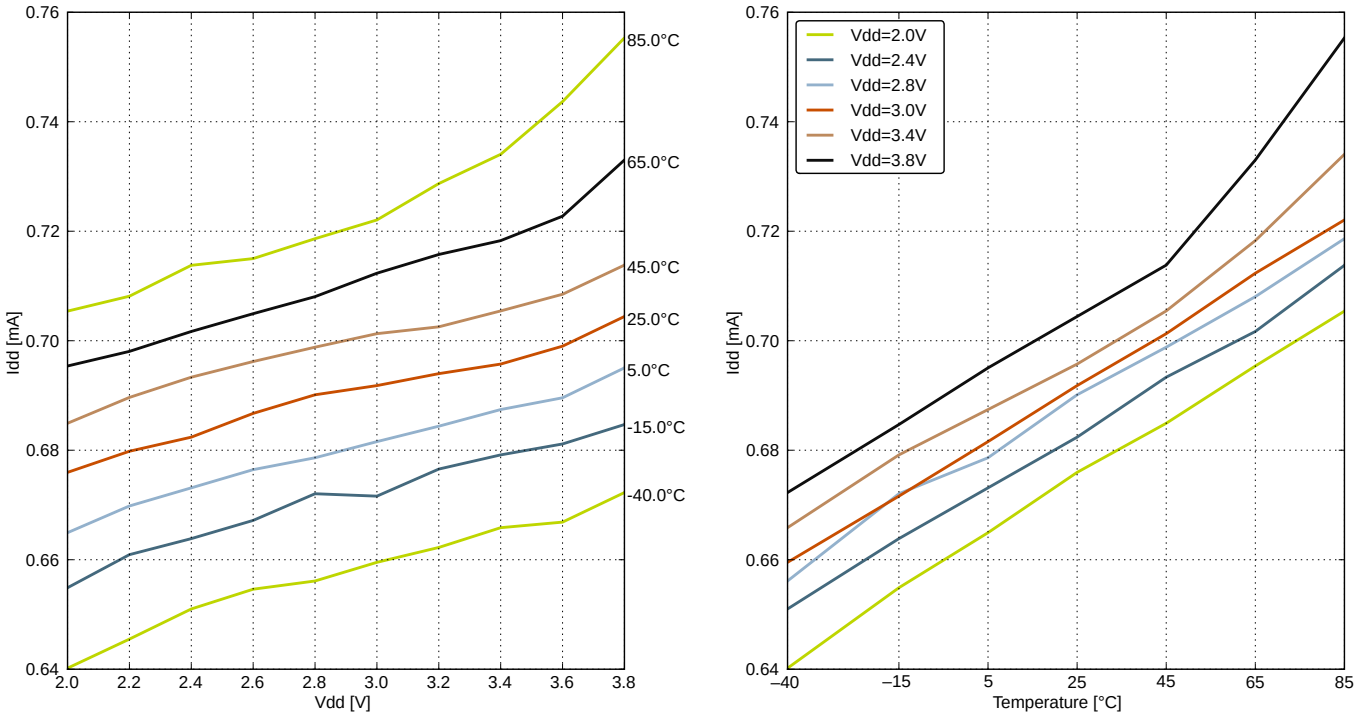


**Figure 4.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz**

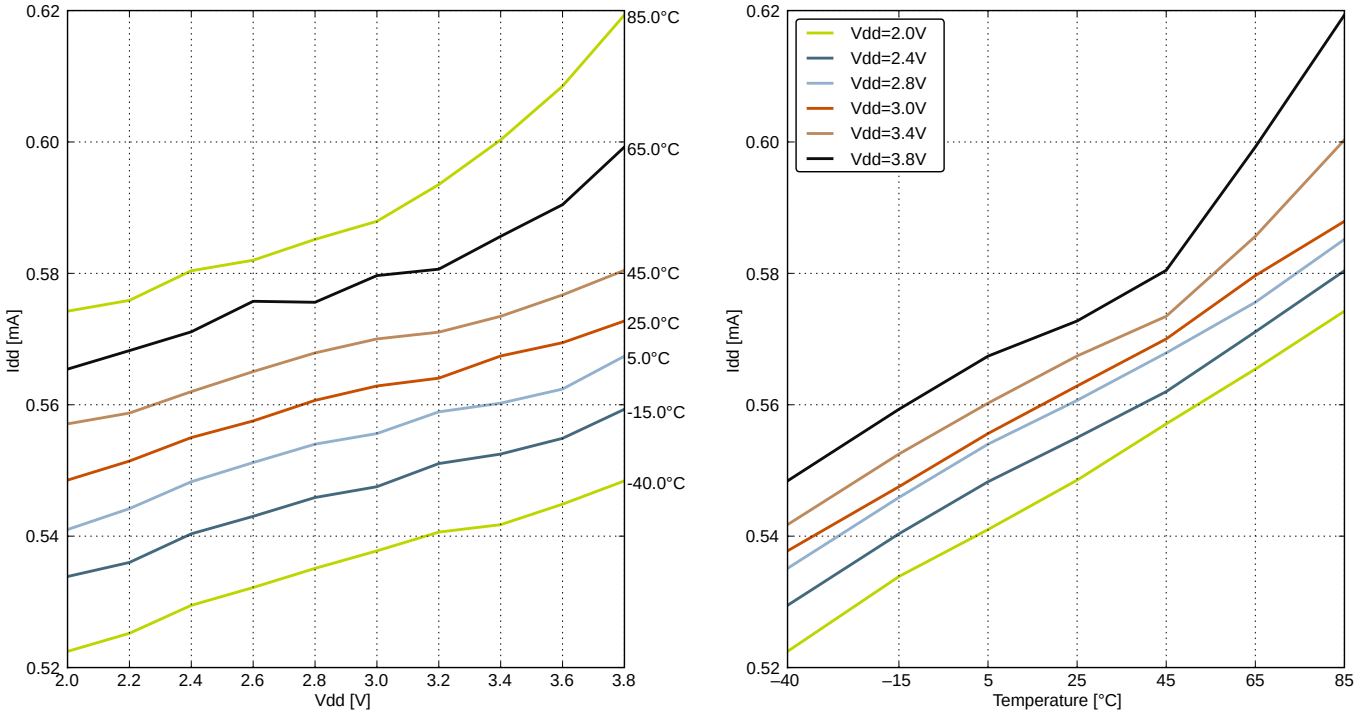


**Figure 4.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz**

## 4.7 Flash

**Table 4.6. Flash**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Flash erase cycles before failure | $EC_{FLASH}$ | | 20000 | — | — | cycles |
| Flash data retention | $RET_{FLASH}$ | $T_{AMB}$<150 ºC | 10000 | — | — | h |
| | | $T_{AMB}$<85 ºC | 10 | — | — | years |
| | | $T_{AMB}$<70 ºC | 20 | — | — | years |
| Word (32-bit) programming time | $t_{W\_PROG}$ | | 20 | — | — | µs |
| Page erase time[2] | $t_{P\_ERASE}$ | | 20.7 | 22.0 | 24.8 | ms |
| Device erase time[3] | $t_{D\_ERASE}$ | | 41.8 | 45.0 | 49.2 | ms |
| Erase current | $I_{ERASE}$ | | — | — | 7[1] | mA |
| Write current | $I_{WRITE}$ | | — | — | 7[1] | mA |
| Supply voltage during flash erase and write | $V_{FLASH}$ | | 1.98 | — | 3.8 | V |

**Note:**

1. Measured at 25 °C.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.

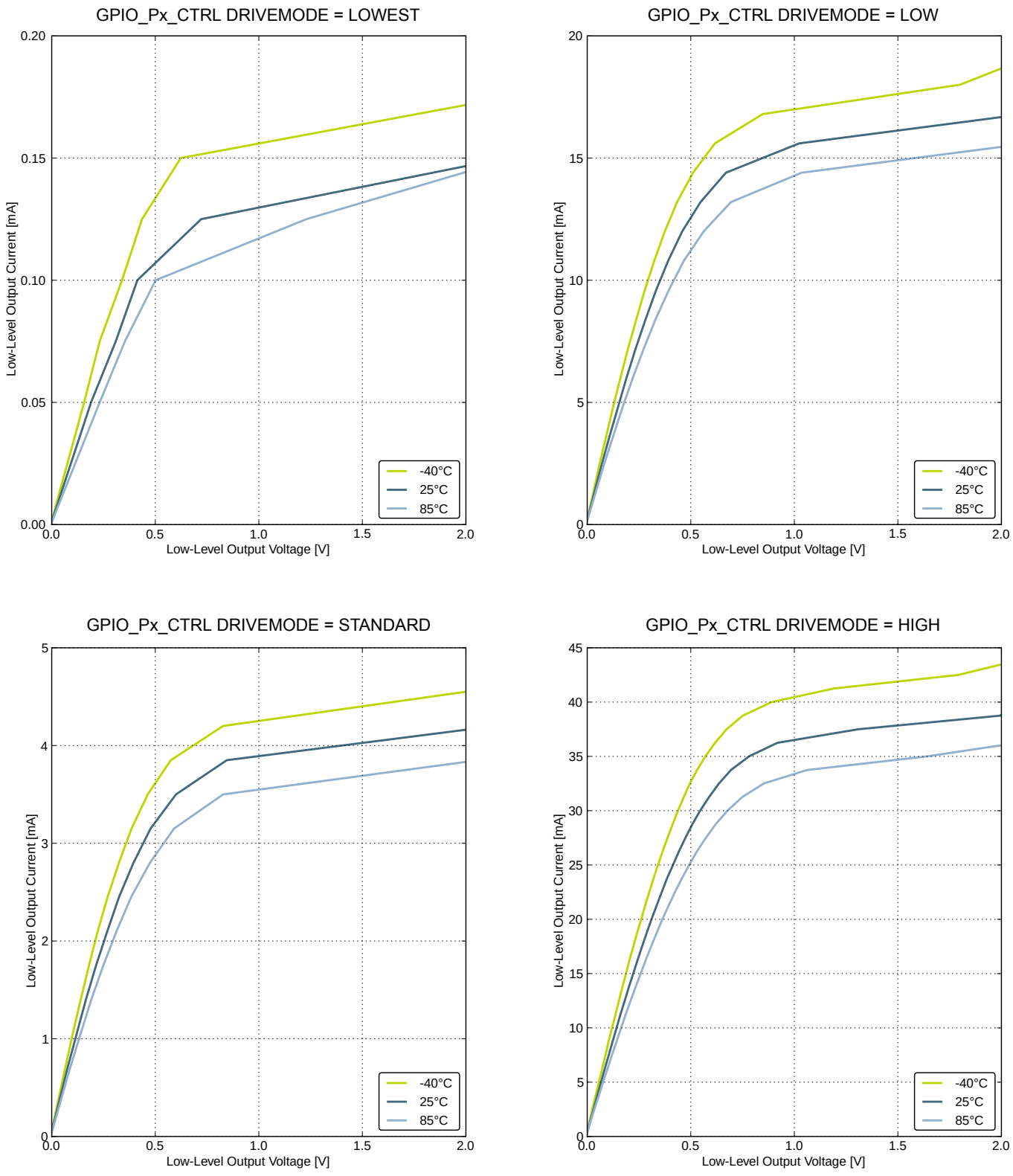


**Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage**

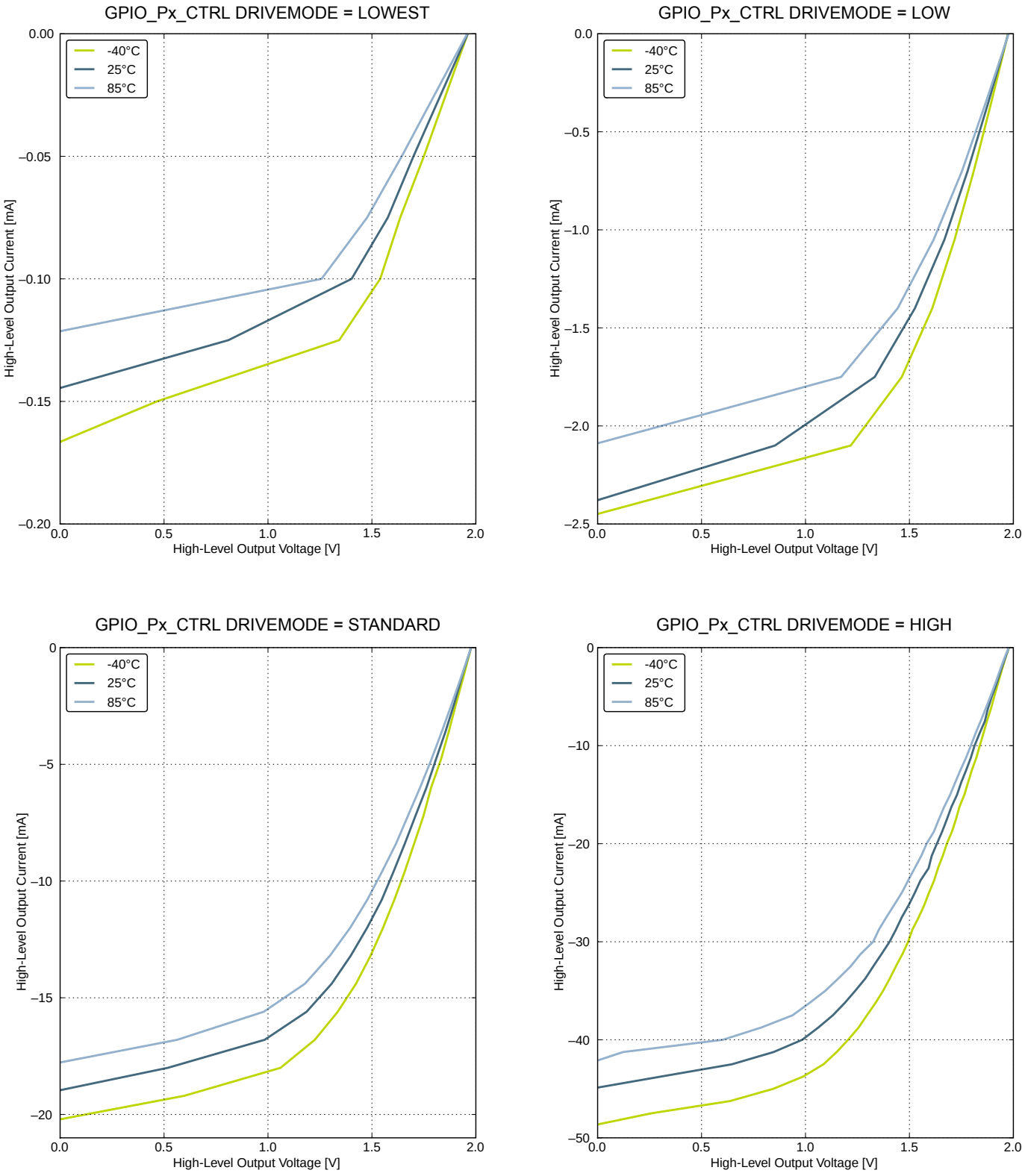


**Figure 4.15. Typical High-Level Output Current, 2V Supply Voltage**

## 4.10 Analog Digital Converter (ADC)

**Table 4.14. ADC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{ADCIN}$ | Single-ended | 0 | — | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | — | $V_{REF}/2$ | V |
| Input range of external reference voltage, single-ended and differential | $V_{ADCREFIN}$ | | 1.25 | — | $V_{DD}$ | V |
| Input range of external negative reference voltage on channel 7 | $V_{ADCREFIN\_CH7}$ | See $V_{ADCREFIN}$ | 0 | — | $V_{DD}$ - 1.1 | V |
| Input range of external positive reference voltage on channel 6 | $V_{ADCREFIN\_CH6}$ | See $V_{ADCREFIN}$ | 0.625 | — | $V_{DD}$ | V |
| Common mode input range | $V_{ADCCMIN}$ | | 0 | — | $V_{DD}$ | V |
| Input current | $I_{ADCIN}$ | 2 pF sampling capacitors | — | <100 | — | nA |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | | — | 65 | — | dB |
| Average active current | $I_{ADC}$ | 1 Msamples/s, 12 bit, external reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 735[1] | — | µA |
| | | 1 Msamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 760[1] | — | µA |
| | | 500 Ksamples/s, 12 bit, external reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 346[1] | — | µA |
| | | 500 Ksamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 354[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 00b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 52[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 01b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 50[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 10b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 54[1] | — | µA |
| Input capacitance | $C_{ADCIN}$ | | — | 2 | — | pF |
| Input ON resistance | $R_{ADCIN}$ | | 1 | — | — | MΩ |
| Input RC filter resistance | $R_{ADCFILT}$ | | — | 10 | — | kΩ |
| Input RC filter/decoupling capacitance | $C_{ADCFILT}$ | | — | 250 | — | fF |
| Input bias current | $I_{ADCBIASIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |

### 5.1.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.2. Alternate functionality overview**

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | | | Clock Management Unit, clock output number 1. |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | | Low Energy Timer LETIM0, output channel 0. |

## 5.4 EFM32G232 (TQFP64)

### 5.4.1 Pinout

The EFM32G232 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

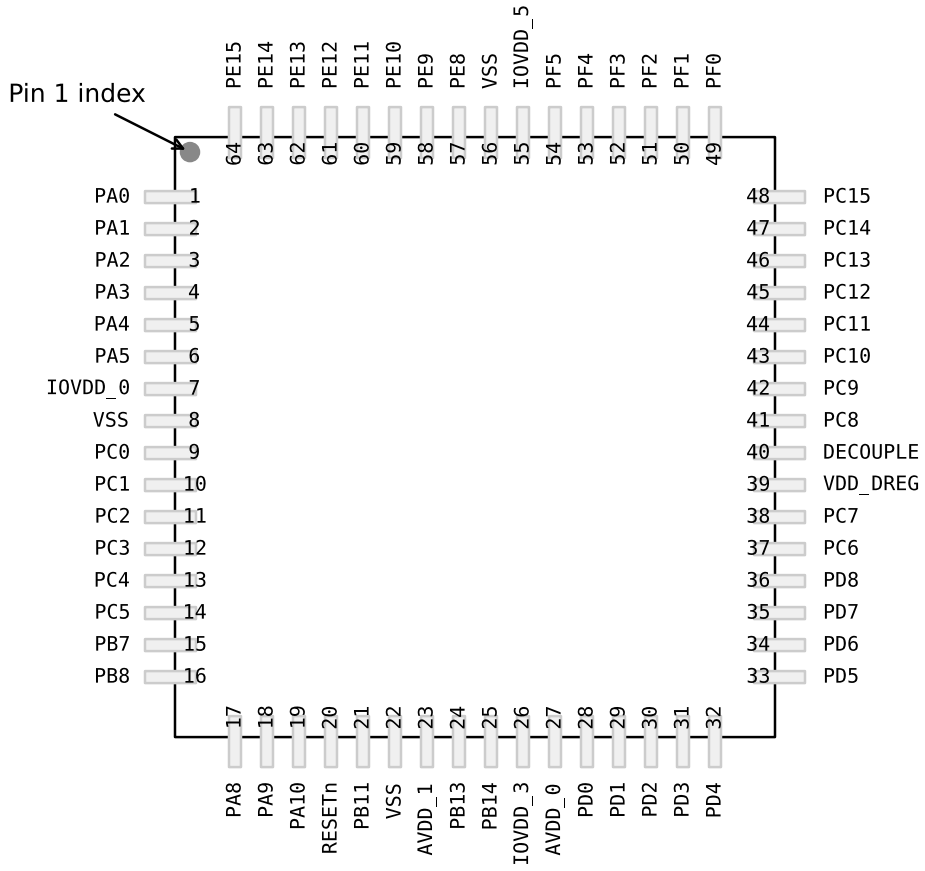


**Figure 5.4. EFM32G232 Pinout (top view, not to scale)**

**Table 5.10. Device Pinout**

| TQFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | | TIM0_CDTI0 #0 | | |
| 5 | PA4 | | TIM0_CDTI1 #0 | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A6 | PF7 | | | TIM0_CC1 #2 | U0_RX #0 | |
| A7 | PF5 | | EBI_REn #0 | TIM0_CDTI2 #2 | | |
| A8 | PF4 | | EBI_WEn #0 | TIM0_CDTI1 #2 | | |
| A9 | PE4 | | | | US0_CS #1 | |
| A10 | PC14 | ACMP1_CH6 | | TIM0_CDTI1 #1/3<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | U0_TX #3 | |
| A11 | PC15 | ACMP1_CH7 | | TIM0_CDTI2 #1/3<br>TIM1_CC2 #0 | U0_RX #3 | DBG_SWO #1 |
| B1 | PA15 | | EBI_AD08 #0 | | | |
| B2 | PE13 | | EBI_AD05 #0 | | US0_CS #0 | ACMP0_O #0 |
| B3 | PE11 | | EBI_AD03 #0 | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| B4 | PE8 | | EBI_AD00 #0 | PCNT2_S0IN #1 | | |
| B5 | PD11 | | EBI_CS2 #0 | | | |
| B6 | PF8 | | | TIM0_CC2 #2 | | |
| B7 | PF6 | | | TIM0_CC0 #2 | U0_TX #0 | |
| B8 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2 | | |
| B9 | PE5 | | | | US0_CLK #1 | |
| B10 | PC12 | ACMP1_CH4 | | | | CMU_CLK0 #1 |
| B11 | PC13 | ACMP1_CH5 | | TIM0_CDTI0 #1/3<br>TIM1_CC0 #0<br>PCNT0_S0IN #0 | | |
| C1 | PA1 | | EBI_AD10 #0 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| C2 | PA0 | | EBI_AD09 #0 | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| C3 | PE10 | | EBI_AD02 #0 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | |
| C5 | PD12 | | EBI_CS3 #0 | | | |
| C6 | PF9 | | | | | |
| C7 | VSS | Ground. | | | | |
| C8 | PF2 | | EBI_ARDY #0 | | | ACMP1_O #0<br>DBG_SWO #0 |
| C9 | PE6 | | | | US0_RX #1 | |
| C10 | PC10 | ACMP1_CH2 | | TIM2_CC2 #2 | US0_RX #2 | |
| C11 | PC11 | ACMP1_CH3 | | | US0_TX #2 | |
| D1 | PA3 | | EBI_AD12 #0 | TIM0_CDTI0 #0 | U0_TX #2 | |
| D2 | PA2 | | EBI_AD11 #0 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| K5 | PA11 | | | | | |
| K6 | RESETn | Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |
| K11 | PD1 | ADC0_CH 1 | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| L1 | PB8 | LFXTAL_N | | | US1_CS #0 | |
| L2 | PC5 | ACMP0_C H5 | | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| L3 | PA14 | | | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OU T0 | | LETIM0_OUT0 #1 | | |
| L6 | PB12 | DAC0_OU T1 | | LETIM0_OUT1 #1 | | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_ P | | | LEU0_TX #1 | |
| L9 | PB14 | HFXTAL_ N | | | LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |
| L11 | PD0 | ADC0_CH 0 | | PCNT2_S0IN #0 | US1_TX #1 | |

### 5.6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.17. Alternate functionality overview**

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| PCNT1_S0IN | PC4 | PB3 | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | PA12 | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | PA13 | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | PA14 | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | | PD1 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | PD0 | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | USART2 chip select input / output. |
| US2_RX | | PB4 | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 53 | PD7 | ADC0_CH7 | | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 54 | PD8 | | | | | CMU_CLK1 #1 |
| 55 | PC6 | ACMP0_CH6 | | | LEU1_TX #0<br>I2C0_SDA #2 | |
| 56 | PC7 | ACMP0_CH7 | | | LEU1_RX #0<br>I2C0_SCL #2 | |
| 57 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| 58 | VSS | Ground. | | | | |
| 59 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| 60 | PE0 | | | PCNT0_S0IN #1 | U0_TX #1 | |
| 61 | PE1 | | | PCNT0_S1IN #1 | U0_RX #1 | |
| 62 | PE2 | | | | | ACMP0_O #1 |
| 63 | PE3 | | | | | ACMP1_O #1 |
| 64 | PE4 | LCD_COM0 | | | US0_CS #1 | |
| 65 | PE5 | LCD_COM1 | | | US0_CLK #1 | |
| 66 | PE6 | LCD_COM2 | | | US0_RX #1 | |
| 67 | PE7 | LCD_COM3 | | | US0_TX #1 | |
| 68 | PC8 | ACMP1_CH0 | | TIM2_CC0 #2 | US0_CS #2 | |
| 69 | PC9 | ACMP1_CH1 | | TIM2_CC1 #2 | US0_CLK #2 | |
| 70 | PC10 | ACMP1_CH2 | | TIM2_CC2 #2 | US0_RX #2 | |
| 71 | PC11 | ACMP1_CH3 | | | US0_TX #2 | |
| 72 | PC12 | ACMP1_CH4 | | | | CMU_CLK0 #1 |
| 73 | PC13 | ACMP1_CH5 | | TIM0_CDTI0 #1/3<br>TIM1_CC0 #0<br>PCNT0_S0IN #0 | | |
| 74 | PC14 | ACMP1_CH6 | | TIM0_CDTI1 #1/3<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | U0_TX #3 | |
| 75 | PC15 | ACMP1_CH7 | | TIM0_CDTI2 #1/3<br>TIM1_CC2 #0 | U0_RX #3 | DBG_SWO #1 |
| 76 | PF0 | | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DAC0_OUT1 | PB12 | | | | Digital to Analog Converter DAC0 output channel number 1. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_AD00 | PE8 | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | | | | External Bus Interface (EBI) Address Latch Enable output. |

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| LCD_SEG7 | PE11 | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20 | PB3 | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG21 | PB4 | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG22 | PB5 | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG23 | PB6 | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG24 | PF6 | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|
| D | 0.170 | — | 0.270 | S1 | — | 4.500 BSC | — |
| E | 0.950 | — | 1.050 | V | — | 9.000 BSC | — |
| F | 0.170 | — | 0.230 | V1 | — | 4.5000 BSC | — |
| G | — | 0.500 BSC | — | W | — | 0.200 BSC | — |
| H | 0.050 | — | 0.150 | AA | — | 1.000BSC | — |
| J | 0.090 | — | 0.200 | | | | |
| K | 0.500 | — | 0.700 | | | | |
| L | 0DEG | — | 7DEG | | | | |

The TQFP48 Package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

### 10.2 QFN64 PCB Layout

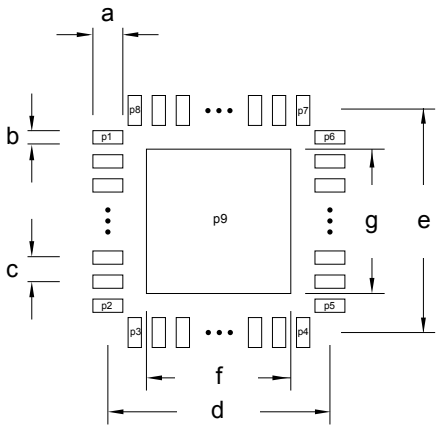


**Figure 10.2. QFN64 PCB Land Pattern**

**Table 10.2. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 0.85 | P1 | 1 | P8 | 64 |
| b | 0.30 | P2 | 16 | P9 | 65 |
| c | 0.50 | P3 | 17 | | |
| d | 8.90 | P4 | 32 | | |
| e | 8.90 | P5 | 33 | | |
| f | 7.20 | P6 | 48 | | |
| g | 7.20 | P7 | 49 | | |

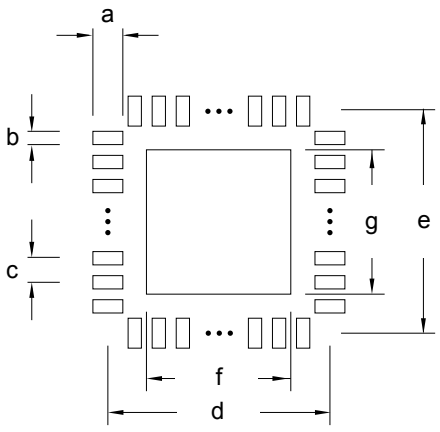


**Figure 10.3. QFN64 PCB Solder Mask**

**Table 10.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|---|---|---|---|
| a | 0.97 | e | 8.90 |
| b | 0.42 | f | 7.32 |
| c | 0.50 | g | 7.32 |

### 11.2 QFN32 PCB Layout

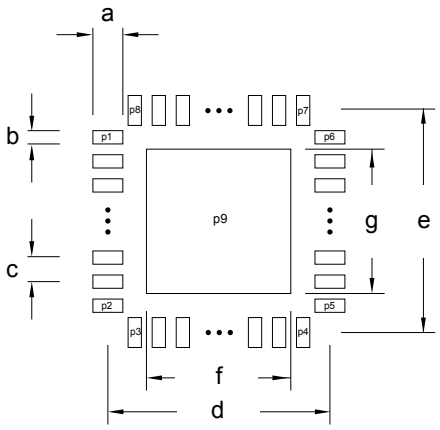


**Figure 11.2. QFN32 PCB Land Pattern**

**Table 11.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 0.80 | P1 | 1 | P6 | 24 |
| b | 0.35 | P2 | 8 | P7 | 25 |
| c | 0.65 | P3 | 9 | P8 | 32 |
| d | 6.00 | P4 | 16 | P9 | 33 |
| e | 6.00 | P5 | 17 | | |
| f | 4.40 | | | | |
| g | 4.40 | | | | |

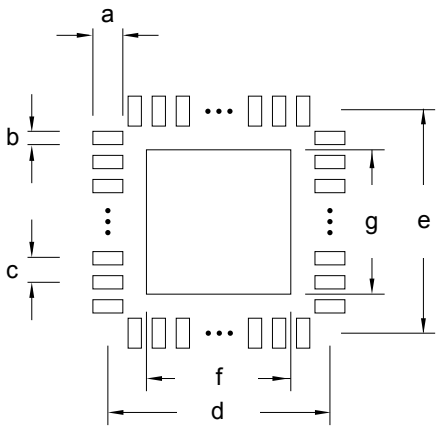


**Figure 11.3. QFN32 PCB Solder Mask**

**Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.92 |
| b | 0.47 |
| c | 0.65 |

| Symbol | Dim. (mm) |
|---|---|
| d | 6.00 |
| e | 6.00 |
| f | 4.52 |
| g | 4.52 |

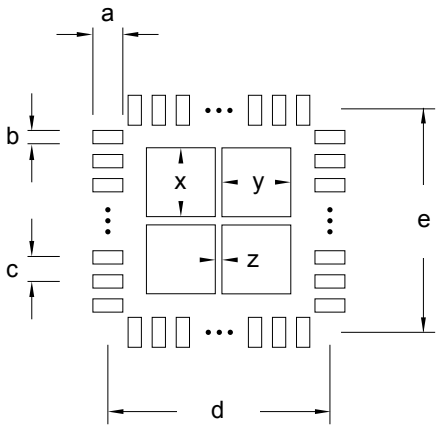


**Figure 11.4. QFN32 PCB Stencil Design**

**Table 11.4. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.70 |
| b | 0.25 |
| c | 0.65 |
| d | 6.00 |
| e | 6.00 |
| x | 1.30 |
| y | 1.30 |
| z | 0.50 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see 5. Pin Definitions.

Corrected pin number for symbol P3 in Table 11.2 QFN32 PCB Land Pattern Dimensions (Dimensions in mm) on page 191.

Updated package marking figures to include temperature grade.

### 13.3 Revision 1.90

May 22nd, 2015

For devices with an ADC, Added clarification on conditions for $INL_{ADC}$ and $DNL_{ADC}$ parameters.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Updated HFRCO table in the Electrical Characteristics section.

Updated EM0, EM2, EM3, and EM4 maximum current specifications in the Electrical Characteristics section.

Updated the Output Low Voltage maximum for sinking 20 mA with VDD = 3.0 V in the Electrical Characteristics section.

Updated the Input Leakage Current maximum in the Electrical Characteristics section.

Updated the minimum and maximum frequency specifications for the LFRCO, HFRCO, and AUXHFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Added some minimum ADC SNR, SNDR, and SFDR specifications in the Electrical Characteristics section.

Added some minimum and maximum ADC offset voltage, DNL, and INL specifications in the Electrical Characteristics section.

Added maximum DAC current specifications in the Electrical Characteristics section.

Added maximum ACMP current and maximum and minimum offset voltage specifications in the Electrical Characteristics section.

Added maximum VCMP current and updated typical VCMP current specifications in the Electrical Characteristics section.

Updated references to energyAware Designer to Configurator.

### 13.4 Revision 1.80

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

For devices with an ACMP, updated ACMP data.