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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g880f32-qfp100t

2. Ordering Information

The following table shows the available EFM32G devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32G200F16G-E-QFN32	16	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F32G-E-QFN32	32	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F64G-E-QFN32	64	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G210F128G-E-QFN32	128	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G222F32G-E-QFP48	32	8	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F64G-E-QFP48	64	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F128G-E-QFP48	128	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G230F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G232F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G280F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G290F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G840F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G842F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G880F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G890F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112

3. System Overview

3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32G devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32G Reference Manual.

The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

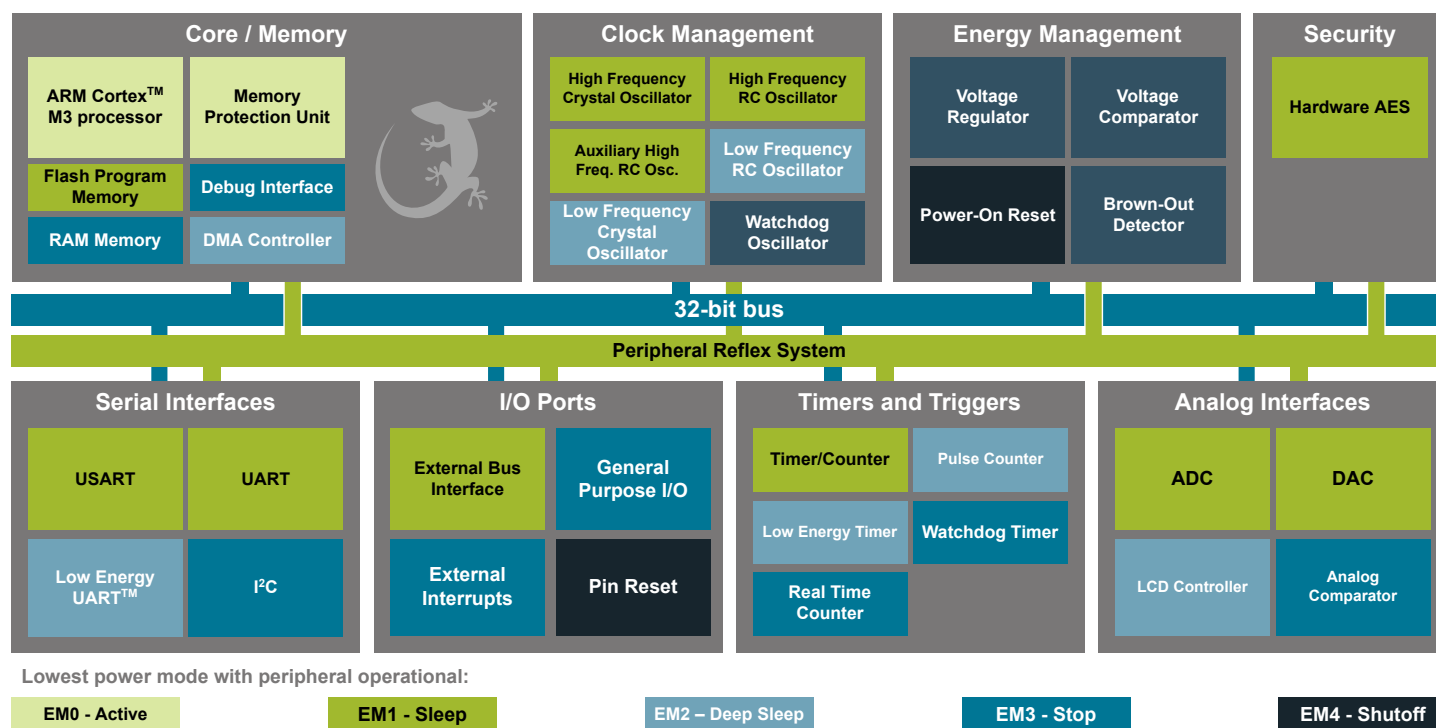


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32G Reference Manual.

3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

3.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32G.

3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32G microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32G. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

3.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M3. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

3.1.11 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 Smart-Cards, and IrDA devices.

3.1.13 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

3.2.10 EFM32G880

The features of the EFM32G880 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.10. EFM32G880 Configuration Summary

Module	Module	Module
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	86 pins	Available pins are shown in Table 4.3 (p. 57)

Module	Module	Module
LCD	Full configuration	LCD_SEG[39:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

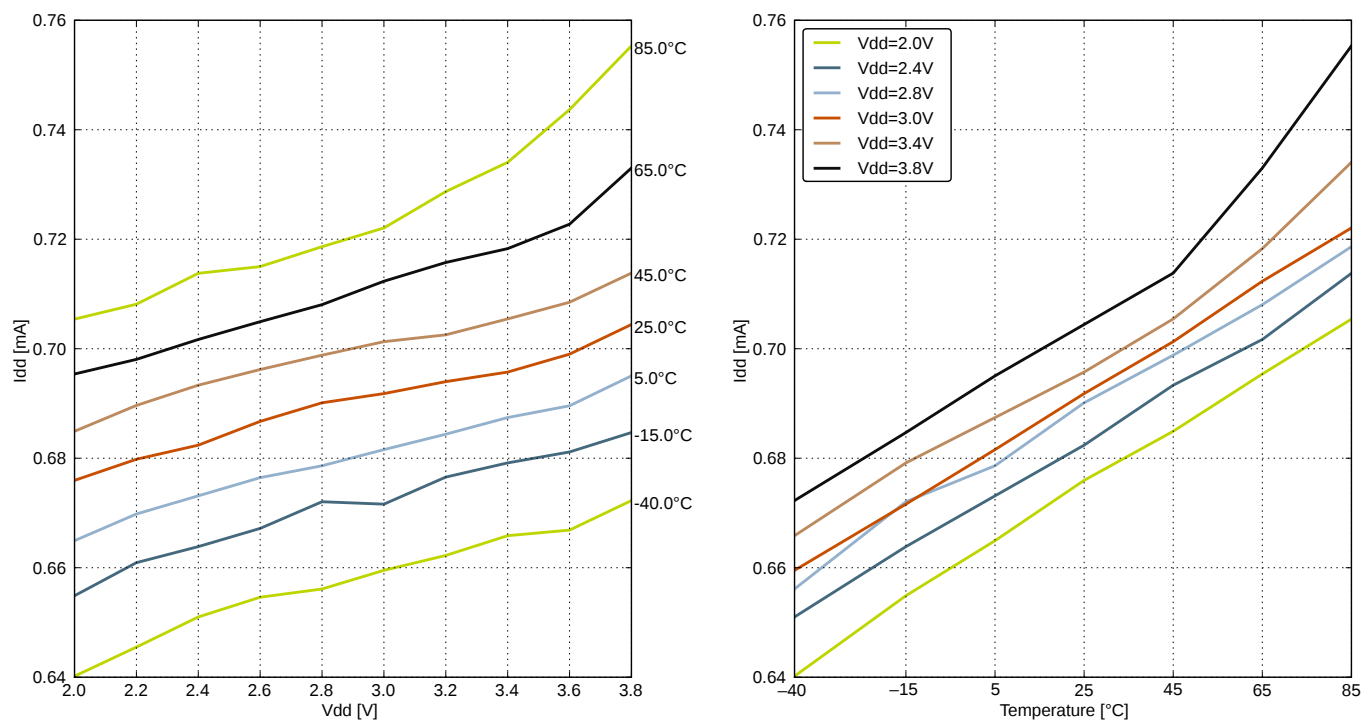


Figure 4.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz

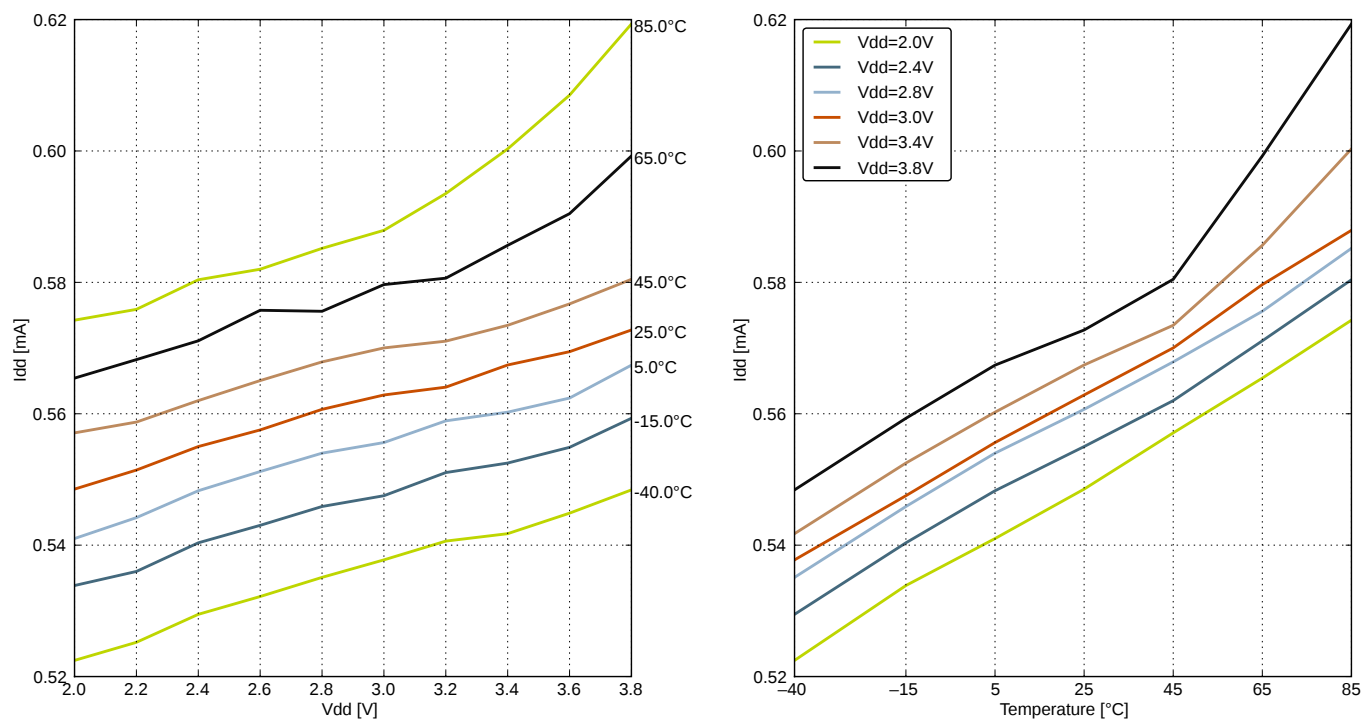


Figure 4.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

4.9.3 LFRCO

Table 4.10. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, $V_{DD}=3.0$ V, $T_{AMB}=25^{\circ}\text{C}$	f_{LFRCO}		31.29	32.768	34.24	kHz
Startup time not including software calibration	t_{LFRCO}		—	150	—	μs
Current consumption	I_{LFRCO}		—	190	—	nA
Temperature coefficient	TC_{LFRCO}		—	± 0.02	—	$\%/^{\circ}\text{C}$
Supply voltage coefficient	VC_{LFRCO}		—	± 15	—	$\%/V$
Frequency step for LSB change in TUNING value	$TUNESTEP_{LFRCO}$		—	1.5	—	%

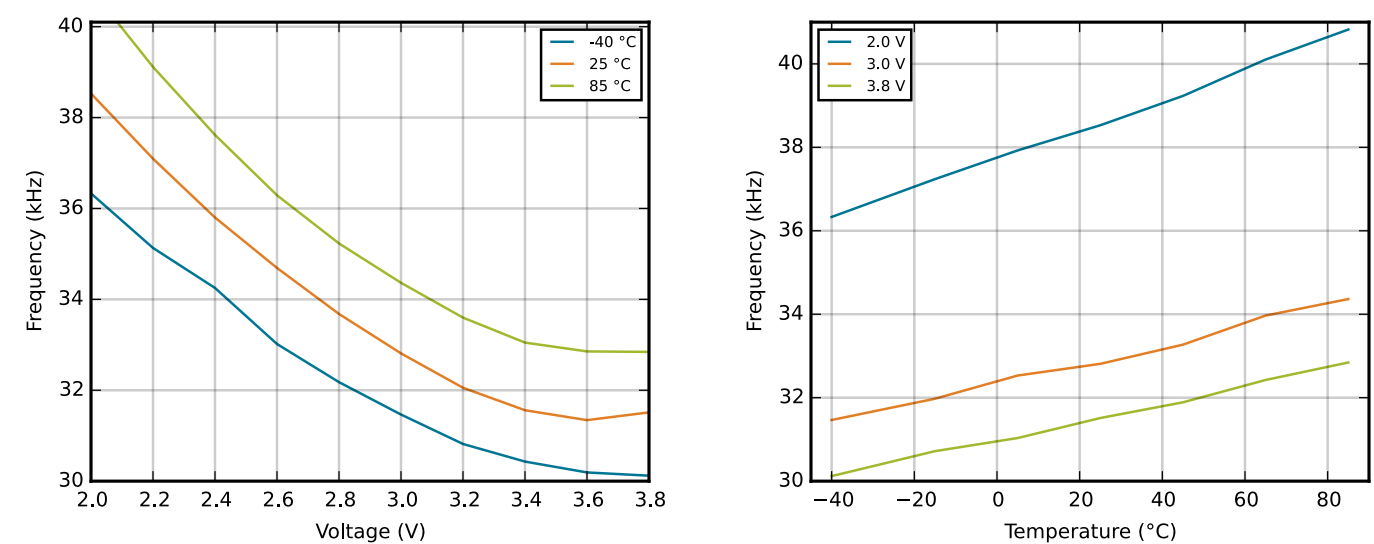


Figure 4.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
7	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
8	PC2	ACMP0_CH2			
9	PC3	ACMP0_CH3			
10	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0		
11	PB7	LFXTAL_P		US1_CLK #0	
12	PB8	LFXTAL_N		US1_CS #0	
13	PA8		TIM2_CC0 #0		
14	PA9		TIM2_CC1 #0		
15	PA10		TIM2_CC2 #0		
16	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
17	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
18	VSS	Ground.			
19	AVDD_1	Analog power supply 1.			
20	PB13	HFXTAL_P		LEU0_TX #1	
21	PB14	HFXTAL_N		LEU0_RX #1	
22	IOVDD_3	Digital IO power supply 3.			
23	AVDD_0	Analog power supply 0.			
24	PD4	ADC0_CH4		LEU0_TX #0	
25	PD5	ADC0_CH5		LEU0_RX #0	
26	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
27	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
28	VDD_DREG	Power supply for on-chip voltage regulator.			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
30	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
31	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
32	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
33	PC11	ACMP1_CH3		US0_TX #2	
34	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
35	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
36	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
37	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1

5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G230 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.9. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	—	—	—	—	PA10	PA8	PA8 —	—	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	—	—	PB8	PB7	—	—	—	—	—	—	—
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	—	—	—	—	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

5.4 EFM32G232 (TQFP64)

5.4.1 Pinout

The EFM32G232 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

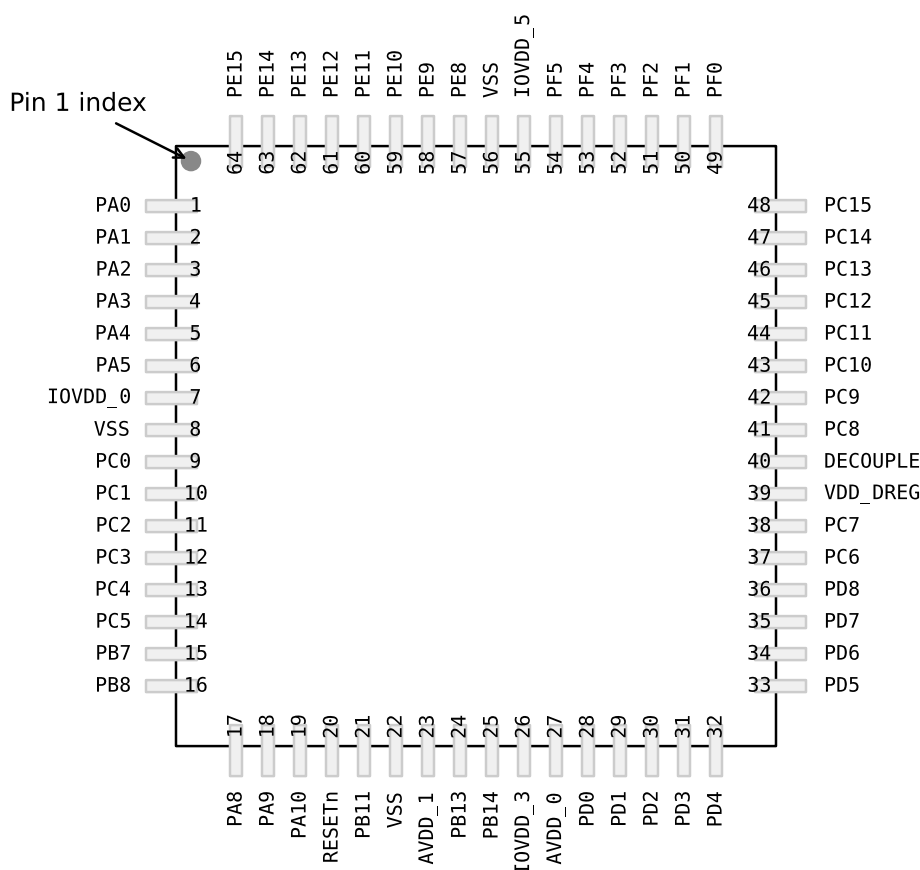


Figure 5.4. EFM32G232 Pinout (top view, not to scale)

Table 5.10. Device Pinout

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3		TIM0_CDTI0 #0		
5	PA4		TIM0_CDTI1 #0		

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
44	PC11	ACMP1_CH3		US0_TX #2	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2				ACMP1_O #0 DBG_SWO #0
52	PF3		TIM0_CDTI0 #2		
53	PF4		TIM0_CDTI1 #2		
54	PF5		TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground.			
57	PE8		PCNT2_S0IN #1		
58	PE9		PCNT2_S1IN #1		
59	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
60	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX
61	PE12		TIM1_CC2 #1	US0_CLK #0	
62	PE13			US0_CS #0	ACMP0_O #0
63	PE14			LEU0_TX #2	
64	PE15			LEU0_RX #2	

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PA5	LCD_SEG18	TIM0_CDTI2 #0	LEU1_TX #1	
7	IOVDD_0	Digital IO power supply 0.			
8	VSS	Ground.			
9	PB3	LCD_SEG20	PCNT1_S0IN #1	US2_TX #1	
10	PB4	LCD_SEG21	PCNT1_S1IN #1	US2_RX #1	
11	PB5	LCD_SEG22		US2_CLK #1	
12	PB6	LCD_SEG23		US2_CS #1	
13	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
14	PC5	ACMP0_CH5	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
15	PB7	LFXTAL_P		US1_CLK #0	
16	PB8	LFXTAL_N		US1_CS #0	
17	PA12	LCD_BCAP_P	TIM2_CC0 #1		
18	PA13	LCD_BCAP_N	TIM2_CC1 #1		
19	PA14	LCD_BEXT	TIM2_CC2 #1		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
22	VSS	Ground.			
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		LEU0_TX #1	
25	PB14	HFXTAL_N		LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	
31	PD3	ADC0_CH3	TIM0_CC2 #3	US1_CS #1	
32	PD4	ADC0_CH4		LEU0_TX #0	
33	PD5	ADC0_CH5		LEU0_RX #0	
34	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
35	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
36	PD8				CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	

5.10 EFM32G890 (BGA112)

5.10.1 Pinout

The EFM32G890 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

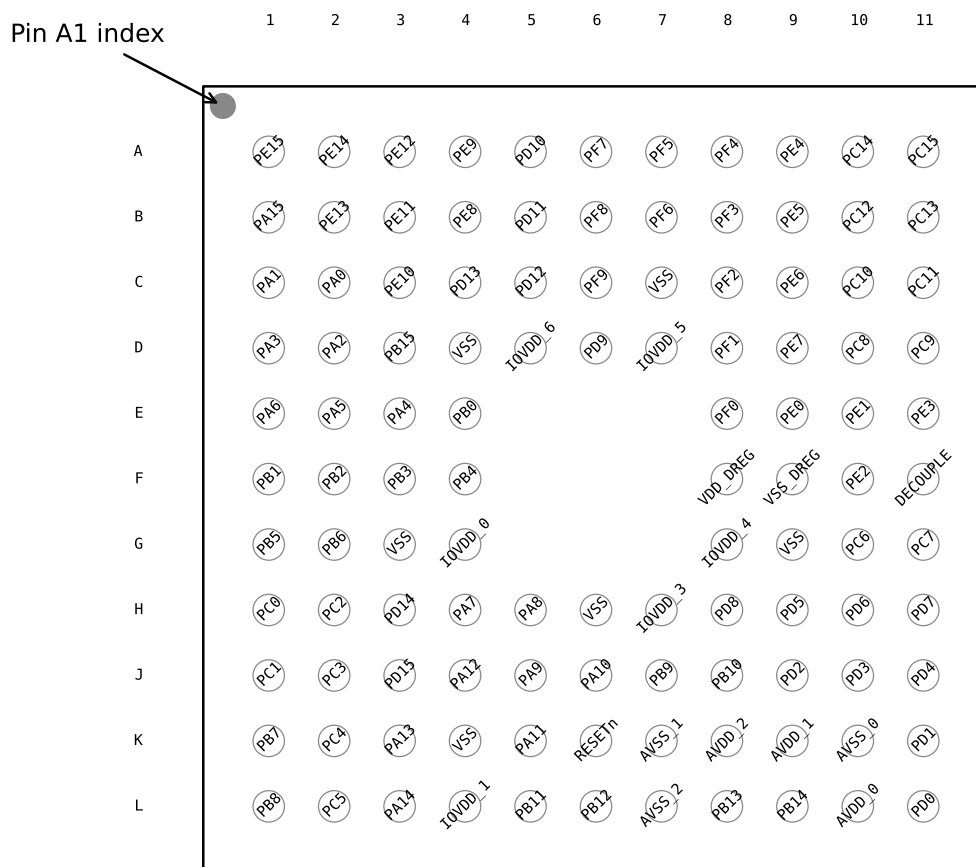


Figure 5.10. EFM32G890 Pinout (top view, not to scale)

Table 5.28. Device Pinout

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15	LCD_SEG 11	EBI_AD07 #0		LEU0_RX #2	
A2	PE14	LCD_SEG 10	EBI_AD06 #0		LEU0_TX #2	
A3	PE12	LCD_SEG 8	EBI_AD04 #0	TIM1_CC2 #1	US0_CLK #0	

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MI-SO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MI-SO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MI-SO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

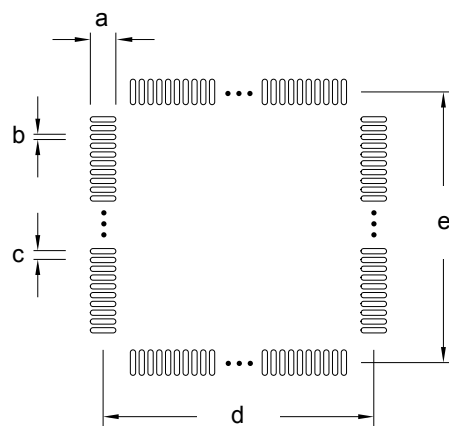


Figure 7.4. LQFP100 PCB Stencil Design

Table 7.4. LQFP100 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.35
b	0.20
c	0.50
d	15.40
e	15.40

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
b	0.17	0.22	0.27	S	0.20	—	—
b1	0.17	0.20	0.23	θ	0°	3.5°	7°
c	0.09	—	0.20	θ1	0°	—	—
C1	0.09	—	0.16	θ2	11°	12°	13°
D	12.0 BSC			θ3	11°	12°	13°
D1	10.0 BSC						
e	0.50 BSC						
E	12.0 BSC						
E1	10.0 BSC						
L	0.45	0.60	0.75				

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

8.3 TQFP64 Package Marking

In the illustration below package fields and position are shown.

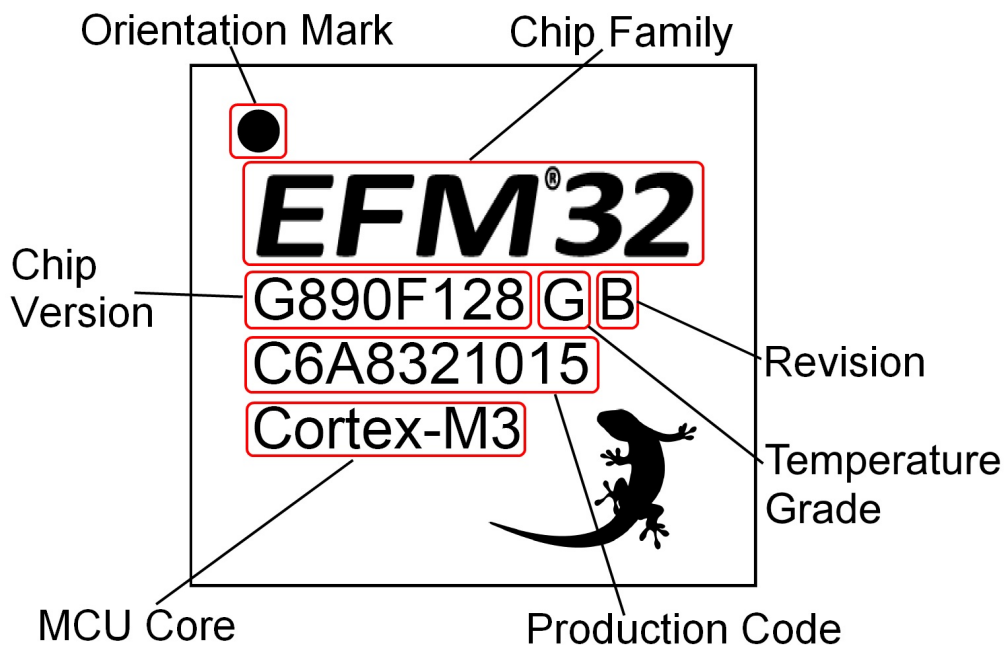


Figure 8.5. Example Chip Marking (Top View)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
d	8.90	-	-

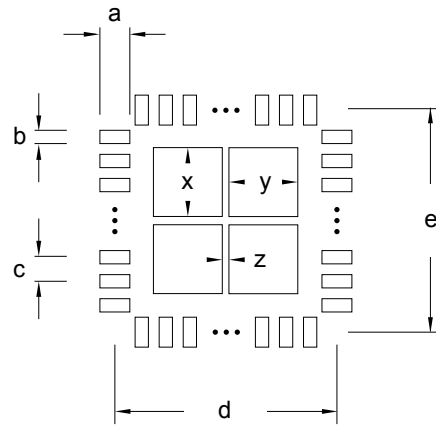


Figure 10.4. QFN64 PCB Stencil Design

Table 10.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.75	e	8.90
b	0.22	x	2.70
c	0.50	y	2.70
d	8.90	z	0.80

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

11.2 QFN32 PCB Layout

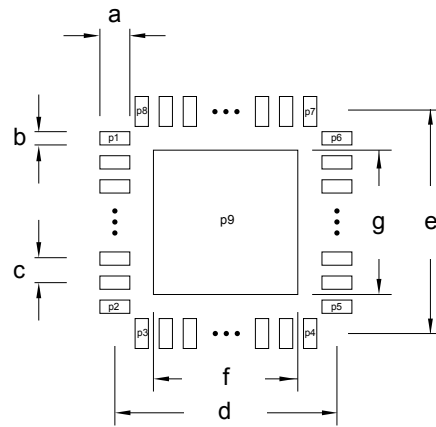


Figure 11.2. QFN32 PCB Land Pattern

Table 11.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
c	0.65	P3	9	P8	32
d	6.00	P4	16	P9	33
e	6.00	P5	17		
f	4.40				
g	4.40				

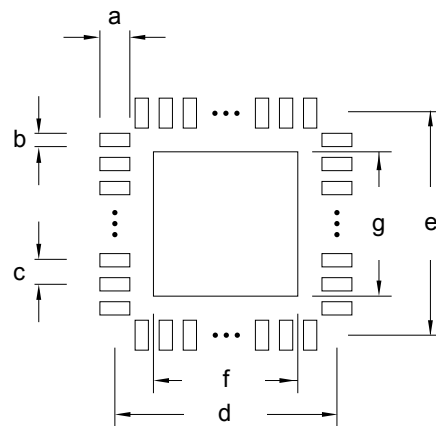


Figure 11.3. QFN32 PCB Solder Mask

Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.92
b	0.47
c	0.65