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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g880f64-qfp100t

  - Supply Voltage Comparator
- Ultra efficient Power-on Reset and Brown-Out Detector
- 2-pin Serial Wire Debug Interface
  - 1-pin Serial Wire Viewer
- Pre-Programmed USB/UART Bootloader
- Temperature range -40 to 85 ºC
- Single power supply 1.98 to 3.8 V
- Packages
  - BGA112
  - LQFP100
  - TQFP64
  - TQFP48
  - QFN64
  - QFN32

3.2.11 EFM32G890

The features of the EFM32G890 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.11. EFM32G890 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 57)

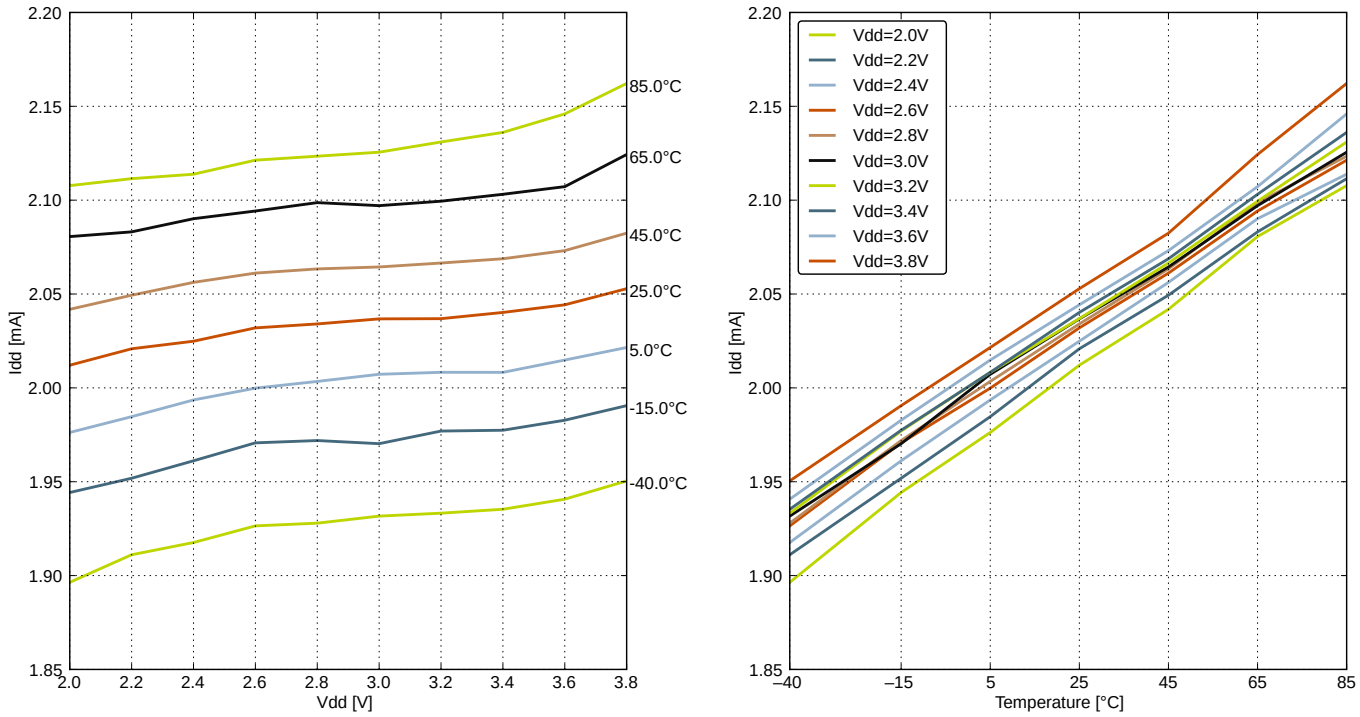

Figure 4.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz

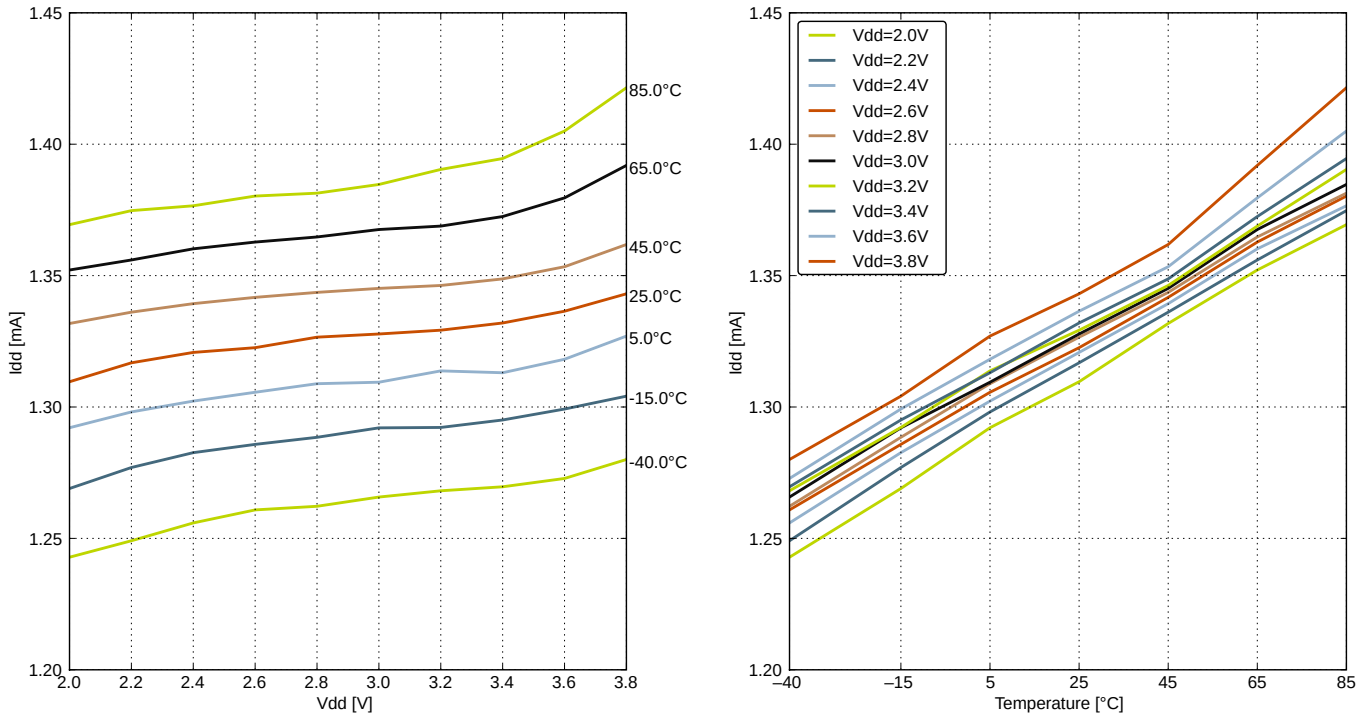

Figure 4.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 7 MHz

4.7 Flash

Table 4.6. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 ºC	10000	—	—	h
		T_{AMB}<85 ºC	10	—	—	years
		T_{AMB}<70 ºC	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time[2]	t_{P_ERASE}		20.7	22.0	24.8	ms
Device erase time[3]	t_{D_ERASE}		41.8	45.0	49.2	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

Note:

1. Measured at 25 °C.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.

4.8 General Purpose Input Output

Table 4.7. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	$0.30 \times V_{DD}$[1]	V
Input high voltage	V_{IOIH}		$0.70 \times V_{DD}$[1]	—	—	V
Output high voltage (Production test condition = 3.0 V, DRIVEMODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.80 \times V_{DD}$	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.90 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.85 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.90 \times V_{DD}$	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75 \times V_{DD}$	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80 \times V_{DD}$	—	—	V

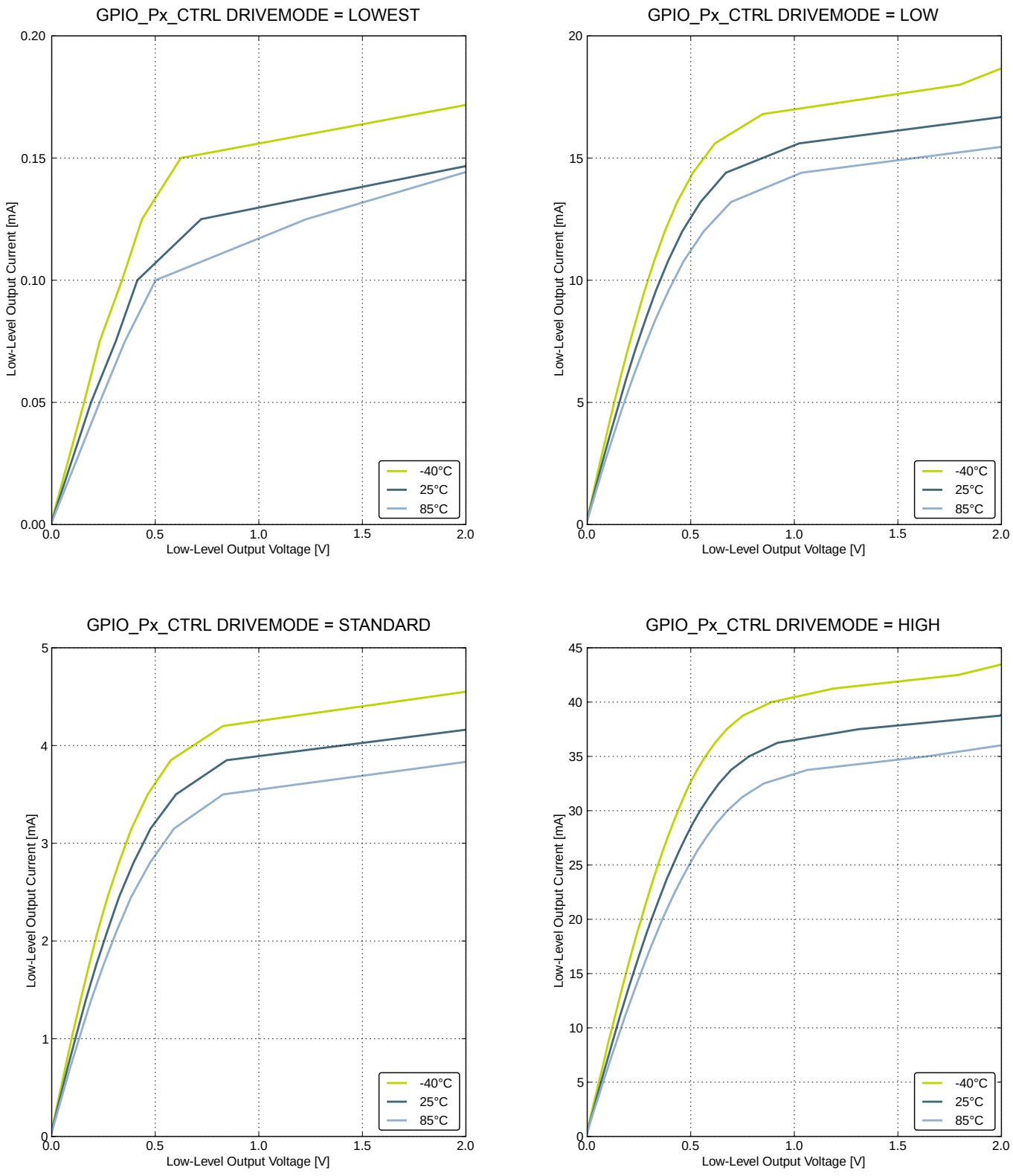

Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage

4.9.2 HFXO

Table 4.9. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal Frequency	f_{HFXO}		4	—	32	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 32 MHz	—	30	60	Ω
		Crystal frequency 4 MHz	—	400	1500	Ω
The transconductance of the HFXO input transistor at crystal startup	g_{mHFXO}	HFXOBOOST in CMU_CTRL equals 0b11	20	—	—	mS
Supported crystal external load range	C_{HFXOL}		5	—	25	pF
Current consumption for HFXO after startup	I_{HFXO}	4 MHz: ESR=400 Ω, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	85	—	µA
		32 MHz: ESR=30 Ω, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	165	—	µA
Startup time	t_{HFXO}	32 MHz: ESR=30 Ω, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	400	—	µs
Pulse width removed by glitch detector			1	—	4	ns

4.9.3 LFRCO

Table 4.10. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	f_{LFRCO}		31.29	32.768	34.24	kHz
Startup time not including software calibration	t_{LFRCO}		—	150	—	µs
Current consumption	I_{LFRCO}		—	190	—	nA
Temperature coefficient	TC_{LFRCO}		—	±0.02	—	%/°C
Supply voltage coefficient	VC_{LFRCO}		—	±15	—	%/V
Frequency step for LSB change in TUNING value	$TUNESTEP_{LFRCO}$		—	1.5	—	%

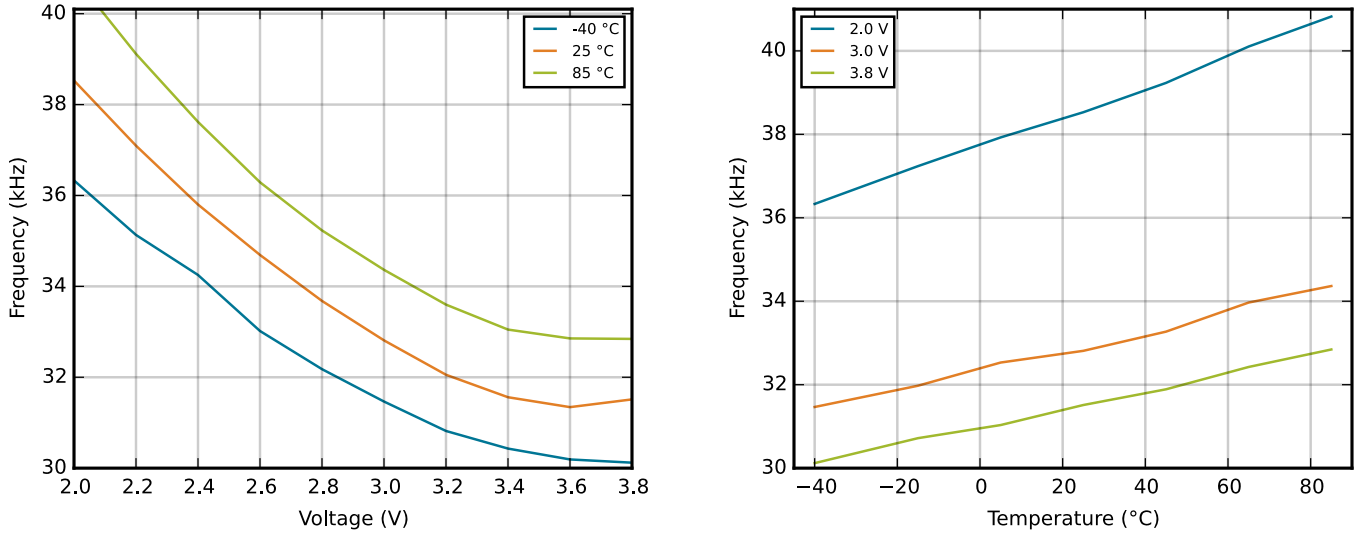

Figure 4.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

5.1.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G200 and EFM32G210 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	—	—	—	—	—	—	—	—	—	—	—	—	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	—	—	—	—	—	—	—
Port C	PC15	PC14	PC13	—	—	—	—	—	—	—	—	—	—	—	PC1	PC0
Port D	—	—	—	—	—	—	—	—	PD7	PD6	PD5	PD4	—	—	—	—
Port E	—	—	PE13	PE12	PE11	PE10	—	—	—	—	—	—	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	—	—	—	PF2	PF1	PF0

5.3 EFM32G230 (QFN64)

5.3.1 Pinout

The EFM32G230 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

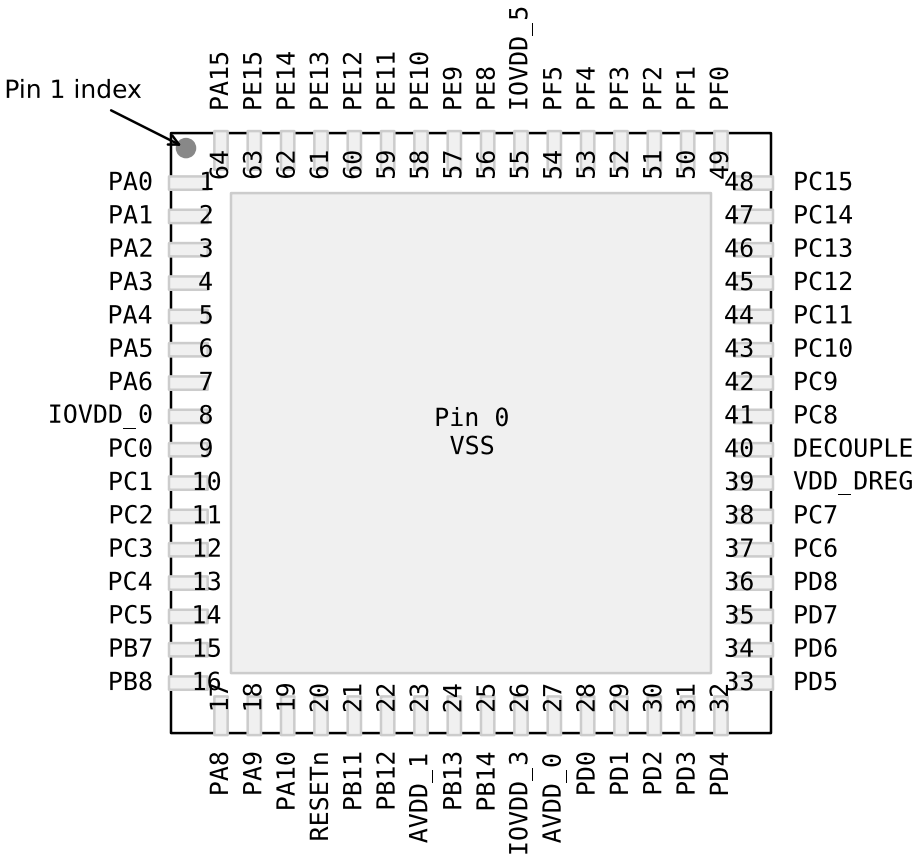

Figure 5.3. EFM32G230 Pinout (top view, not to scale)

Table 5.7. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3		TIM0_CDTI0 #0		
5	PA4		TIM0_CDTI1 #0		

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
37	PB9					
38	PB10					
39	PB11	DAC0_OUT0		LETIM0_OUT0 #1		
40	PB12	DAC0_OUT1		LETIM0_OUT1 #1		
41	AVDD_1	Analog power supply 1.				
42	PB13	HFXTAL_P			LEU0_TX #1	
43	PB14	HFXTAL_N			LEU0_RX #1	
44	IOVDD_3	Digital IO power supply 3.				
45	AVDD_0	Analog power supply 0.				
46	PD0	ADC0_CH0		PCNT2_S0IN #0	US1_TX #1	
47	PD1	ADC0_CH1		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
48	PD2	ADC0_CH2		TIM0_CC1 #3	US1_CLK #1	
49	PD3	ADC0_CH3		TIM0_CC2 #3	US1_CS #1	
50	PD4	ADC0_CH4			LEU0_TX #0	
51	PD5	ADC0_CH5			LEU0_RX #0	
52	PD6	ADC0_CH6		LETIM0_OUT0 #0	I2C0_SDA #1	
53	PD7	ADC0_CH7		LETIM0_OUT1 #0	I2C0_SCL #1	
54	PD8					CMU_CLK1 #1
55	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
56	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
57	VDD_DREG	Power supply for on-chip voltage regulator.				
58	VSS	Ground.				
59	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
60	PE0			PCNT0_S0IN #1	U0_TX #1	
61	PE1			PCNT0_S1IN #1	U0_RX #1	
62	PE2					ACMP0_O #1

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PA5	LCD_SEG18	TIM0_CDTI2 #0	LEU1_TX #1	
6	PA6	LCD_SEG19		LEU1_RX #1	
8	IOVDD_0	Digital IO power supply 0.			
9	PB3	LCD_SEG20	PCNT1_S0IN #1	US2_TX #1	
10	PB4	LCD_SEG21	PCNT1_S1IN #1	US2_RX #1	
11	PB5	LCD_SEG22		US2_CLK #1	
12	PB6	LCD_SEG23		US2_CS #1	
13	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
14	PC5	ACMP0_CH5	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
15	PB7	LFXTAL_P		US1_CLK #0	
16	PB8	LFXTAL_N		US1_CS #0	
17	PA12	LCD_BCAP_P	TIM2_CC0 #1		
18	PA13	LCD_BCAP_N	TIM2_CC1 #1		
19	PA14	LCD_BEXT	TIM2_CC2 #1		
20	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
22	PB12	DAC0_OUT1	LETIM0_OUT1 #1		
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		LEU0_TX #1	
25	PB14	HFXTAL_N		LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	
31	PD3	ADC0_CH3	TIM0_CC2 #3	US1_CS #1	
32	PD4	ADC0_CH4		LEU0_TX #0	
33	PD5	ADC0_CH5		LEU0_RX #0	
34	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
35	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
36	PD8				CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM0_CC0	PA0	PA0		PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12			Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13			Timer 2 Capture Compare input / output channel 1.
TIM2_CC2		PA14			Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12	PE5			USART0 clock input / output.
US0_CS	PE13	PE4			USART0 chip select input / output.
US0_RX	PE11	PE6			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7			USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX		PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX		PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX		PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX		PB3			USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.9 EFM32G880 (LQFP100)

5.9.1 Pinout

The EFM32G880 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

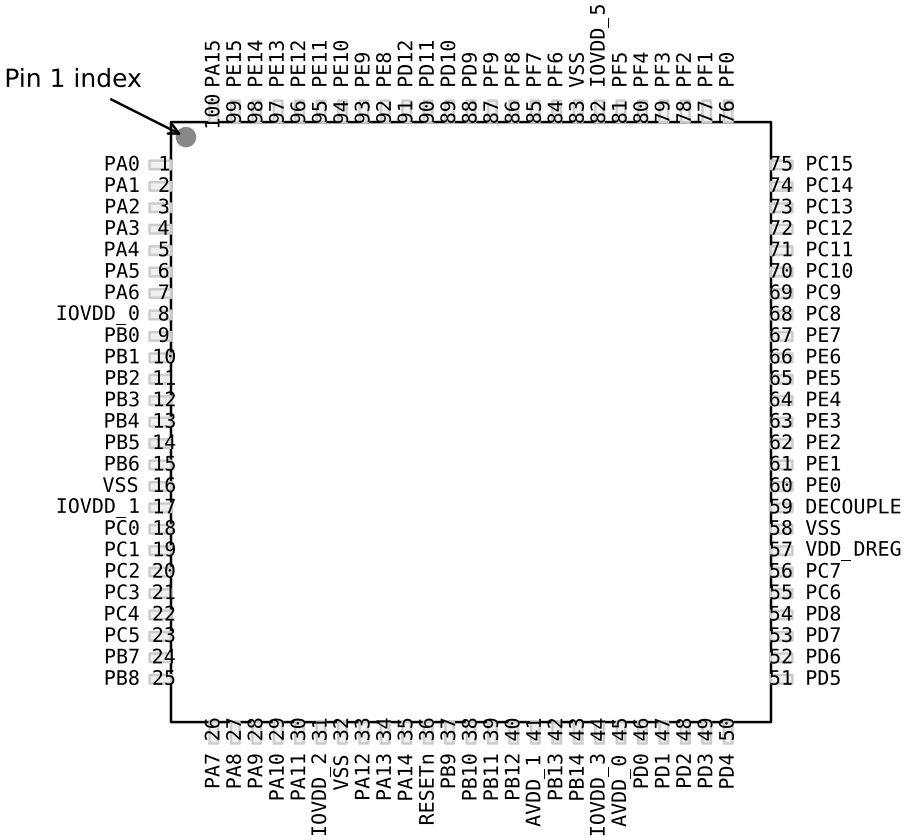

Figure 5.9. EFM32G880 Pinout (top view, not to scale)

Table 5.25. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0	LCD_SEG 13	EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1	LCD_SEG 14	EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2	LCD_SEG 15	EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
53	PD7	ADC0_CH7		LETIM0_OUT1 #0	I2C0_SCL #1	
54	PD8					CMU_CLK1 #1
55	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
56	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
57	VDD_DREG	Power supply for on-chip voltage regulator.				
58	VSS	Ground.				
59	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
60	PE0			PCNT0_S0IN #1	U0_TX #1	
61	PE1			PCNT0_S1IN #1	U0_RX #1	
62	PE2					ACMP0_O #1
63	PE3					ACMP1_O #1
64	PE4	LCD_COM0			US0_CS #1	
65	PE5	LCD_COM1			US0_CLK #1	
66	PE6	LCD_COM2			US0_RX #1	
67	PE7	LCD_COM3			US0_TX #1	
68	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
69	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
70	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
71	PC11	ACMP1_CH3			US0_TX #2	
72	PC12	ACMP1_CH4				CMU_CLK0 #1
73	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
74	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
75	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
76	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1

5.9.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G880 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.27. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	—	—	—	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A4	PE9	LCD_SEG 5	EBI_AD01 #0	PCNT2_S1IN #1		
A5	PD10	LCD_SEG 29	EBI_CS1 #0			
A6	PF7	LCD_SEG 25		TIM0_CC1 #2	U0_RX #0	
A7	PF5	LCD_SEG 3	EBI_REn #0	TIM0_CDTI2 #2		
A8	PF4	LCD_SEG 2	EBI_WEn #0	TIM0_CDTI1 #2		
A9	PE4	LCD_COM 0			US0_CS #1	
A10	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
A11	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
B1	PA15	LCD_SEG 12	EBI_AD08 #0			
B2	PE13	LCD_SEG 9	EBI_AD05 #0		US0_CS #0	ACMP0_O #0
B3	PE11	LCD_SEG 7	EBI_AD03 #0	TIM1_CC1 #1	US0_RX #0	BOOT_RX
B4	PE8	LCD_SEG 4	EBI_AD00 #0	PCNT2_S0IN #1		
B5	PD11	LCD_SEG 30	EBI_CS2 #0			
B6	PF8	LCD_SEG 26		TIM0_CC2 #2		
B7	PF6	LCD_SEG 24		TIM0_CC0 #2	U0_TX #0	
B8	PF3	LCD_SEG 1	EBI_ALE #0	TIM0_CDTI0 #2		
B9	PE5	LCD_COM 1			US0_CLK #1	
B10	PC12	ACMP1_CH4				CMU_CLK0 #1
B11	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
C1	PA1	LCD_SEG 14	EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
C2	PA0	LCD_SEG 13	EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	

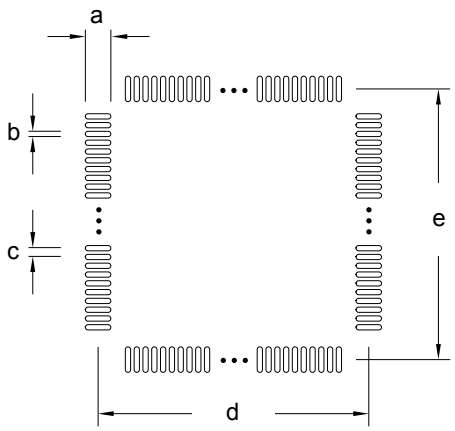

Figure 9.4. TQFP48 PCB Stencil Design

Table 9.4. TQFP48 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.50
b	0.20
c	0.50
d	8.50
e	8.50

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see 5. Pin Definitions.

13.2 Revision 2.00

May 10th, 2017

Consolidated all EFM32G data sheets:

- EFM32G200
- EFM32G210
- EFM32G222
- EFM32G230
- EFM32G232
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G842
- EFM32G880
- EFM32G890

New formatting throughout.

Added 1. Feature List.

Updated ordering codes in 2. Ordering Information for Revision E and tape and reel.

Added Figure 2.1 Ordering Code Decoder on page 5.

Separated Memory Map figure into Figure 3.2 System Address Space with Core and Code Space Listing on page 27 and Figure 3.3 System Address Space with Peripheral Listing on page 28 for readability.

Removed footnote for storage temperature range in 4.2 Absolute Maximum Ratings.

In 4.6 Power Management:

- Updated EM0 condition for $V_{BODextthr-}$ specification.
- Added $V_{BODextthr-}$ in EM1 and EM2 specifications.
- Updated EM0 condition for $V_{BODextthr+}$ specification.

Updated Flash page erase time and device erase time in 4.7 Flash and added footnotes.

Updated figures in 4.9.3 LFRCO.

Updated figures and HFRCO current consumption typical values in 4.9.4 HFRCO.

In 4.10 Analog Digital Converter (ADC):

- Updated test conditions, updated specifications, and added footnote for average active current.
- Added input bias current.
- Added input offset current.
- Updated ADC clock frequency.
- Updated SNR, SINAD and SFDR.
- Updated offset voltage.
- Updated missing codes.
- Added gain error drift and offset error drift.
- Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

In 4.11 Digital Analog Converter (DAC):

- Updated I_{DAC} parameter, test conditions, and footnote.
- Added DAC load current specification to 4.11 Digital Analog Converter (DAC).
- Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

Updated ACMP active current (BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register) typical value in 4.12 Analog Comparator (ACMP).

Updated VCMP hysteresis typical value in 4.13 Voltage Comparator (VCMP).