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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g880f64g-e-qfp100r

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3. System Overview

3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32G devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32G Reference Manual.

The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.





3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32G Reference Manual.

3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.2.11 EFM32G890

The features of the EFM32G890 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
12C0	Full configuration	12C0_SDA, 12C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 57)

Table 3.11. EFM32G890 Configuration Summary

4.4.1 EM0 Current Consumption



Figure 4.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28 MHz

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Spurious-Free Dynamic Range (SFDR)	SFDR _{ADC}	200 kSamples/s, 12 bit, differen- tial, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	68	79	_	dBc
		200 kSamples/s, 12 bit, differen- tial, 2xV _{DD} reference,ADC_CLK = 7 MHz, BIASPROG = 0x747	_	79	_	dBc
Offset voltage	VADCOFFSET	After calibration, single-ended	—	0.3	_	mV
		After calibration, differential	-4	0.3	4	mV
Thermometer output gradient	TGRAD _{ADCTH}		—	-1.92	_	mV/°C
			_	-6.3		ADC Co- des/°C
Differential non-linearity (DNL)	DNL _{ADC}	V _{DD} = 3.0 V, external 2.5 V reference	-1	±0.7	4	LSB
Integral non-linearity (INL), End point method	INL _{ADC}	V _{DD} = 3.0 V, external 2.5 V reference	—	±1.2	±3	LSB
Missing codes	MC _{ADC}		—	—	3	LSB
Gain error drift	GAIN _{ED}	1.25 V reference	_	0.01 ²	0.033 ³	%/°C
		2.5 V reference		0.01 ²	0.03 ³	%/°C
Offset error drift	OFFSET _{ED}	1.25 V reference		0.00 ²	0.06 ³	LSB/°C
		2.5 V reference	_	0.00 ²	0.04 ³	LSB/°C
VREF voltage	V _{REF}	1.25 V reference	1.2	1.25	1.3	V
		2.5 V reference	2.4	2.5	2.6	V
VREF voltage drift	V _{REF_VDRIFT}	1.25 V reference	-12.4	2.9	18.2	mV/V
		2.5 V reference, VDD > 2.5 V	-24.6	5.7	35.2	mV/V
VREF temperature drift	V _{REF_TDRIFT}	1.25 V reference	-132	272	677	μV/°C
		2.5 V reference	-231	545	1271	μV/°C
VREF current consumption	I _{VREF}	1.25 V reference	—	67	114	μA
		2.5 V reference	—	55	82	μA
ADC and DAC VREF matching	V _{REF_MATCH}	1.25 V reference	_	99.85	_	%
		2.5 V reference	_	100.01	_	%

Note:

1. Includes required contribution from the voltage reference.

2. Typical numbers given by abs(Mean) / (85 - 25).

3. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in the following figures.



Figure 4.31. ADC Differential Linearity Error vs Code, VDD = 3V, Temp = 25°C

Alternate					LOCATION
Functionality	0	1	2	3	Description
					Debug-interface Serial Wire viewer Output.
DBG_SWO	PF2	PC15			Note that this function is not enabled after reset, and must be enabled by software to be used.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7			I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1		Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14			LEUART0 Receive input.
LEU0_TX	PD4	PB13			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4				Pulse Counter PCNT1 input number 0.
TIM0_CC0	PA0	PA0			Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0		PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8		PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9		PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10		PC10		Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12		PC9		USART0 clock input / output.
US0_CS	PE13		PC8		USART0 chip select input / output.
					USART0 Asynchronous Receive.
US0_RX	PE11		PC10		USART0 Synchronous mode Master Input / Slave Output (MI-SO).

5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G280 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	_	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	_	_	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	_		_	_	_	_	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

Table 5.15. GPIO Pinout

5.6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Alternate					LOCATION
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2			Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_0	PF2	PE3			Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.

Table 5.17. Alternate functionality overview

LQFP100 Pin# and Name			Pi	Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other		
53	PD7	ADC0_CH 7		LETIM0_OUT1 #0	I2C0_SCL #1			
54	PD8					CMU_CLK1 #1		
55	PC6	ACMP0_C H6			LEU1_TX #0 I2C0_SDA #2			
56	PC7	ACMP0_C H7			LEU1_RX #0 I2C0_SCL #2			
57	VDD_DRE G	Power supp	ly for on-chip voltage reg	ulator.				
58	VSS	Ground.						
59	DECOU- PLE	Decouple or	utput for on-chip voltage r	egulator. An external capa	acitance of size C _{DECOUP}	LE is required at this pin.		
60	PE0			PCNT0_S0IN #1	U0_TX #1			
61	PE1			PCNT0_S1IN #1	U0_RX #1			
62	PE2					ACMP0_O #1		
63	PE3					ACMP1_O #1		
64	PE4	LCD_COM 0			US0_CS #1			
65	PE5	LCD_COM 1			US0_CLK #1			
66	PE6	LCD_COM 2			US0_RX #1			
67	PE7	LCD_COM 3			US0_TX #1			
68	PC8	ACMP1_C H0		TIM2_CC0 #2	US0_CS #2			
69	PC9	ACMP1_C H1		TIM2_CC1 #2	US0_CLK #2			
70	PC10	ACMP1_C H2		TIM2_CC2 #2	US0_RX #2			
71	PC11	ACMP1_C H3			US0_TX #2			
72	PC12	ACMP1_C H4				CMU_CLK0 #1		
73	PC13	ACMP1_C H5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0				
74	PC14	ACMP1_C H6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3			
75	PC15	ACMP1_C H7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1		
76	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1		

Alternate					LOCATION
Functionality	0	1	2	3	Description
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		I2C0 Serial Data input / output.
LCD_BCAP_N	PA13				LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12				LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14				LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4				LCD driver common line number 0.
LCD_COM1	PE5				LCD driver common line number 1.
LCD_COM2	PE6				LCD driver common line number 2.
LCD_COM3	PE7				LCD driver common line number 3.
LCD_SEG0	PF2				LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3				LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4				LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5				LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8				LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9				LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10				LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.

BGA11	2 Pin# and Name	Pin Alternate Functionality / Description					
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other	
C3	PE10	LCD_SEG 6	EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	BOOT_TX	
C4	PD13						
C5	PD12	LCD_SEG 31	EBI_CS3 #0				
C6	PF9	LCD_SEG 27					
C7	VSS	Ground.					
C8	PF2	LCD_SEG 0	EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0	
C9	PE6	LCD_COM 2			US0_RX #1		
C10	PC10	ACMP1_C H2		TIM2_CC2 #2	US0_RX #2		
C11	PC11	ACMP1_C H3			US0_TX #2		
D1	PA3	LCD_SEG 16	EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2		
D2	PA2	LCD_SEG 15	EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0	
D3	PB15						
D4	VSS	Ground.					
D5	IOVDD_6	Digital IO po	ower supply 6.				
D6	PD9	LCD_SEG 28	EBI_CS0 #0				
D7	IOVDD_5	Digital IO po	ower supply 5.				
D8	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1	
D9	PE7	LCD_COM 3			US0_TX #1		
D10	PC8	ACMP1_C H0		TIM2_CC0 #2	US0_CS #2		
D11	PC9	ACMP1_C H1		TIM2_CC1 #2	US0_CLK #2		
E1	PA6	LCD_SEG 19	EBI_AD15 #0		LEU1_RX #1		
E2	PA5	LCD_SEG 18	EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1		
E3	PA4	LCD_SEG 17	EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2		
E4	PB0	LCD_SEG 32		TIM1_CC0 #2			
E8	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1	

8.3 TQFP64 Package Marking

In the illustration below package fields and position are shown.



Figure 8.5. Example Chip Marking (Top View)

9.2 TQFP48 PCB Layout



Figure 9.2. TQFP48 PCB Land Pattern



Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
а	1.60	P1	1	P6	36
b	0.30	P2	12	P7	37
с	0.50	P3	13	P8	48
d	8.50	P4	24		
е	8.50	P5	25		



Figure 9.3. TQFP48 PCB Solder Mask

Table 9.3. TQFP48 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.72
b	0.42
C	0.50
d	8.50
e	8.50

9.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.





10. QFN64 Package Specifications

10.1 QFN64 Package Dimensions



Figure 10.1. QFN64

Note:

- 1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
- 2. All dimensions are in millimeters. Angles are in degrees.
- 3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm isacceptable.
- 4. Coplanarity applies to the exposed heat slug as well as the terminal.
- 5. Radius on terminal is optional.

Table 10.1.	QFN64	(Dimensions	in mm)
-------------	-------	-------------	--------

Symbol	Min	Nom	Мах
A	0.80	0.85	0.90
A1	0.00	_	0.05
A3	0.203 REF		
b	0.25	0.30	0.35
D	9.00 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30

Symbol	Dim. (mm)	Symbol	Dim. (mm)
d	8.90	_	-





Table 10.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
а	0.75	e	8.90
b	0.22	x	2.70
С	0.50	У	2.70
d	8.90	Z	0.80

Note:

- 1. The drawings are not to scale.
- 2. All dimensions are in millimeters.
- 3. All drawings are subject to change without notice.
- 4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
- 5. Stencil thickness 0.125 mm.
- 6. For detailed pin-positioning, see Pin Definitions.

10.3 QFN64 Package Marking

In the illustration below package fields and position are shown.



Figure 10.5. Example Chip Marking (Top View)

11.2 QFN32 PCB Layout



Figure 11.2. QFN32 PCB Land Pattern



Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
а	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
С	0.65	P3	9	P8	32
d	6.00	P4	16	P9	33
e	6.00	P5	17		
f	4.40				
g	4.40				



Figure 11.3. QFN32 PCB Solder Mask

Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
а	0.92
b	0.47
C	0.65

13.11 Revision 1.20

December 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Increased max storage temperature.

Added data for <150°C and <70°C on Flash data retention.

Changed latch-up sensitivity test description.

Added IO leakage current.

For LQFP100 devices, updated ESD CDM value.

Added Flash current consumption.

Updated HFRCO data.

Updated LFRCO data.

Added graph for ADC Absolute Offset over temperature.

Added graph for ADC Temperature sensor readout.

13.12 Revision 1.11

November 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Corrected maximum DAC clock speed for continuous mode.

Added DAC sample-hold mode voltage drift rate.

Added pulse widths detected by the HFXO glitch detector.

Added power sequencing information to Power Management section.

13.15 Revision 0.90

This revision applies the following devices:

• EFM32G222

Initial preliminary revision, April 14th, 2011

This revision applies the following devices:

- EFM32G232
- EFM32G842

Initial preliminary revision, June 30th, 2011

13.16 Revision 0.85

February 19th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Renamed DBG_SWV pin to DBG_SWO.

13.17 Revision 0.84

February 11th, 2010

This revision applies the following devices:

- EFM32G230
- EFM32G840

Corrected pinout tables.

13.18 Revision 0.83

January 25th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Updated errata section.

Specified flash word width in Flash Electrical Characteristics.

Added Capacitive Sense Internal Resistor values in ACMP Electrical Characteristics.