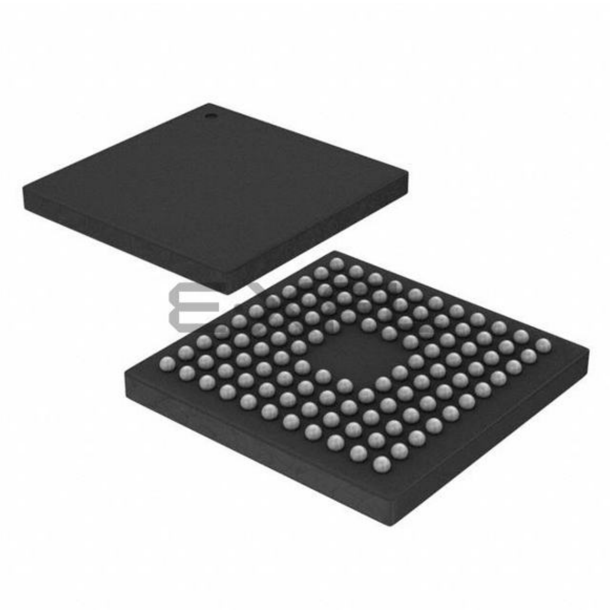

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	90
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g890f128-bga112

3.2.8 EFM32G840

The features of the EFM32G840 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.8. EFM32G840 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:4], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:4], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 57)
LCD	Full configuration	LCD_SEG[23:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

Module	Configuration	Pin Connections
LCD	Full configuration	LCD_SEG[39:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	200 kSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	68	79	—	dBc
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference,ADC_CLK = 7 MHz, BIASPROG = 0x747	—	79	—	dBc
Offset voltage	$V_{ADCOFFSET}$	After calibration, single-ended	—	0.3	—	mV
		After calibration, differential	-4	0.3	4	mV
Thermometer output gradient	$TGRAD_{ADCTH}$		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes/°C
Differential non-linearity (DNL)	DNL_{ADC}	V_{DD}= 3.0 V, external 2.5 V reference	-1	±0.7	4	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	V_{DD}= 3.0 V, external 2.5 V reference	—	±1.2	±3	LSB
Missing codes	MC_{ADC}		—	—	3	LSB
Gain error drift	$GAIN_{ED}$	1.25 V reference	—	0.01[2]	0.033[3]	%/°C
		2.5 V reference	—	0.01[2]	0.03[3]	%/°C
Offset error drift	$OFFSET_{ED}$	1.25 V reference	—	0.00[2]	0.06[3]	LSB/°C
		2.5 V reference	—	0.00[2]	0.04[3]	LSB/°C
VREF voltage	V_{REF}	1.25 V reference	1.2	1.25	1.3	V
		2.5 V reference	2.4	2.5	2.6	V
VREF voltage drift	V_{REF_VDRIFT}	1.25 V reference	-12.4	2.9	18.2	mV/V
		2.5 V reference, VDD > 2.5 V	-24.6	5.7	35.2	mV/V
VREF temperature drift	V_{REF_TDRIFT}	1.25 V reference	-132	272	677	µV/°C
		2.5 V reference	-231	545	1271	µV/°C
VREF current consumption	I_{VREF}	1.25 V reference	—	67	114	µA
		2.5 V reference	—	55	82	µA
ADC and DAC VREF matching	V_{REF_MATCH}	1.25 V reference	—	99.85	—	%
		2.5 V reference	—	100.01	—	%

Note:
1. Includes required contribution from the voltage reference.
2. Typical numbers given by abs(Mean) / (85 - 25).
3. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in the following figures.

4.14 LCD

Table 4.18. LCD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frame rate	f_{LCDFR}		30	—	200	Hz
Number of segments supported	NUM_{SEG}		—	4×40	—	seg
LCD supply voltage range	V_{LCD}	Internal boost circuit enabled	2.0	—	3.8	V
Steady state current consumption.	I_{LCD}	Display disconnected, static mode, framerate 32 Hz, all segments on.	—	250	—	nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONE-THIRD in LCD_DISPCTRL register.	—	550	—	nA
Steady state Current contribution of internal boost.	$I_{LCDBOOST}$	Internal voltage boost off	—	0	—	µA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.	—	8.4	—	µA
Boost Voltage	V_{BOOST}	VBLEV of LCD_DISPCTRL register to LEVEL0	—	3.0	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL1	—	3.08	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL2	—	3.17	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL3	—	3.26	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL4	—	3.34	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL5	—	3.43	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL6	—	3.52	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL7	—	3.6	—	V

The total LCD current is given by the following equation. $I_{LCDBOOST}$ is zero if internal boost is off.

$$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST}$$

4.15 I2C

Table 4.19. I2C Standard-mode (Sm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	100[1]	kHz
SCL clock low time	t_{LOW}	4.7	—	—	µs
SCL clock high time	t_{HIGH}	4.0	—	—	µs
SDA set-up time	$t_{SU,DAT}$	250	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	3450[2,3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	4.0	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	4.0	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	4.7	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32G Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < $((3450 \cdot 10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 4.20. I2C Fast-mode (Fm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	400[1]	kHz
SCL clock low time	t_{LOW}	1.3	—	—	µs
SCL clock high time	t_{HIGH}	0.6	—	—	µs
SDA set-up time	$t_{SU,DAT}$	100	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	900[2,3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.6	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.6	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.6	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	1.3	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32G Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < $((900 \cdot 10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 4).

5.2 EFM32G222 (TQFP48)

5.2.1 Pinout

The EFM32G222 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

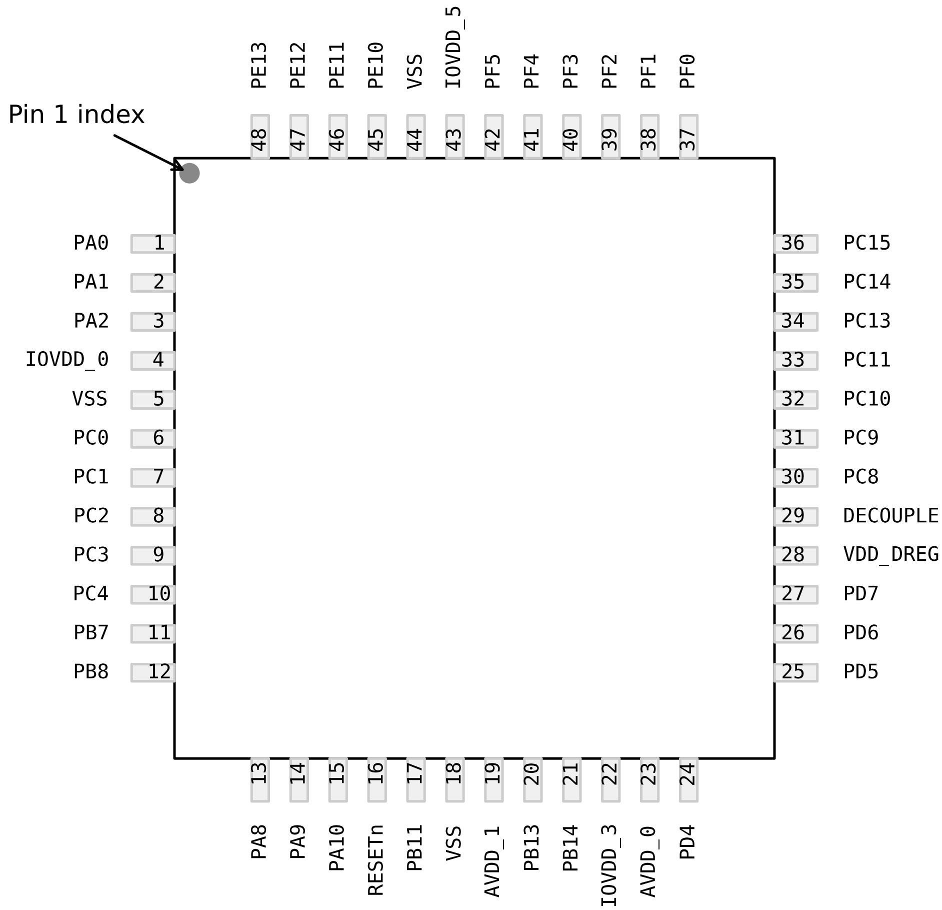

Figure 5.2. EFM32G222 Pinout (top view, not to scale)

Table 5.4. Device Pinout

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_0	Digital IO power supply 0.			
5	VSS	Ground.			

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
7	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
8	PC2	ACMP0_CH2			
9	PC3	ACMP0_CH3			
10	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0		
11	PB7	LFXTAL_P		US1_CLK #0	
12	PB8	LFXTAL_N		US1_CS #0	
13	PA8		TIM2_CC0 #0		
14	PA9		TIM2_CC1 #0		
15	PA10		TIM2_CC2 #0		
16	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
17	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
18	VSS	Ground.			
19	AVDD_1	Analog power supply 1.			
20	PB13	HFXTAL_P		LEU0_TX #1	
21	PB14	HFXTAL_N		LEU0_RX #1	
22	IOVDD_3	Digital IO power supply 3.			
23	AVDD_0	Analog power supply 0.			
24	PD4	ADC0_CH4		LEU0_TX #0	
25	PD5	ADC0_CH5		LEU0_RX #0	
26	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
27	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
28	VDD_DREG	Power supply for on-chip voltage regulator.			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
30	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
31	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
32	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
33	PC11	ACMP1_CH3		US0_TX #2	
34	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
35	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
36	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
37	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
38	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
39	PF2				ACMP1_O #0 DBG_SWO #0
40	PF3		TIM0_CDTI0 #2		
41	PF4		TIM0_CDTI1 #2		
42	PF5		TIM0_CDTI2 #2		
43	IOVDD_5	Digital IO power supply 5.			
44	VSS	Ground.			
45	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
46	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX
47	PE12		TIM1_CC2 #1	US0_CLK #0	
48	PE13			US0_CS #0	ACMP0_O #0

5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.5. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1				Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
44	PC11	ACMP1_CH3		US0_TX #2	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2				ACMP1_O #0 DBG_SWO #0
52	PF3		TIM0_CDTI0 #2		
53	PF4		TIM0_CDTI1 #2		
54	PF5		TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	PE8		PCNT2_S0IN #1		
57	PE9		PCNT2_S1IN #1		
58	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX
60	PE12		TIM1_CC2 #1	US0_CLK #0	
61	PE13			US0_CS #0	ACMP0_O #0
62	PE14			LEU0_TX #2	
63	PE15			LEU0_RX #2	
64	PA15				

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A6	PF7			TIM0_CC1 #2	U0_RX #0	
A7	PF5		EBI_REn #0	TIM0_CDTI2 #2		
A8	PF4		EBI_WEn #0	TIM0_CDTI1 #2		
A9	PE4				US0_CS #1	
A10	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
A11	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
B1	PA15		EBI_AD08 #0			
B2	PE13		EBI_AD05 #0		US0_CS #0	ACMP0_O #0
B3	PE11		EBI_AD03 #0	TIM1_CC1 #1	US0_RX #0	BOOT_RX
B4	PE8		EBI_AD00 #0	PCNT2_S0IN #1		
B5	PD11		EBI_CS2 #0			
B6	PF8			TIM0_CC2 #2		
B7	PF6			TIM0_CC0 #2	U0_TX #0	
B8	PF3		EBI_ALE #0	TIM0_CDTI0 #2		
B9	PE5				US0_CLK #1	
B10	PC12	ACMP1_CH4				CMU_CLK0 #1
B11	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
C1	PA1		EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
C2	PA0		EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	
C3	PE10		EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					
C5	PD12		EBI_CS3 #0			
C6	PF9					
C7	VSS	Ground.				
C8	PF2		EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
C9	PE6				US0_RX #1	
C10	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
C11	PC11	ACMP1_CH3			US0_TX #2	
D1	PA3		EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
D2	PA2		EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0

5.7 EFM32G840 (QFN64)

5.7.1 Pinout

The EFM32G840 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

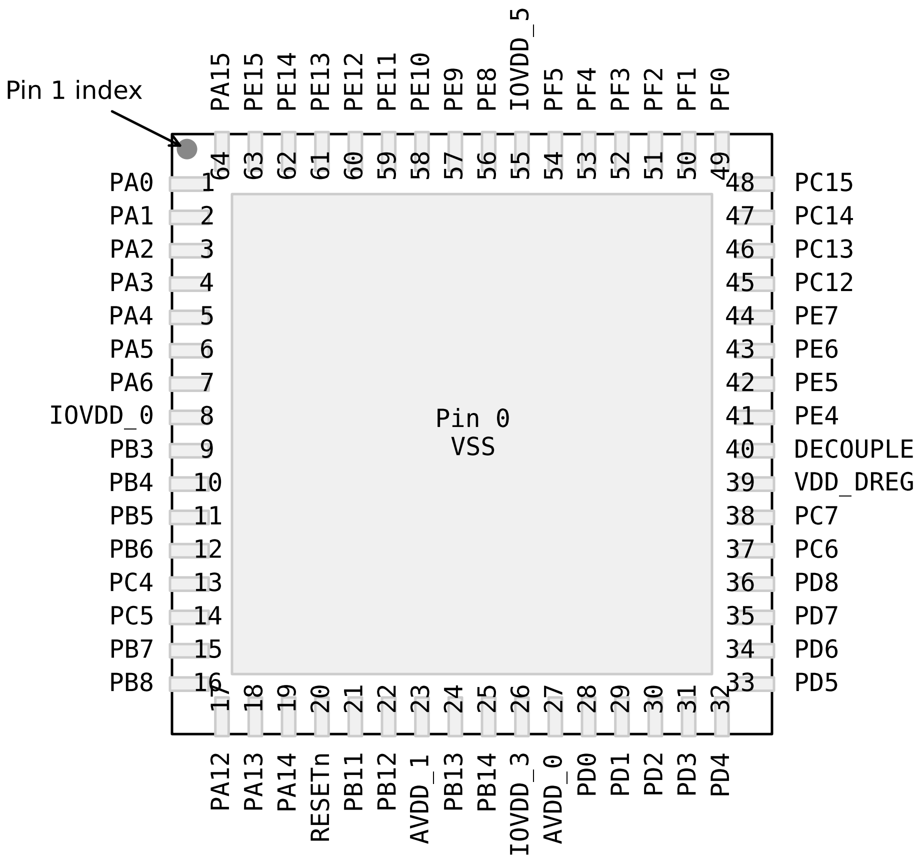

Figure 5.7. EFM32G840 Pinout (top view, not to scale)

Table 5.19. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0	LCD_SEG13	TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1	LCD_SEG14	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2	LCD_SEG15	TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3	LCD_SEG16	TIM0_CDTI0 #0		
5	PA4	LCD_SEG17	TIM0_CDTI1 #0		

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
53	PD7	ADC0_CH7		LETIM0_OUT1 #0	I2C0_SCL #1	
54	PD8					CMU_CLK1 #1
55	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
56	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
57	VDD_DREG	Power supply for on-chip voltage regulator.				
58	VSS	Ground.				
59	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
60	PE0			PCNT0_S0IN #1	U0_TX #1	
61	PE1			PCNT0_S1IN #1	U0_RX #1	
62	PE2					ACMP0_O #1
63	PE3					ACMP1_O #1
64	PE4	LCD_COM0			US0_CS #1	
65	PE5	LCD_COM1			US0_CLK #1	
66	PE6	LCD_COM2			US0_RX #1	
67	PE7	LCD_COM3			US0_TX #1	
68	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
69	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
70	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
71	PC11	ACMP1_CH3			US0_TX #2	
72	PC12	ACMP1_CH4				CMU_CLK0 #1
73	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
74	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
75	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
76	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1

Alternate	LOCATION				
Functionality	0	1	2	3	Description
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		I2C0 Serial Data input / output.
LCD_BCAP_N	PA13				LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12				LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14				LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4				LCD driver common line number 0.
LCD_COM1	PE5				LCD driver common line number 1.
LCD_COM2	PE6				LCD driver common line number 2.
LCD_COM3	PE7				LCD driver common line number 3.
LCD_SEG0	PF2				LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3				LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4				LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5				LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8				LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9				LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10				LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.

10. QFN64 Package Specifications

10.1 QFN64 Package Dimensions

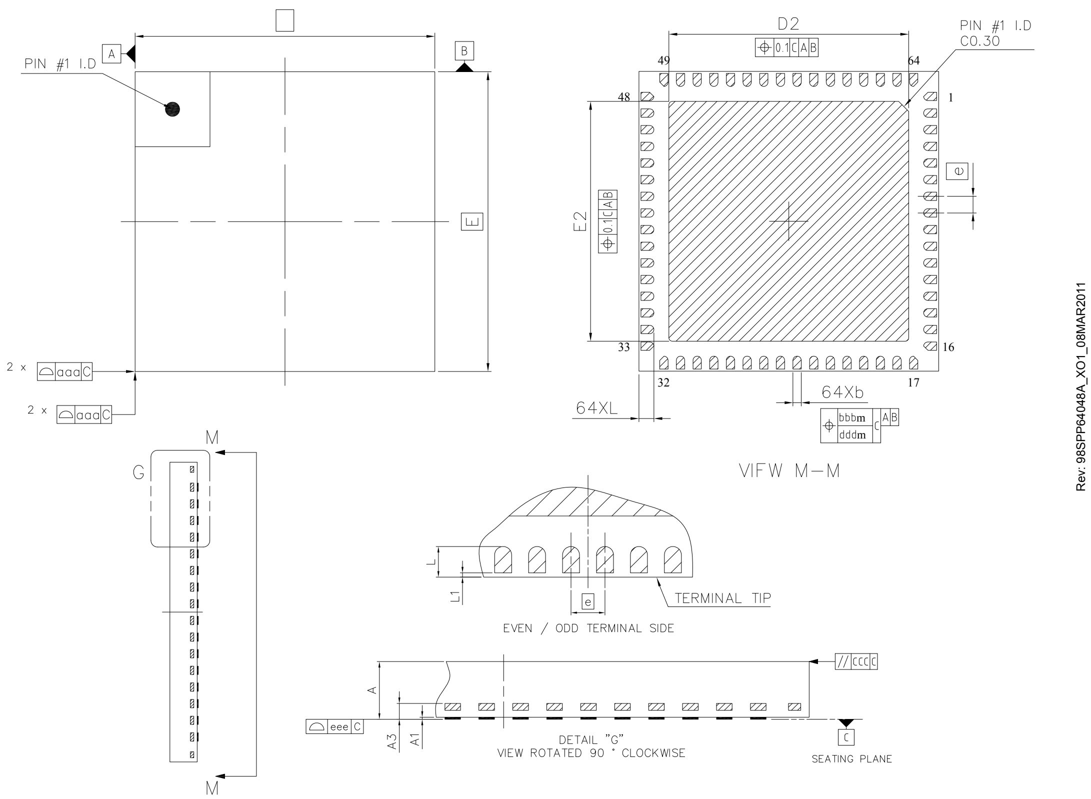

Figure 10.1. QFN64

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm fromthe terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm isacceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 10.1. QFN64 (Dimensions in mm)

Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	—	0.05
A3		0.203 REF	
b	0.25	0.30	0.35
D		9.00 BSC	
E		9.00 BSC	
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30

Symbol	Min	Nom	Max
e		0.50 BSC	
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

The QFN64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

10.3 QFN64 Package Marking

In the illustration below package fields and position are shown.

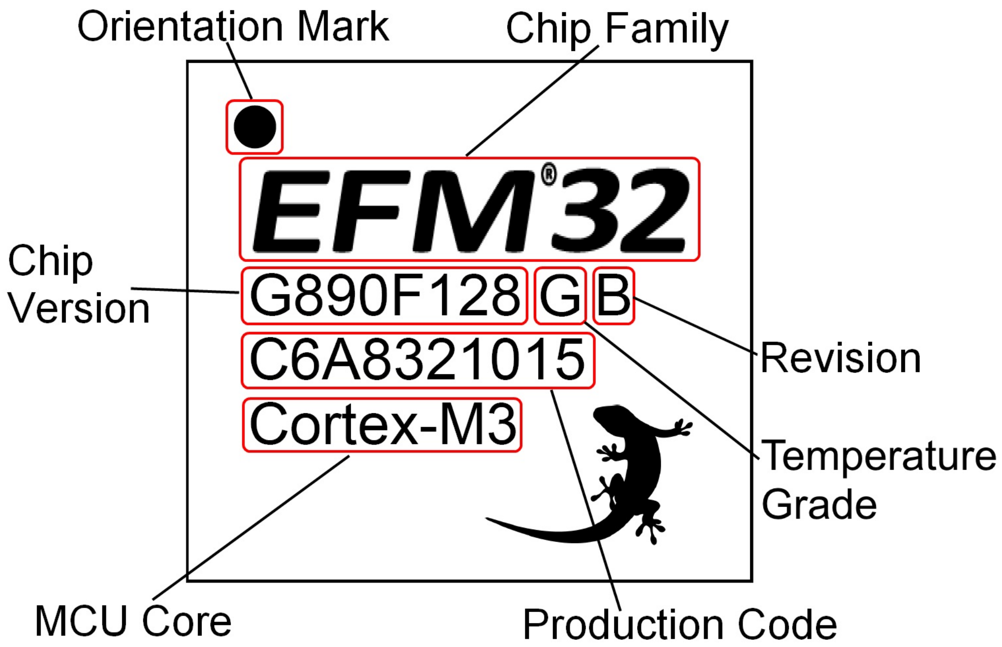

Figure 10.5. Example Chip Marking (Top View)

Symbol	Dim. (mm)
d	6.00
e	6.00
f	4.52
g	4.52

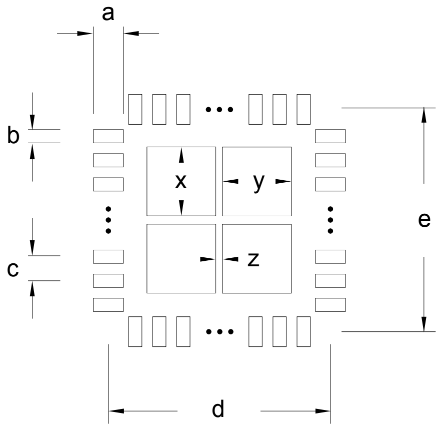

Figure 11.4. QFN32 PCB Stencil Design

Table 11.4. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.70
b	0.25
c	0.65
d	6.00
e	6.00
x	1.30
y	1.30
z	0.50

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see 5. Pin Definitions.

13.5 Revision 1.71

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

For devices with a DAC, re-added missing DAC-data.

13.6 Revision 1.70

September 30th, 2013

For devices with an I2C, added I2C characterization data.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

For devices with an ADC, corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

For QFN64 devices, updated the Max V_{ESDCDM} value to 750 V.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

13.7 Revision 1.60

June 28th, 2013

For BGA devices, updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

13.8 Revision 1.50

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

For BGA devices, corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

Other minor corrections.

13.15 Revision 0.90

This revision applies the following devices:
- EFM32G222

Initial preliminary revision, April 14th, 2011

This revision applies the following devices:
- EFM32G232
- EFM32G842

Initial preliminary revision, June 30th, 2011

13.16 Revision 0.85

February 19th, 2010

This revision applies the following devices:
- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Renamed DBG_SWV pin to DBG_SWO.

13.17 Revision 0.84

February 11th, 2010

This revision applies the following devices:
- EFM32G230
- EFM32G840

Corrected pinout tables.

13.18 Revision 0.83

January 25th, 2010

This revision applies the following devices:
- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Updated errata section.

Specified flash word width in Flash Electrical Characteristics.

Added Capacitive Sense Internal Resistor values in ACMP Electrical Characteristics.