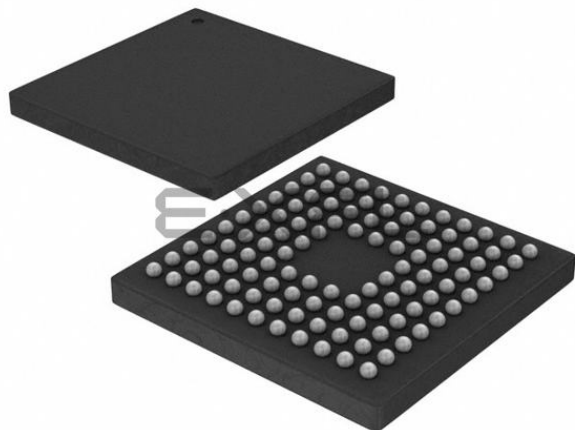




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	90
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g890f128g-e-bga112

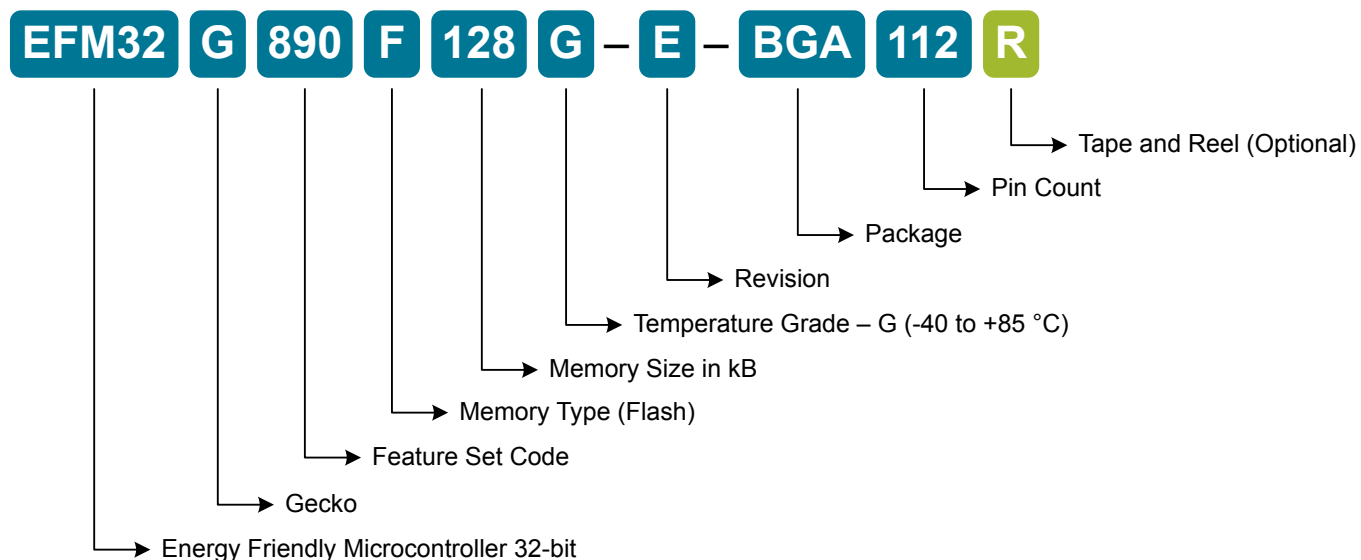


Figure 2.1. Ordering Code Decoder

Adding the suffix 'R' to the part number (e.g., EFM32G890F128G-E-BGA112R) denotes tape and reel.

Visit www.silabs.com for information on global distributors and representatives.

4.6 Power Management

The EFM32G requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 4.5. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$	EM0	1.74	—	1.96	V
		EM1	1.74	—	1.96	V
		EM2	1.74	—	1.96	V
BOD threshold on rising external supply voltage	$V_{BODextthr+}$	EM0	—	1.85	—	V
Power-on Reset (POR) threshold on rising external supply voltage	$V_{PORthr+}$		—	—	1.98	V
Delay from reset is released until program execution starts	$t_{RESETdy}$	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	μ s
negative pulse length to ensure complete reset of device	t_{RESET}		50	—	—	ns
Voltage regulator decoupling capacitor.	$C_{DECOUPLE}$	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	μ F

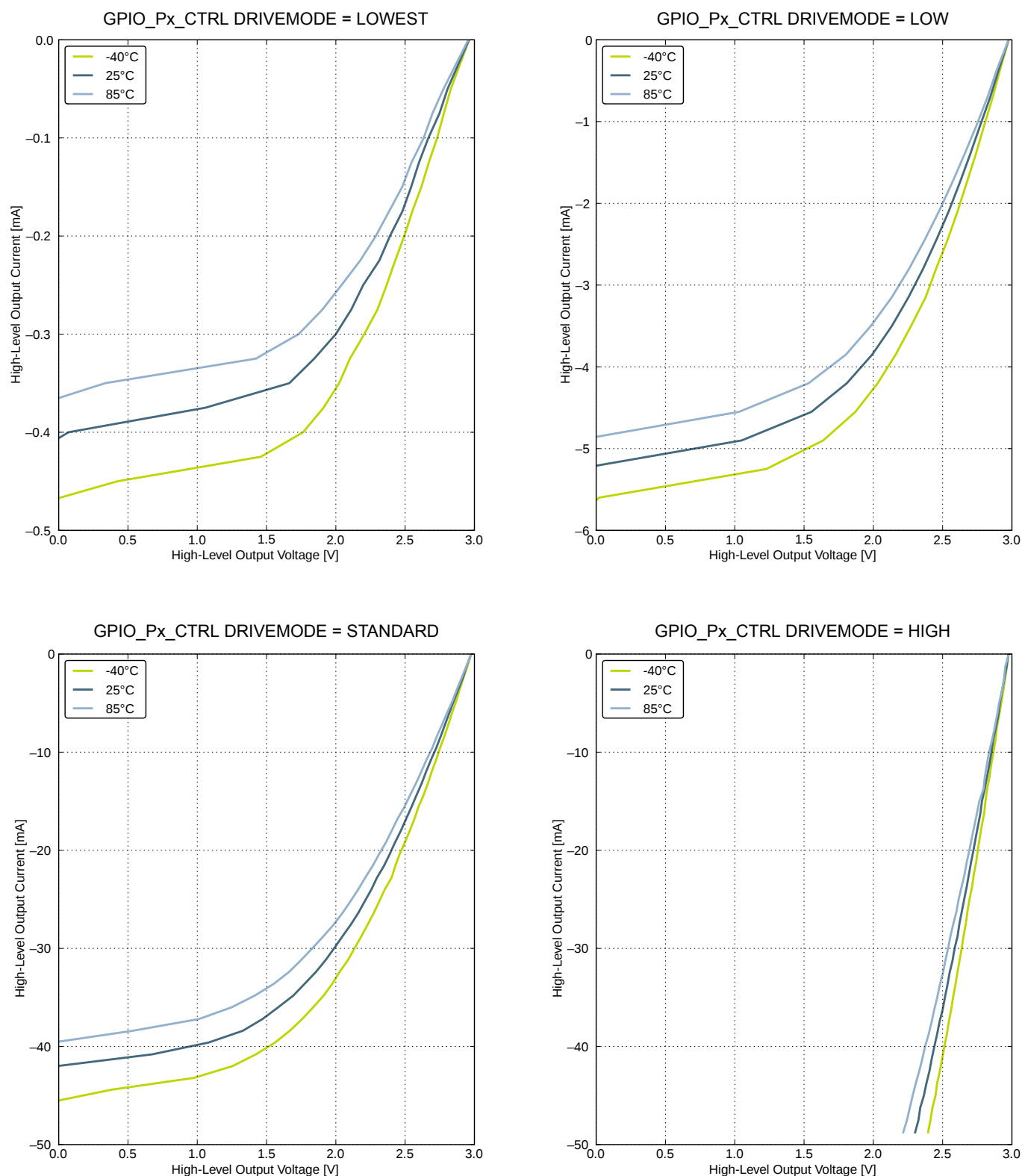


Figure 4.17. Typical High-Level Output Current, 3V Supply Voltage

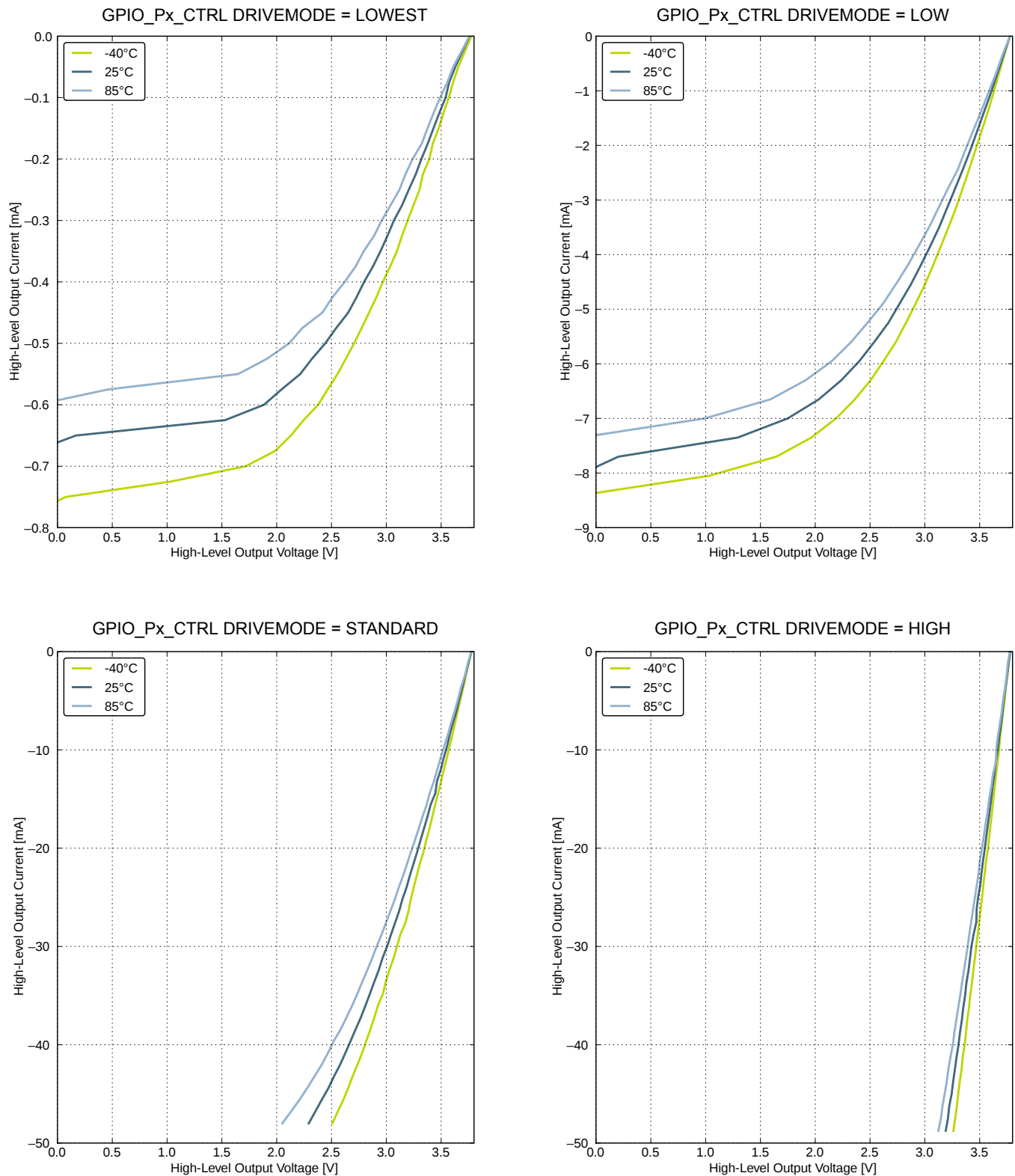


Figure 4.19. Typical High-Level Output Current, 3.8V Supply Voltage

4.9.2 HFXO

Table 4.9. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal Frequency	f_{HFXO}		4	—	32	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 32 MHz	—	30	60	Ω
		Crystal frequency 4 MHz	—	400	1500	Ω
The transconductance of the HFXO input transistor at crystal startup	g_{mHFXO}	HFXOBOOST in CMU_CTRL equals 0b11	20	—	—	mS
Supported crystal external load range	C_{HFXOL}		5	—	25	pF
Current consumption for HFXO after startup	I_{HFXO}	4 MHz: ESR=400 Ω , C_L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	85	—	μA
		32 MHz: ESR=30 Ω , C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	165	—	μA
Startup time	t_{HFXO}	32 MHz: ESR=30 Ω , C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	400	—	μs
Pulse width removed by glitch detector			1	—	4	ns

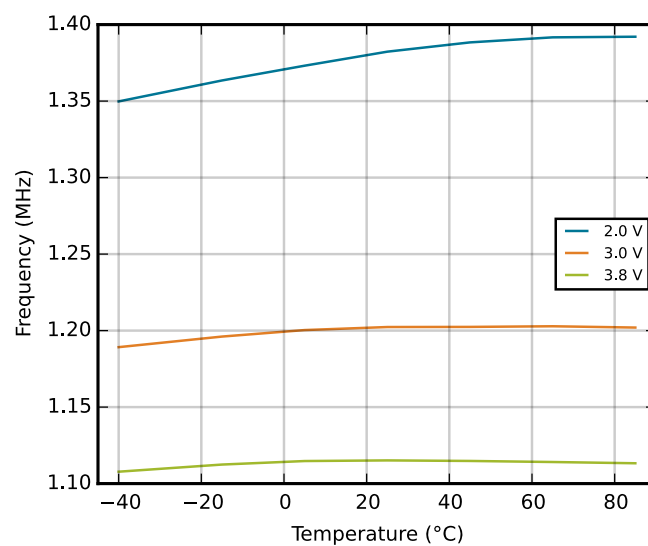
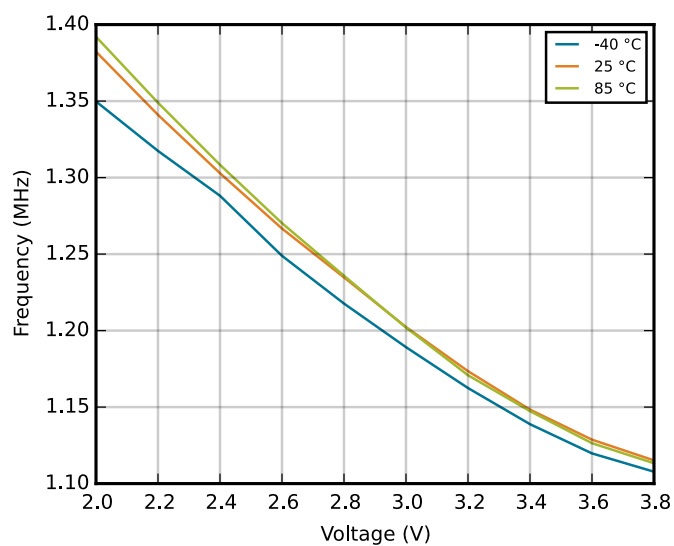


Figure 4.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

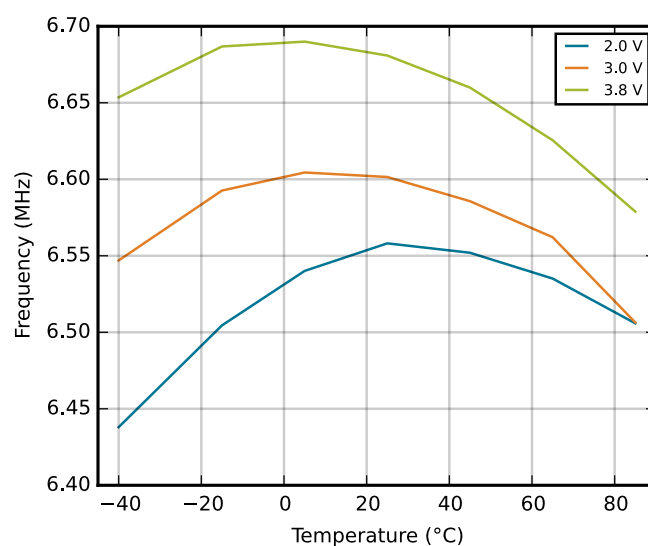
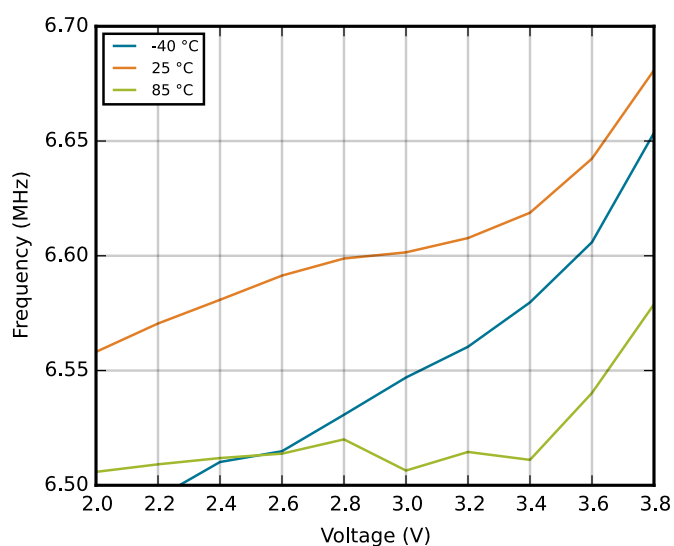


Figure 4.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

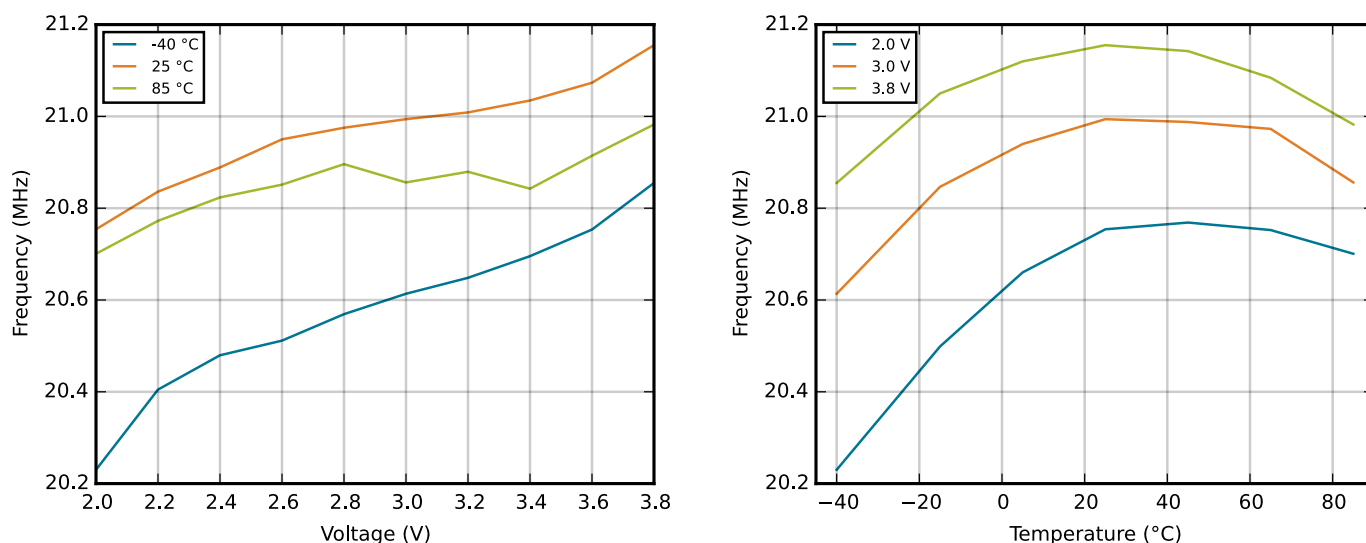


Figure 4.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

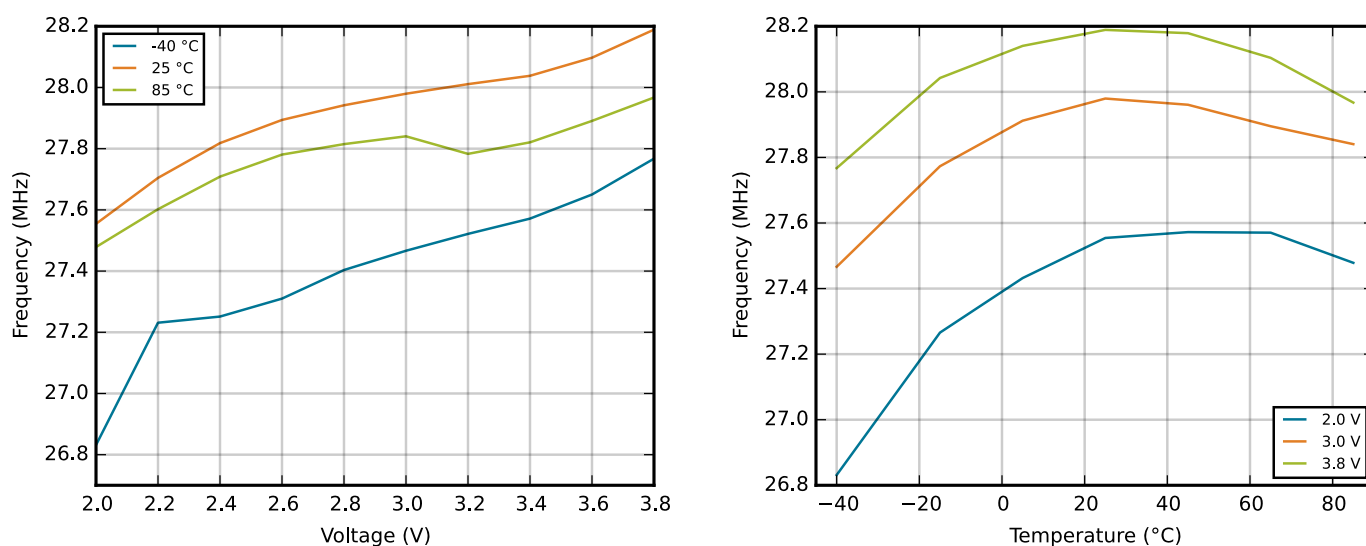


Figure 4.26. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature

4.11 Digital Analog Converter (DAC)

Table 4.15. DAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage range	V_{DACOUT}	VDD voltage reference, single-ended	0	—	V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$	—	V_{DD}	V
Output common mode voltage range	V_{DACCM}		0	—	V_{DD}	V
Average active current	I_{DAC}	500 kSamples/s, 12 bit, internal 1.25 V reference, Continuous Mode	—	400 ¹	650 ¹	μA
		100 kSamples/s, 12 bit, internal 1.25 V reference, Sample/Hold Mode	—	200 ¹	250 ¹	μA
		1 kSamples/s 12 bit, internal 1.25 V reference, Sample/Off Mode	—	17 ¹	25 ¹	μA
Sample rate	SR_{DAC}		—	—	500	ksamples/s
DAC clock frequency	f_{DAC}	Continuous Mode	—	—	1000	kHz
		Sample/Hold Mode	—	—	250	kHz
		Sample/Off Mode	—	—	250	kHz
Clock cycles per conversion	$CYC_{DACCONV}$		—	2	—	cycles
Conversion time	$t_{DACCONV}$		2	—	—	μs
Settling time	$t_{DACSETTLE}$		—	5	—	μs
Signal-to-Noise Ratio (SNR)	SNR_{DAC}	500 kSamples/s, 12 bit, single-ended, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference	—	59	—	dB
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	59	—	dB

4.13 Voltage Comparator (VCMP)

Table 4.17. VCMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{VCMPIN}		—	V_{DD}	—	V
VCMP Common Mode voltage range	V_{VCMPCM}		—	V_{DD}	—	V
Active current	I_{VCMP}	BIASPROG=0b0000 and HALF-BIAS=1 in VCMPn_CTRL register	—	0.3	1	μA
		BIASPROG=0b1111 and HALF-BIAS=0 in VCMPn_CTRL register. LPREF=0.	—	22	30	μA
Startup time reference generator	$t_{VCMPREF}$	NORMAL	—	10	—	μs
Offset voltage	$V_{VCMPOFFSET}$	Single-ended	—	10	—	mV
		Differential	—	10	—	mV
VCMP hysteresis	$V_{VCMPHYST}$		—	40	—	mV
Startup time	$t_{VCMPSTART}$		—	—	10	μs

The V_{DD} Trigger Level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{DD \text{ Trigger Level}} = 1.667V + 0.034 \times \text{TRIGLEVEL}$$

Table 4.21. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	1000 ¹	kHz
SCL clock low time	t_{LOW}	0.5	—	—	μs
SCL clock high time	t_{HIGH}	0.26	—	—	μs
SDA set-up time	$t_{SU,DAT}$	50	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26	—	—	μs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26	—	—	μs
STOP condition set-up time	$t_{SU,STO}$	0.26	—	—	μs
Bus free time between a STOP and a START condition	t_{BUF}	0.5	—	—	μs

Note:

1. For the minimum HPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32G Reference Manual.

4.16 Digital Peripherals

Table 4.22. Digital Peripherals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	7.5	—	$\mu A/MHz$
UART current	I_{UART}	UART idle current, clock enabled	—	5.63	—	$\mu A/MHz$
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	150	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	6.25	—	$\mu A/MHz$
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	8.75	—	$\mu A/MHz$
LETIMER current	$I_{LETIMER}$	LETIMER idle current, clock enabled	—	150	—	nA
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	100	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	100	—	nA
LCD current	I_{LCD}	LCD idle current, clock enabled	—	100	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	2.5	—	$\mu A/MHz$
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	5.31	—	$\mu A/MHz$
EBI current	I_{EBI}	EBI idle current, clock enabled	—	1.56	—	$\mu A/MHz$
PRS current	I_{PRS}	PRS idle current	—	2.81	—	$\mu A/MHz$
DMA current	I_{DMA}	Clock enable	—	8.12	—	$\mu A/MHz$

Note: Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32G.

5.2 EFM32G222 (TQFP48)

5.2.1 Pinout

The EFM32G222 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

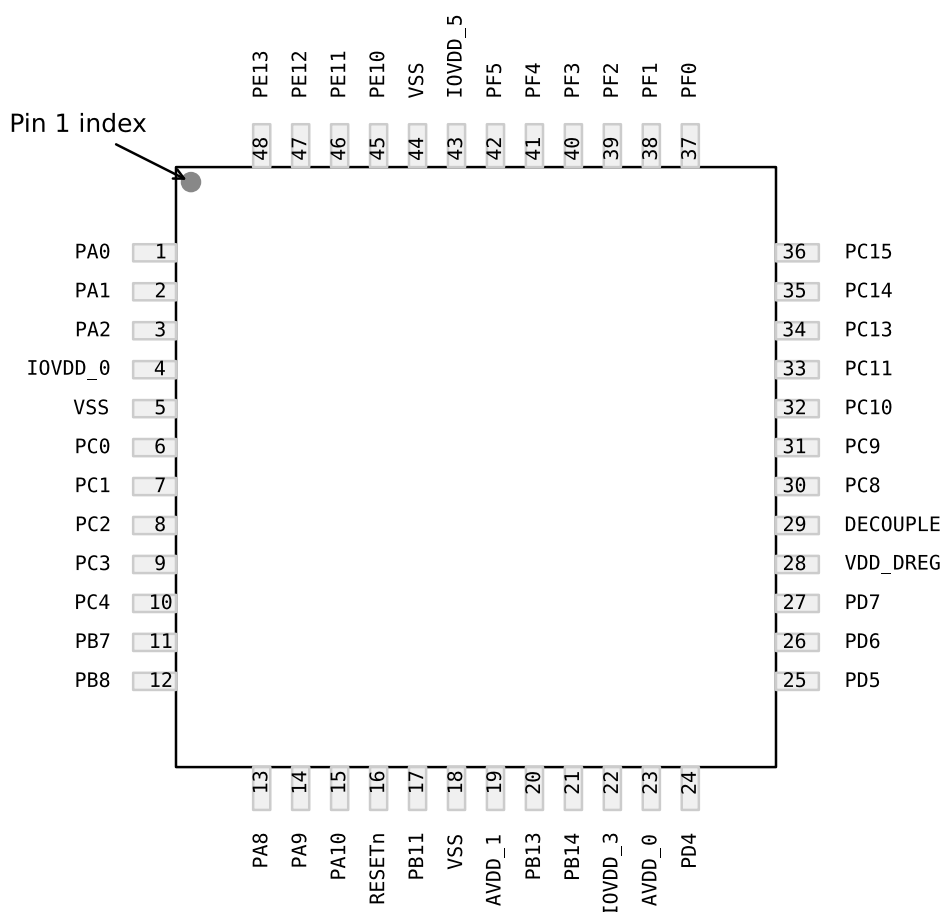


Figure 5.2. EFM32G222 Pinout (top view, not to scale)

Table 5.4. Device Pinout

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_0	Digital IO power supply 0.			
5	VSS	Ground.			

5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.5. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1				Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8		PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9		PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10		PC10		Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12		PC9		USART0 clock input / output.
US0_CS	PE13		PC8		USART0 chip select input / output.
US0_RX	PE11		PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10		PC11		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4				USART2 clock input / output.
US2_CS	PC5				USART2 chip select input / output.
US2_RX	PC3				USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2				USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

Alternate	LOCATION				
Functionality	0	1	2	3	Description
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0	PF6	PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2	LCD_SEG0			ACMP1_O #0 DBG_SWO #0
52	PF3	LCD_SEG1	TIM0_CDTI0 #2		
53	PF4	LCD_SEG2	TIM0_CDTI1 #2		
54	PF5	LCD_SEG3	TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground.			
57	PE8	LCD_SEG4	PCNT2_S0IN #1		
58	PE9	LCD_SEG5	PCNT2_S1IN #1		
59	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
60	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	BOOT_RX
61	PE12	LCD_SEG8	TIM1_CC2 #1	US0_CLK #0	
62	PE13	LCD_SEG9		US0_CS #0	ACMP0_O #0
63	PE14	LCD_SEG10		LEU0_TX #2	
64	PE15	LCD_SEG11		LEU0_RX #2	

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG7	PE11				LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12				LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13				LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14				LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15				LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15				LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0				LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1				LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2				LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3				LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4				LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5				LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6				LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20	PB3				LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG21	PB4				LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG22	PB5				LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG23	PB6				LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG24	PF6				LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG25	PF7				LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG26	PF8				LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG27	PF9				LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG28	PD9				LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG29	PD10				LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7.

11.2 QFN32 PCB Layout

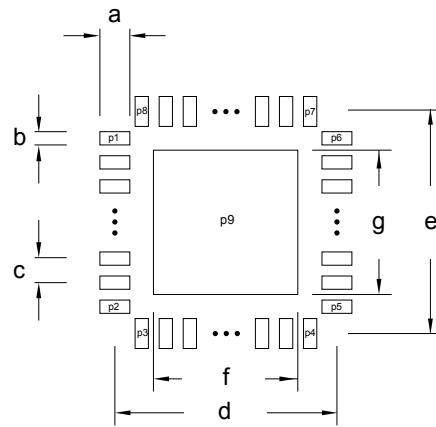


Figure 11.2. QFN32 PCB Land Pattern

Table 11.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
c	0.65	P3	9	P8	32
d	6.00	P4	16	P9	33
e	6.00	P5	17		
f	4.40				
g	4.40				

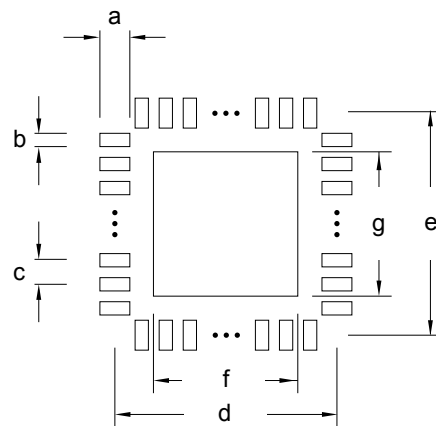


Figure 11.3. QFN32 PCB Solder Mask

Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.92
b	0.47
c	0.65

13.19 Revision 0.82

December 9th, 2009

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For LQFP100 devices, incorrect pin 0 removed from pinout table.

Updated contact information.

ADC current consumption numbers updated in ADC Electrical Characteristics.

For devices with LCD, updated LCD supply voltage range in LCD Electrical Characteristics.

13.20 Revision 0.81

November 20th, 2009

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For devices without a differential DAC, System Summary updated.

Electrical Characteristics updated.

Storage temperature in Electrical Characteristics updated.

Temperature coefficient of band-gap reference in Electrical Characteristics added.

Erase times in Flash Electrical Characteristics updated.

Definitions of DNL and INL added in ADC section.

For devices with and LCD, LCD Electrical Characteristics added.

Current consumption of digital peripherals added in Electrical Characteristics.

For LQFP100 devices, package information in Pinout and Package corrected.

For BGA112 devices, pinout information in Pinout table corrected.

Updated errata section.