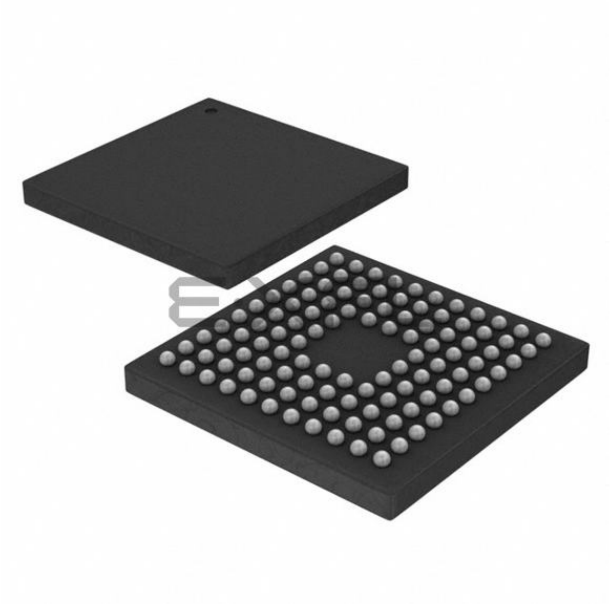

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	90
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g890f32g-e-bga112

- Supply Voltage Comparator
- Ultra efficient Power-on Reset and Brown-Out Detector
- 2-pin Serial Wire Debug Interface
  - 1-pin Serial Wire Viewer
- Pre-Programmed USB/UART Bootloader
- Temperature range -40 to 85 ºC
- Single power supply 1.98 to 3.8 V
- Packages
  - BGA112
  - LQFP100
  - TQFP64
  - TQFP48
  - QFN64
  - QFN32

3.1.14 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

3.1.15 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART^{TM}, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/ s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.16 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

3.1.17 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.18 Low Energy Timer (LETIMER)

The unique LETIMER^{TM}, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

3.1.19 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.1.20 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.21 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.22 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

3.1.23 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single-ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

3.2 Configuration Summary

3.2.1 EFM32G200

The features of the EFM32G200 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.1. EFM32G200 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:5], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:4]
DAC0	Full configuration	DAC0_OUT[0]
GPIO	24 pins	Available pins are shown in Table 4.3 (p. 57)

3.2.4 EFM32G230

The features of the EFM32G230 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.4. EFM32G230 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 57)

4.4.3 EM2 Current Consumption

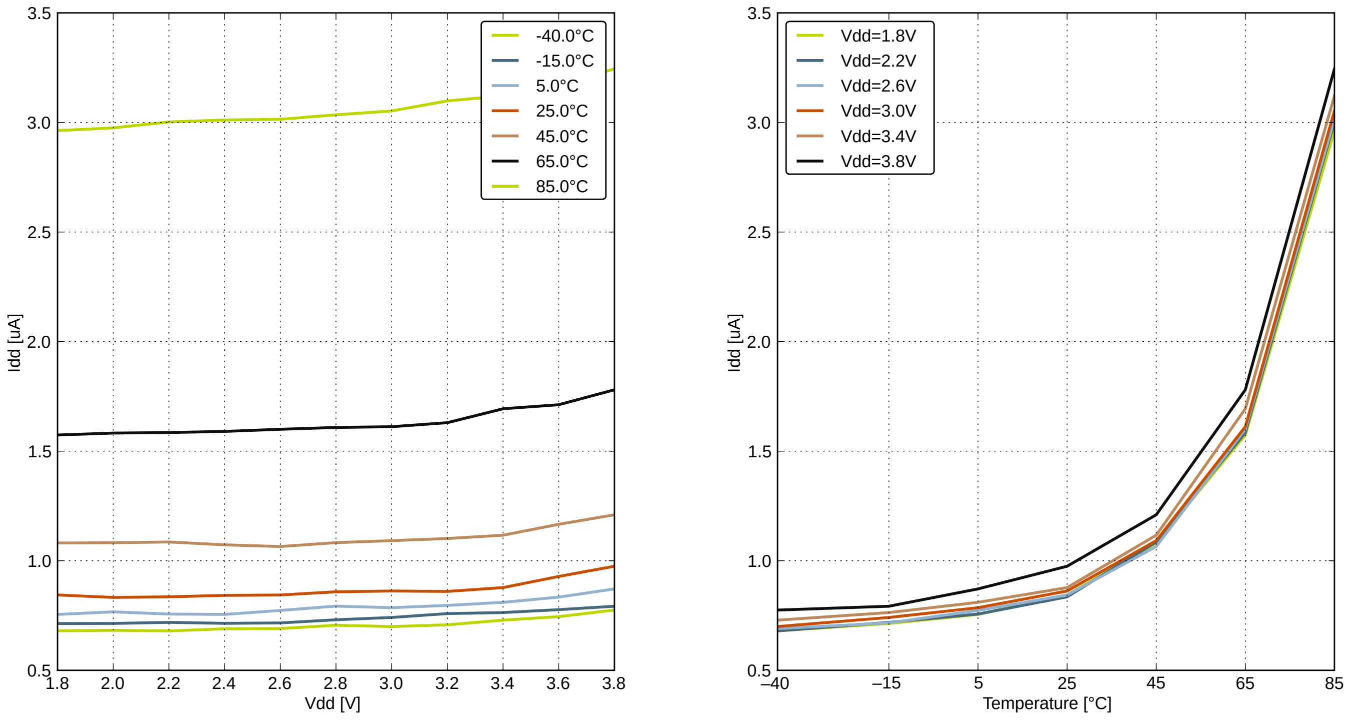

Figure 4.11. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO

4.7 Flash

Table 4.6. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 ºC	10000	—	—	h
		T_{AMB}<85 ºC	10	—	—	years
		T_{AMB}<70 ºC	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time[2]	t_{P_ERASE}		20.7	22.0	24.8	ms
Device erase time[3]	t_{D_ERASE}		41.8	45.0	49.2	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

Note:

1. Measured at 25 °C.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.

4.8 General Purpose Input Output

Table 4.7. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	$0.30 \times V_{DD}$[1]	V
Input high voltage	V_{IOIH}		$0.70 \times V_{DD}$[1]	—	—	V
Output high voltage (Production test condition = 3.0 V, DRIVE-MODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.80 \times V_{DD}$	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.90 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.85 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.90 \times V_{DD}$	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75 \times V_{DD}$	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80 \times V_{DD}$	—	—	V

4.9.4 HFRCO

Table 4.11. HFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25 °C	f_{HFRCO}	28 MHz frequency band	27.16	28	28.84	MHz
		21 MHz frequency band	20.37	21	21.63	MHz
		14 MHz frequency band	13.58	14	14.42	MHz
		11 MHz frequency band	10.67	11	11.33	MHz
		7 MHz frequency band	6.402	6.6[1]	6.798	MHz
		1 MHz frequency band	1.164	1.2[2]	1.236	MHz
Settling time	$t_{HFRCO\_settling}$	After start-up, f_{HFRCO} = 14 MHz	—	0.6	—	Cycles
		After band switch	—	25	—	Cycles
Current consumption (Production test condition = 14 MHz)	I_{HFRCO}	f_{HFRCO} = 28 MHz	—	158	190	µA
		f_{HFRCO} = 21 MHz	—	125	155	µA
		f_{HFRCO} = 14 MHz	—	99	120	µA
		f_{HFRCO} = 11 MHz	—	88	110	µA
		f_{HFRCO} = 6.6 MHz	—	72	90	µA
		f_{HFRCO} = 1.2 MHz	—	24	32	µA
Duty cycle	DC_{HFRCO}	f_{HFRCO} = 14 MHz	48.5	50	51	%
Frequency step for LSB change in TUNING value	$TUNESTEP_{HFRCO}$		—	0.3[3]	—	%

Note:

1. For devices with prod. rev. < 19, Typ = 7 MHz and Min/Max values not applicable.
2. For devices with prod. rev. < 19, Typ = 1 MHz and Min/Max values not applicable.
3. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise Ratio (SNR)	SNR_{ADC}	200 kSamples/s, 12 bit, differential, V_{DD} reference,ADC_CLK = 7 MHz, BIASPROG = 0x747	63	69	—	dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference,ADC_CLK = 7 MHz, BIASPROG = 0x747	—	70	—	dB

4.10.1 Typical Performance

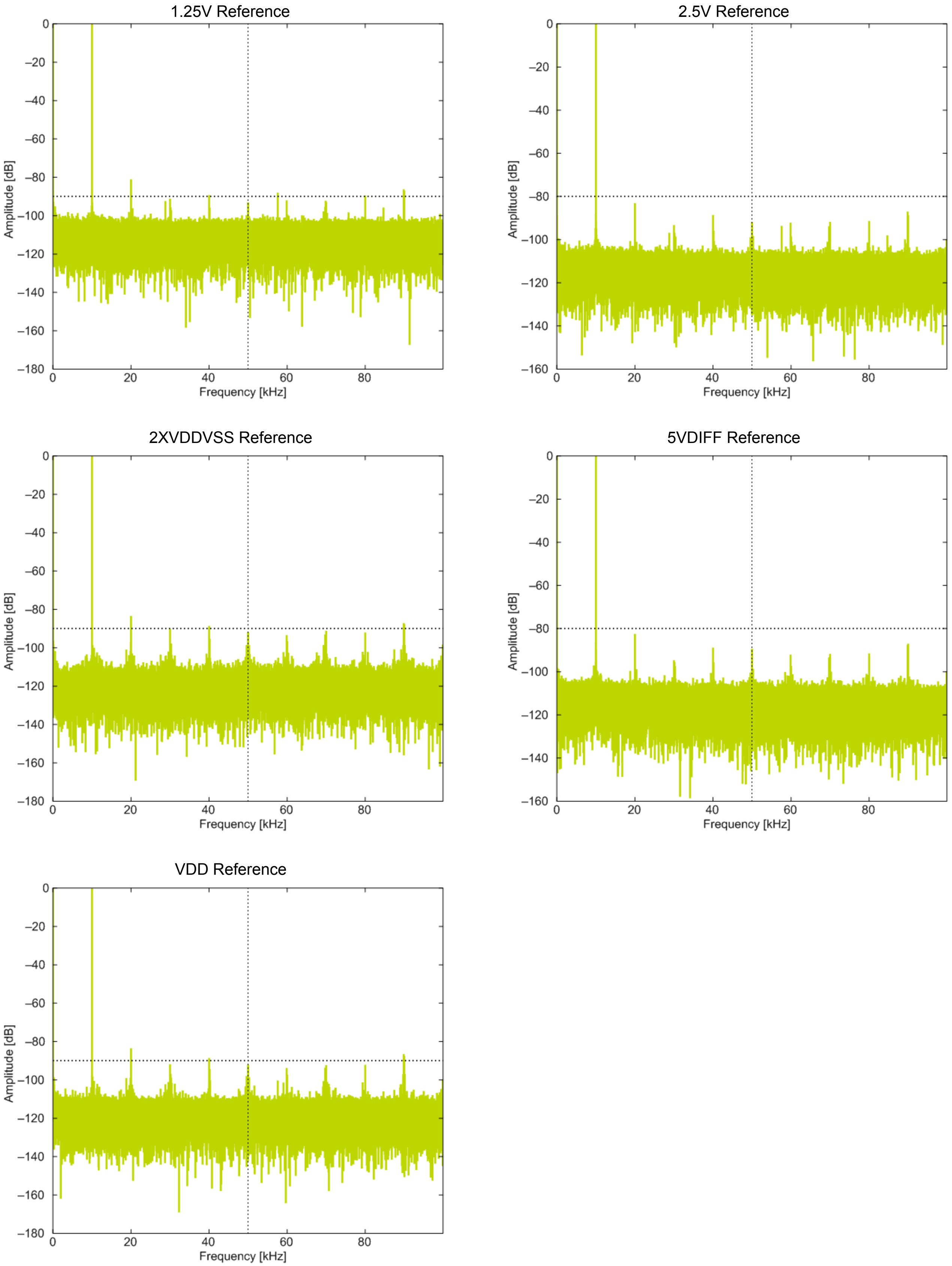

Figure 4.29. ADC Frequency Spectrum, VDD = 3V, Temp = 25°C

4.11 Digital Analog Converter (DAC)

Table 4.15. DAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage range	V_{DACOUT}	VDD voltage reference, single-ended	0	—	V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$	—	V_{DD}	V
Output common mode voltage range	V_{DACCM}		0	—	V_{DD}	V
Average active current	I_{DAC}	500 kSamples/s, 12 bit, internal 1.25 V reference, Continuous Mode	—	400[1]	650[1]	µA
		100 kSamples/s, 12 bit, internal 1.25 V reference, Sample/Hold Mode	—	200[1]	250[1]	µA
		1 kSamples/s 12 bit, internal 1.25 V reference, Sample/Off Mode	—	17[1]	25[1]	µA
Sample rate	SR_{DAC}		—	—	500	ksamples/s
DAC clock frequency	f_{DAC}	Continuous Mode	—	—	1000	kHz
		Sample/Hold Mode	—	—	250	kHz
		Sample/Off Mode	—	—	250	kHz
Clock cycles per conversion	$CYC_{DACCONV}$		—	2	—	cycles
Conversion time	$t_{DACCONV}$		2	—	—	µs
Settling time	$t_{DACSETTLE}$		—	5	—	µs
Signal-to-Noise Ratio (SNR)	SNR_{DAC}	500 kSamples/s, 12 bit, single-ended, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference	—	59	—	dB
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	59	—	dB

4.14 LCD

Table 4.18. LCD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frame rate	f_{LCDFR}		30	—	200	Hz
Number of segments supported	NUM_{SEG}		—	4×40	—	seg
LCD supply voltage range	V_{LCD}	Internal boost circuit enabled	2.0	—	3.8	V
Steady state current consumption.	I_{LCD}	Display disconnected, static mode, framerate 32 Hz, all segments on.	—	250	—	nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONE-THIRD in LCD_DISPCTRL register.	—	550	—	nA
Steady state Current contribution of internal boost.	$I_{LCDBOOST}$	Internal voltage boost off	—	0	—	µA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.	—	8.4	—	µA
Boost Voltage	V_{BOOST}	VBLEV of LCD_DISPCTRL register to LEVEL0	—	3.0	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL1	—	3.08	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL2	—	3.17	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL3	—	3.26	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL4	—	3.34	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL5	—	3.43	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL6	—	3.52	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL7	—	3.6	—	V

The total LCD current is given by the following equation. $I_{LCDBOOST}$ is zero if internal boost is off.

$$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST}$$

Table 5.1. Device Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_1	Digital IO power supply 1.			
5	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
6	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
7	PB7	LFXTAL_P		US1_CLK #0	
8	PB8	LFXTAL_N		US1_CS #0	
9	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
10	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
11	AVDD_2	Analog power supply 2.			
12	PB13	HFXTAL_P		LEU0_TX #1	
13	PB14	HFXTAL_N		LEU0_RX #1	
14	IOVDD_3	Digital IO power supply 3.			
15	AVDD_0	Analog power supply 0.			
16	PD4	ADC0_CH4		LEU0_TX #0	
17	PD5	ADC0_CH5		LEU0_RX #0	
18	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
19	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
20	VDD_DREG	Power supply for on-chip voltage regulator.			
21	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
22	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
23	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
24	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
25	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
26	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
27	PF2				ACMP1_O #0 DBG_SWO #0
28	IOVDD_5	Digital IO power supply 5.			
29	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
30	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
38	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
39	PF2				ACMP1_O #0 DBG_SWO #0
40	PF3		TIM0_CDTI0 #2		
41	PF4		TIM0_CDTI1 #2		
42	PF5		TIM0_CDTI2 #2		
43	IOVDD_5	Digital IO power supply 5.			
44	VSS	Ground.			
45	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
46	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX
47	PE12		TIM1_CC2 #1	US0_CLK #0	
48	PE13			US0_CS #0	ACMP0_O #0

Alternate	LOCATION				
Functionality	0	1	2	3	Description
US0_CS	PE13		PC8		USART0 chip select input / output.
US0_RX	PE11		PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10		PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4				USART2 clock input / output.
US2_CS	PC5				USART2 chip select input / output.
US2_RX	PC3				USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2				USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G2322 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.12. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	—	—	—	—	PA10	PA9	PA8	—	—	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	—	—	—	—	—	—	—
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	—	—	—	—	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

Alternate	LOCATION				
Functionality	0	1	2	3	Description
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0		PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12			Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13			Timer 2 Capture Compare input / output channel 1.
TIM2_CC2		PA14			Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12	PE5			USART0 clock input / output.
US0_CS	PE13	PE4			USART0 chip select input / output.
US0_RX	PE11	PE6			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7			USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX		PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX		PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX		PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).

5.8.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G842 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.24. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	PA14	PA13	PA12	—	—	—	—	—	—	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	PB6	PB5	PB4	PB3	—	—	—
Port C	PC15	PC14	PC13	PC12	—	—	—	—	PC7	PC6	PC5	PC4	—	—	—	—
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
100	PA15	LCD_SEG 12	EBI_AD08 #0			

13.11 Revision 1.20

December 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Increased max storage temperature.

Added data for <150°C and <70°C on Flash data retention.

Changed latch-up sensitivity test description.

Added IO leakage current.

For LQFP100 devices, updated ESD CDM value.

Added Flash current consumption.

Updated HFRCO data.

Updated LFRCO data.

Added graph for ADC Absolute Offset over temperature.

Added graph for ADC Temperature sensor readout.

13.12 Revision 1.11

November 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Corrected maximum DAC clock speed for continuous mode.

Added DAC sample-hold mode voltage drift rate.

Added pulse widths detected by the HFXO glitch detector.

Added power sequencing information to Power Management section.

13.13 Revision 1.10

September 13th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For LQFP100 devices, corrected number of GPIO pins.

Added typical values for $R_{ADCFILT}$ and $C_{ADCFILT}$.

Added two conditions for DAC clock frequency; one for sample/hold and one for sample/off.

Added RoHS information and specified leadframe/solderballs material.

Added Serial Bootloader to feature list and system summary.

Updated ADC characterization data.

Updated DAC characterization data.

Updated RCO characterization data.

Updated ACMP characterization data.

Updated VCMP characterization data.

13.14 Revision 1.00

April 23rd, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

ADC_VCM line removed.

Added pinout illustration and additional pinout table.

Changed "Errata" chapter. Errata description moved to separate document.

Document changed status from "Preliminary".

Updated "Electrical Characteristics" chapter.

For EFM32G222

May 20th, 2011

Updated LFXO load capacitance section.