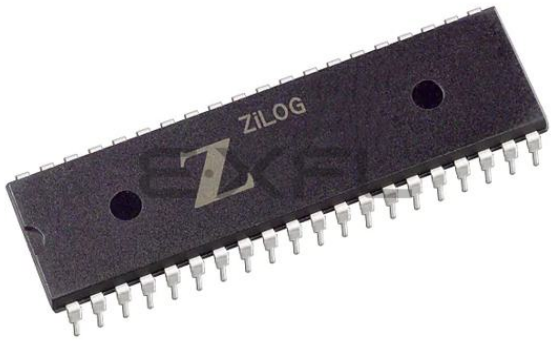


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	-
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e2204psc

ZiLOG

CUSTOMER PROCUREMENT SPECIFICATION

Z86E22
CMOS Z8® OTP MICROCONTROLLER

GENERAL DESCRIPTION

The Z86E22 microcontroller (MCU) introduces the next level of sophistication to single-chip architecture. The Z86E22 is a member of the Z8 single-chip microcontroller family with 8 Kbytes of EPROM and 236 bytes of general purpose RAM.

The Z86E22 is a pin compatible, One-Time-Programmable (OTP) version of the Z86C21. The Z86E22 contains 8 Kbytes of EPROM memory in place of the 8 Kbyte of ROM on the Z86C21.

The MCU is housed in a 40-pin DIP, and is manufactured in CMOS technology. The MCU can address both external memory and preprogrammed ROM which enables this Z8 microcomputer to be used in high volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E22 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E22 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 General-Purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E22 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Functional Block Description).

The Z86E22 is a low EMI noise, low Halt current version of the Z86E21. Rated at no more than 4 MHz, the Z86E22 has a Halt current of 1.5 mA or less.

In ROM Protect Mode, the instructions LDC, LDCI, LDE and LDEI are disabled when reading address locations 0000H to 1FFFH.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

PRODUCT RECOMMENDATIONS

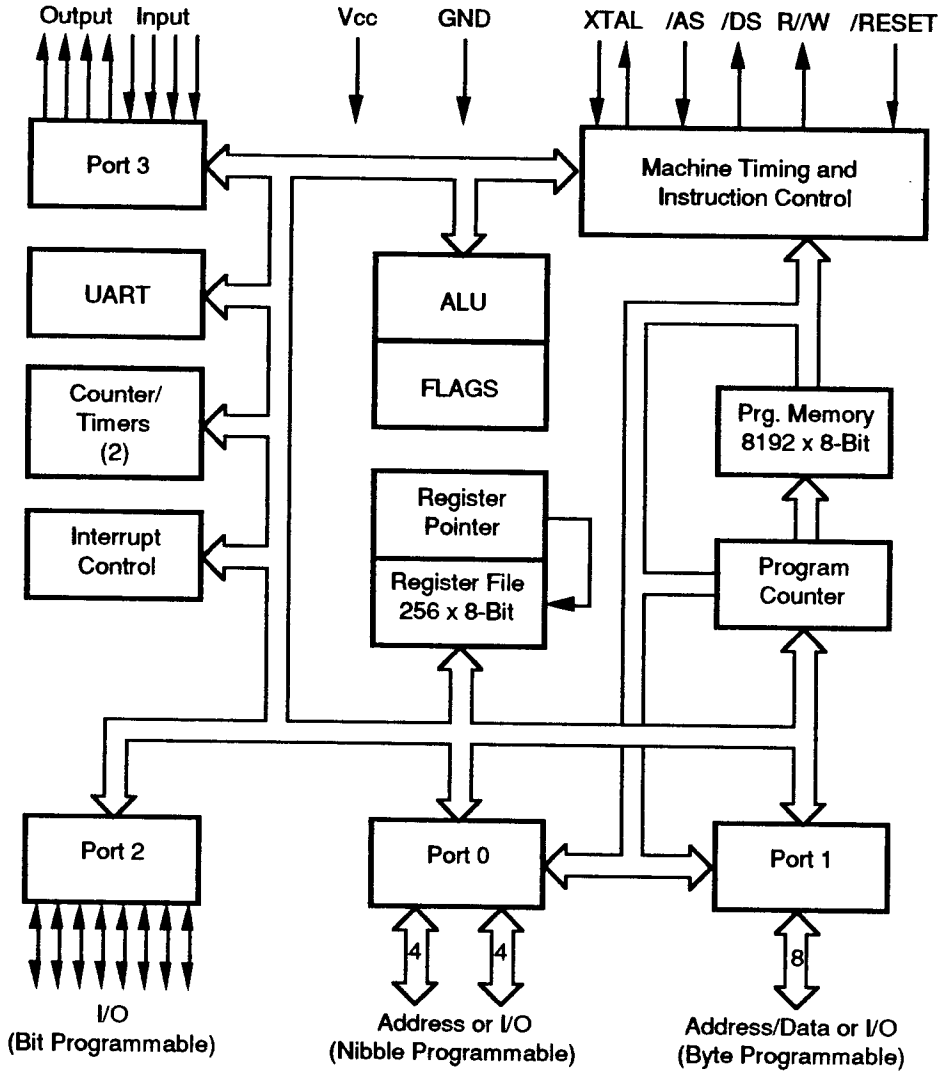
Zilog recommends the following programming equipment for use with this One-Time-Programmable product:

Device	Zilog Support Tool	Recommended Revision Level Hardware	Software
Z86E22	Z86C1200ZEM ICEBOX™ Emulator* (*Does not support 4K/8K option.)	B	1.5
Z86E22	Data I/O Unisite Programmer* (*Does not support option bits.)		3.7

Some non-Zilog programmers may have different programming waveforms, voltages and timings and not all programmers may meet the programming requirements of Zilog's One-Time-Programmable products.

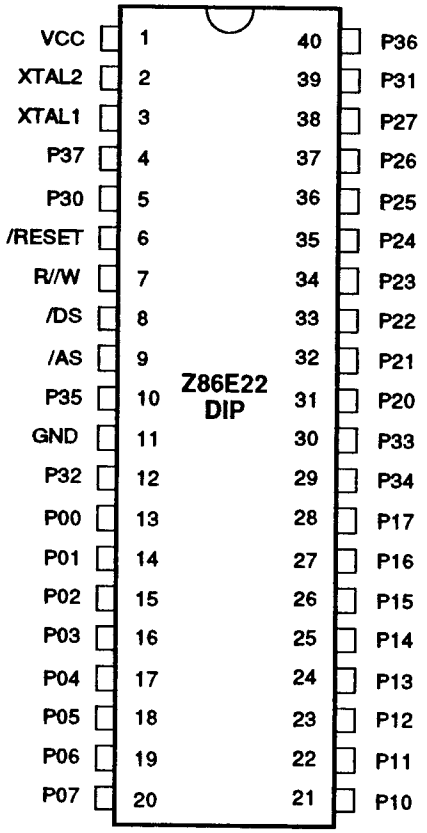
If difficulty is encountered in programming a Zilog OTP product, please contact your local Zilog sales office.

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

PIN DESCRIPTION



Standard Mode Pin Assignments

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp		†	C

Notes:

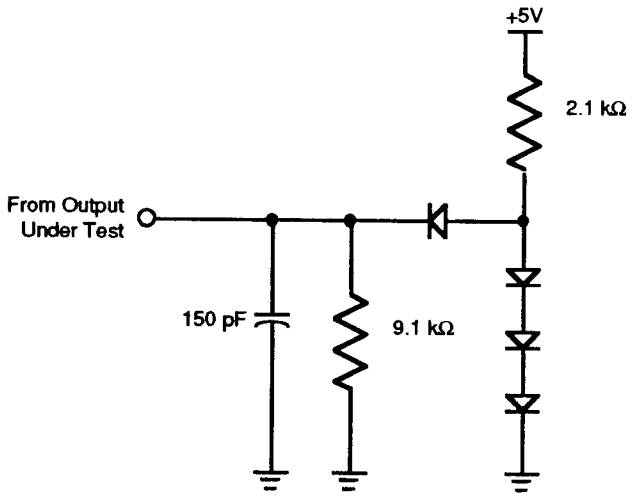
* Voltages on all pins with respect to GND. 13.0 V Maximum on P30-P33.

† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

DC CHARACTERISTICS

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
	Max Input Voltage		13		V	P30-P33 Only
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.0 mA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	0.8		V	
I_{IL}	Input Leakage	-10	10		µA	0V <V_{IN} <+5.25V
I_{OL}	Output Leakage	-10	10		µA	0V <V_{IN} <+5.25V
I_{IR}	Reset Input Current		-50		µA	V_{CC}= +5.25V, V_{RL} = 0V
I_{CC}	Supply Current		25	13.5	mA	4 MHz
I_{CC1}	Standby Current		5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current		10	1.5	µA	STOP Mode V_{IN} = 0V, V_{CC} @ 4 MHz

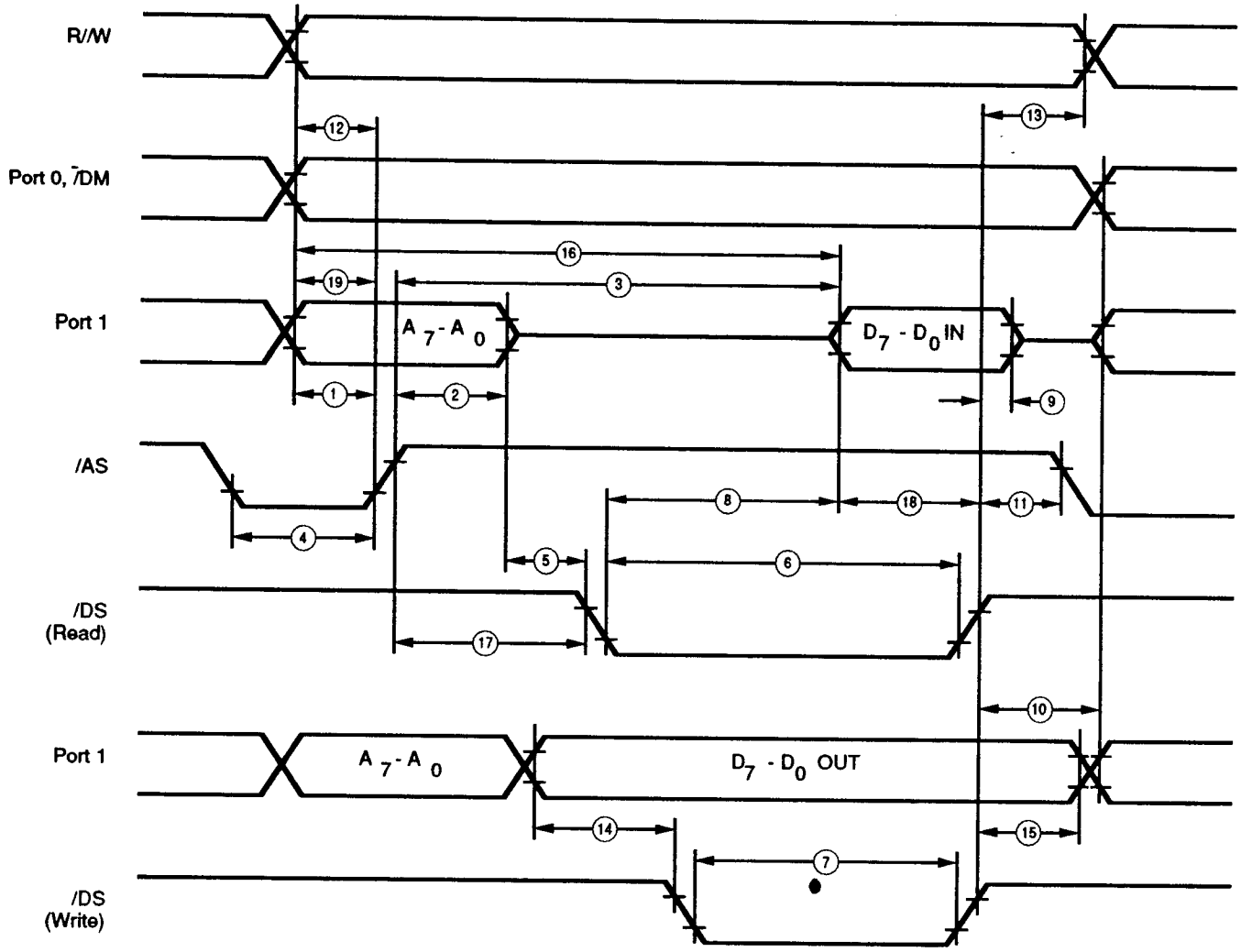
Notes:

I_{CC2} requires loading TMR (F1H) with any value prior to STOP execution.
Use this sequence:

```
LD TMR,#00
NOP
```

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	T_A = 0°C to 70°C 4 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	50		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	60		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		320	ns	[1,2,3]
4	TwAS	/AS Low Width	80		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		ns	
6	TwDSR	/DS (Read) Low Width	250		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	160		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		200	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	80		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	70		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	50		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	60		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	50		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	80		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		410	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	80		ns	[2,3]

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] See clock cycle dependent characteristics table.

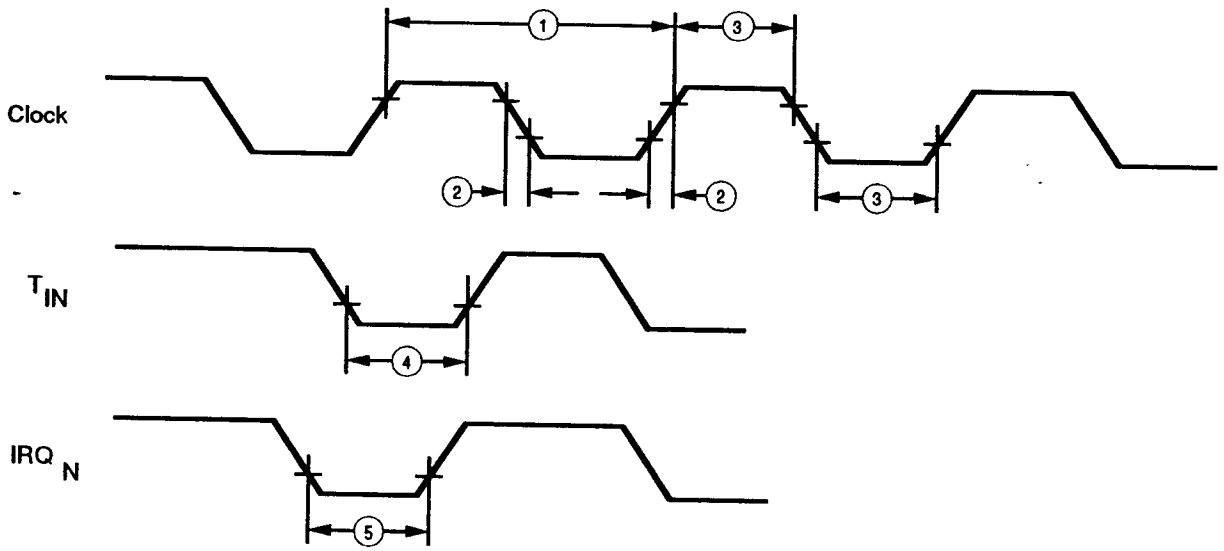
Standard Test Load

All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.2TpC + 0.32
2	TdAS(A)	0.295TpC - 3.25
3	TdAS(DR)	1.19TpC + 6.14
4	TwAS	0.33TpC - 1.65
6	TwDSR	1.165TpC - 10.56
7	TwDSW	0.635TpC + 1.67
8	TdDSR(DR)	0.985TpC - 42.5
10	TdDS(A)	0.4TpC
11	TdDS(AS)	0.295TpC - 3.14
12	TdR/W(AS)	0.2TpC
13	TdDS(R/W)	0.4TpC - 15
14	TdDW(DSW)	0.2TpC
15	TdDS(DW)	0.44TpC - 19
16	TdA(DR)	2TpC - 20
17	TdAS(DS)	45.5TpC - 10.7
18	TsDI(DS)	0.4TpC - 10
19	TdDM(AS)	0.45TpC - 26.3

AC CHARACTERISTICS
Additional Timing Diagram



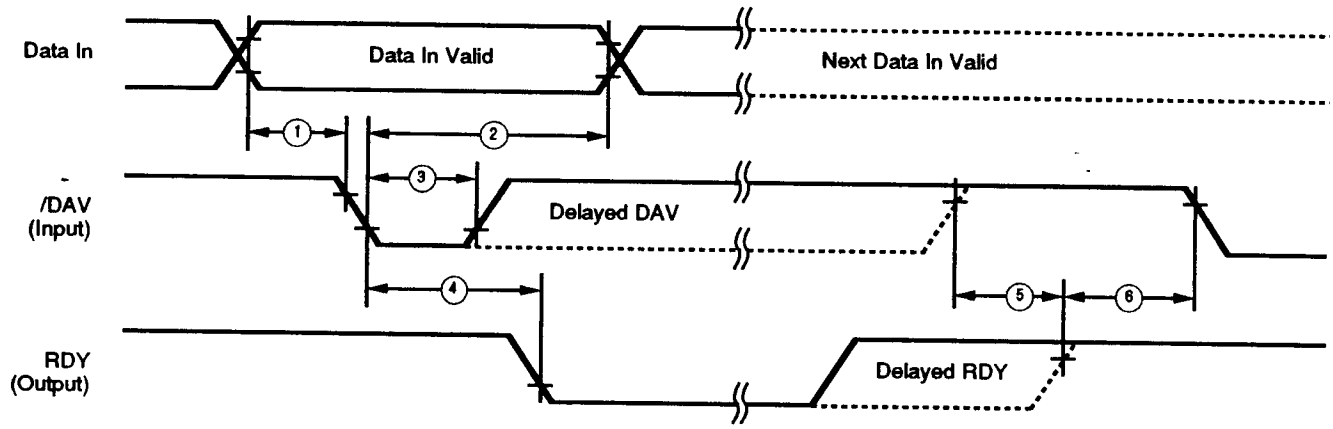
Additional Timing

AC CHARACTERISTICS
Additional Timing Table

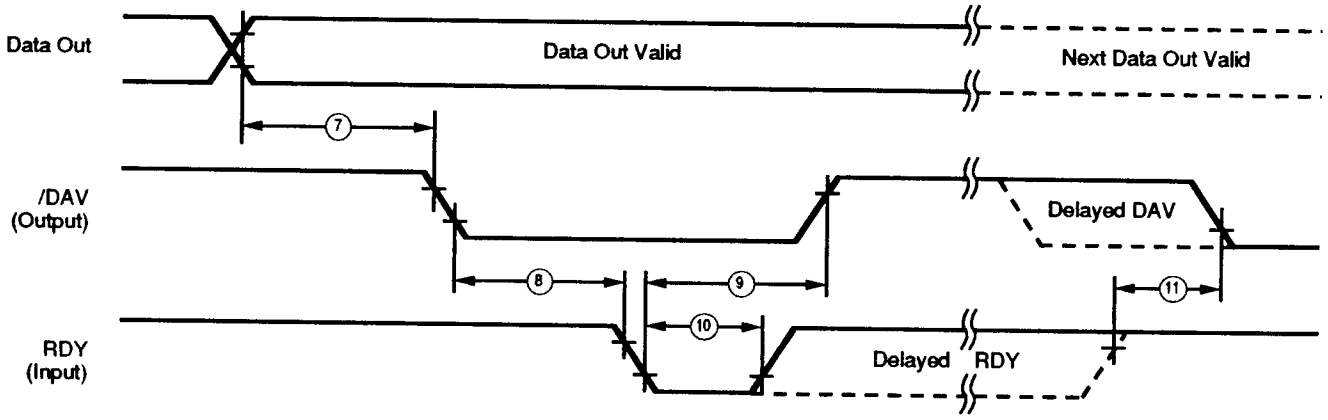
No	Symbol	Parameter	T_A = 0°C to 70°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	250		ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		25	ns	[1]
3	TwC	Input Clock Width	100		ns	[1]
4	TwTinL	Timer Input Low Width	75		ns	[2]
5	TwTinH	Timer Input High Width	2.5TpC			[2]
6	TpTin	Timer Input Period	4TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	2.5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	2.5TpC			[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request via Port 3.
[4] Interrupt request via Port 3 (P31-P33).
[5] Interrupt request via Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

No	Symbol	Parameter	T_A = 0°C to 70°C 4 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		IN
2	ThDI(DAV)	Data In Hold Time	145		IN
3	TwDAV	Data Available Width	110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	0		IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay		TpC	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115	OUT
10	TwRDY	RDY Width	110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115	OUT

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