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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	40MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe160fu8f40raakxuma1

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Summary of Features

16-Bit Single-Chip Real Time Signal Controller XE160FU (XE166 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XE160FU are summarized here.

- High-performance CPU with five-stage pipeline and MPU
 - 15.2 ns instruction cycle @ 66 MHz CPU clock (single-cycle execution)
 - One-cycle 32-bit addition and subtraction with 40-bit result
 - One-cycle multiplication (16 × 16 bit)
 - Background division (32 / 16 bit) in 21 cycles
 - One-cycle multiply-and-accumulate (MAC) instructions
 - Enhanced Boolean bit manipulation facilities
 - Zero-cycle jump execution
 - Additional instructions to support HLL and operating systems
 - Register-based design with multiple variable register banks
 - Fast context switching support with two additional local register banks
 - 16 Mbytes total linear address space for code and data
 - 1,024 Bytes on-chip special function register area (C166 Family compatible)
 - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 46 interrupt nodes
 - Selectable external inputs for interrupt generation and wake-up
 - Fastest sample-rate 15.2 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
 - 2 Kbytes on-chip dual-port RAM (DPRAM)
 - 2 Kbytes on-chip data SRAM (DSRAM)
 - 4 Kbytes on-chip program/data SRAM (PSRAM)
 - Up to 64 Kbytes on-chip program memory (Flash memory)
 - Memory content protection through Error Correction Code (ECC) for Flash memory and through parity for RAMs



Summary of Features

1.1 Device Types

The following XE160FU device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XE160FU Device Types

Derivative ¹⁾	Flash Memory ²⁾	PSRAM DSRAM ³⁾	Capt./Comp. Modules	ADC ⁴⁾ Chan.	Interfaces ⁴⁾
XE160FU-4FxR	32 Kbytes	4 Kbytes 2 Kbytes	CC2 CCU60	8	2 Serial Chan.
XE160FU-8FxR	64 Kbytes	4 Kbytes 2 Kbytes	CC2 CCU60	8	2 Serial Chan.

1) x is a placeholder for available speed grade in MHz. Can be 40 or 66.

2) Specific information about the on-chip Flash memory in Table 3.

3) All derivatives additionally provide 2 Kbytes DPRAM.

4) Specific information about the available channels in Table 5.



General Device Information

Table 6 Pin Definitions and Functions (cont'd)					
Pin	Symbol	Ctrl.	Туре	Function	
15	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output	
	U0C1_SELO 0	01	St/B	USIC0 Channel 1 Select/Control 0 Output	
	U0C0_SELO 1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output	
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.	
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input	
	ESR2_7	1	St/B	ESR2 Trigger Input 7	
16	P2.8	O0 / I	St/B	Bit 8 of Port 2, General Purpose Input/Output	
	U0C1_SCLK OUT	01	St/B	USIC0 Channel 1 Shift Clock Output	
	EXTCLK	O2	St/B	Programmable Clock Signal Output	
	CC2_CC21	O3 / I	St/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.	
	U0C1_DX1D	I	St/B	USIC0 Channel 1 Shift Clock Input	
17	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output	
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output	
	CC2_CC22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.	
	C1	I	St/B	Configuration Pin 1	
	TCK_A	I	St/B	DAP0/JTAG Clock Input	
18	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output	
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output	
	U0C0_SELO 3	02	St/B	USIC0 Channel 0 Select/Control 3 Output	
	CC2_CC23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.	
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input	
	CAPINA	I	St/B	GPT12E Register CAPREL Capture Input	



3.7 Capture/Compare Unit (CC2)

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs allow event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.

All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Compare Modes	Function			
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible			
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible			

Table 9 Compare Modes



Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

 Table 9
 Compare Modes (cont'd)

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.



3.9 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

Note: Signals T2IN, T2EUD, T4EUD, T5EUD, T6OUT, T6IN and T6EUD are not connected to pins.



3.12 Universal Serial Interface Channel Modules (USIC)

The XE160FU features the USIC module USIC0. The module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.



Figure 10 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)



3.18 Instruction Set Summary

Table 11 lists the instructions of the XE160FU.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the "**Instruction Set Manual**".

This document also provides a detailed description of each instruction.

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2/4
ADDC(B)	Add word (byte) operands with Carry	2/4
SUB(B)	Subtract word (byte) operands	2/4
SUBC(B)	Subtract word (byte) operands with Carry	2/4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- \times 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2/4
OR(B)	Bitwise OR, (word/byte operands)	2/4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2/4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2/4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2/4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2/4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 11 Instruction Set Summary



Table II Instru	uction Set Summary (cont d)	
Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2/4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2/4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction ¹⁾	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2/4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2/4

Table 11 Instruction Cat Cummany (cont'd)



4.1.1 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE160FU. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Voltage Regulator Buffer Capacitance for DMP_M	$C_{\rm EVRM}$ SR	1.0	-	4.7	μF	1)2)
External Load Capacitance	$C_{L} \operatorname{SR}$	-	20 ³⁾	_	pF	pin out driver= default 4)
System frequency	$f_{\rm SYS}{ m SR}$	-	-	66	MHz	5)
Overload current for analog inputs ⁶⁾	$I_{\rm OVA}{ m SR}$	-2	-	5	mA	not subject to production test
Overload current for digital inputs ⁶⁾	$I_{\rm OVD}{\rm SR}$	-5	_	5	mA	not subject to production test
Overload current coupling factor for analog inputs ⁷)	K _{OVA} CC	_	2.5 x 10 ⁻⁴	1.5 x 10 ⁻³	-	<i>I</i> _{OV} < 0 mA; not subject to production test
		_	1.0 x 10 ⁻⁶	1.0 x 10 ⁻⁴	-	<i>I</i> _{OV} > 0 mA; not subject to production test

Table 13 Operating Conditions



4.3 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XE160FU can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.

The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE160FU are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in **Section 4.7.4**.



Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Code	Default Voltage Level	Notes ¹⁾
0000 _B	-	out of valid operation range
0001 _B	3.0 V	LEV1V: reset request
0010 _B - 0101 _B	3.1 V - 3.4 V	step width is 0.1 V
0110 _B	3.6 V	
0111 _B	4.0 V	
1000 _B	4.2 V	
1001 _B	4.5 V	LEV2V: no request
1010 _B - 1110 _B	4.6 V - 5.0 V	step width is 0.1 V
1111 _B	5.5 V	

Table 25 Coding of bit fields LEVxV in Register SWDCON0

1) The indicated default levels are selected automatically after a power reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ± 10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in **Table 26**.

Table 26	Coding of t	oit fields LEVx	V in Registers	PVCyCONz

Code	Default Voltage Level	Notes ¹⁾
000 _B - 011 _B	-	out of valid operation range
100 _B	1.35 V	LEV1V: reset request
101 _B	1.45 V	LEV2V: interrupt request ²⁾
110 _B - 111 _B	-	out of valid operation range

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.



4.6 Flash Memory Parameters

The XE160FU is delivered with all Flash sectors erased and with no protection installed. The data retention time of the XE160FU's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Parallel Flash module program/erase limit depending on Flash read activity	N _{PP} SR	-	-	1 ¹⁾		$N_{\rm FL_RD} \le 1$
Flash erase endurance for security pages	$N_{\rm SEC}{ m SR}$	10	-	-	cycle s	$t_{\rm RET} \ge 20$ years
Flash wait states ²⁾	N _{WSFLASH} SR	1	-	-		$f_{\rm SYS} \le 8 \ {\rm MHz}$
		2	-	-		f _{SYS} ≤ 13 MHz
		3	-	-		$f_{\rm SYS}$ \leq 17 MHz
		4	-	-		$f_{\rm SYS}$ > 17 MHz
Erase time per sector/page	t _{ER} CC	-	7 ³⁾	8.0	ms	
Programming time per page	t _{PR} CC	-	3 ³⁾	3.5	ms	
Data retention time	t _{RET} CC	20	-	-	year s	$N_{\rm ER} \le$ 1,000 cycl es
Drain disturb limit	$N_{\rm DD}{ m SR}$	32	-	-	cycle s	

Table 27 Flash Parameters



Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Number of erase cycles	$N_{ER}SR$	-	-	15000	cycle s	$t_{\text{RET}} \ge 5$ years; Valid for up to 64 user selected sectors (data storage)
		-	_	1000	cycle s	$t_{\text{RET}} \ge 20$ years

Table 27 Flash Parameters (cont'd)

 All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.

2) Value of IMB_IMBCTRL.WSFLASH.

3) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XE160FU Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.



Parameter	Symbol		Values	S	Unit	Note / Test Condition
		Min.	Тур.	Max.		
VCO output frequency	f _{vco} CC	50	-	110	MHz	VCOSEL= 00 _B ; VCOmode= controlled
		10	-	40	MHz	VCOSEL= 00 _B ; VCOmode= free running
		100	-	160	MHz	VCOSEL= 01 _B ; VCOmode= controlled
		20	-	80	MHz	VCOSEL= 01 _B ; VCOmode= free running

Table 28 System PLL Parameters

4.7.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

 $f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.7.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system. Please refer to the Programmer's Guide.



4.7.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 32 is valid under the following conditions: C_L = 20 pF; *SSC*= master ; voltage_range= upper

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	1	Test Condition
Slave select output SELO active to first SCLKOUT transmit edge	t ₁ CC	t _{SYS} - 8 ¹⁾	-	-	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t ₂ CC	t _{SYS} - 6 ¹⁾	-	-	ns	
Data output DOUT valid time	t ₃ CC	-6	-	9	ns	
Receive data input setup time to SCLKOUT receive edge	t ₄ SR	31	-	-	ns	
Data input DX0 hold time from SCLKOUT receive edge	t ₅ SR	-4	-	-	ns	

Table 32 USIC SSC Master Mode Timing for Upper Voltage Range

1) $t_{SYS} = 1 / f_{SYS}$



4.7.6 Debug Interface Timing

The debugger can communicate with the XE160FU via 1-pin SPD interface, via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 36 is valid under the following conditions: C_{L} = 20 pF; voltage_range= upper

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	1	Test Condition
DAP0 clock period	<i>t</i> ₁₁ SR	100 ¹⁾	_	_	ns	
DAP0 high time	<i>t</i> ₁₂ SR	8	-	-	ns	
DAP0 low time	t ₁₃ SR	8	-	-	ns	
DAP0 clock rise time	<i>t</i> ₁₄ SR	-	-	4	ns	
DAP0 clock fall time	t ₁₅ SR	-	-	4	ns	
DAP1 setup to DAP0 rising edge	t ₁₆ SR	6	-	-	ns	pad_type= stan dard
DAP1 hold after DAP0 rising edge	<i>t</i> ₁₇ SR	6	-	-	ns	pad_type= stan dard
DAP1 valid per DAP0 clock period ²⁾	<i>t</i> ₁₉ CC	92	95	-	ns	pad_type= stan dard

 Table 36
 DAP Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \ge t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.



XE160FU XE166 Family / Compact Line

Electrical Parameters



Figure 21 DAP Timing Host to Device



Figure 22 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.



Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 38 is valid under the following conditions: $C_1 = 20 \text{ pF}$; voltage_range= upper

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	-	Test Condition
TCK clock period	t ₁ SR	100 ¹⁾	_	_	ns	2)
TCK high time	t_2 SR	16	-	-	ns	
TCK low time	t ₃ SR	16	-	-	ns	
TCK clock rise time	t ₄ SR	-	-	8	ns	
TCK clock fall time	t ₅ SR	-	-	8	ns	
TDI/TMS setup to TCK rising edge	t ₆ SR	6	-	-	ns	
TDI/TMS hold after TCK rising edge	t ₇ SR	6	-	-	ns	
TDO valid from TCK falling edge (propagation delay) ³⁾	t ₈ CC	_	29	32	ns	
TDO high impedance to valid output from TCK falling edge ⁴⁾³⁾	t ₉ CC	-	29	32	ns	
TDO valid output to high impedance from TCK falling edge ³⁾	<i>t</i> ₁₀ CC	-	29	32	ns	
TDO hold after TCK falling edge ³⁾	<i>t</i> ₁₈ CC	5	_	_	ns	

Table 38 JTAG Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \ge t_{SYS}$.

2) Under typical conditions, the JTAG interface can operate at transfer rates up to 10 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.



Package and Reliability

5.2 Thermal Considerations

When operating the XE160FU in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta,IA}$

The internal power consumption is defined as

 $P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as $P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}}-V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- · Reduce the load on active output drivers