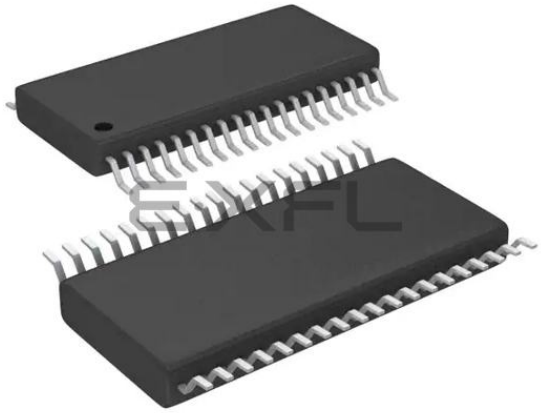
Infineon Technologies - XE160FU8F66RAAFXUMA1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe160fu8f66raafxuma1

Table of Contents

16-Bit Single-Chip
Real Time Signal Controller
XE160FU (XE166 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XE160FU are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 15.2 ns instruction cycle @ 66 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 46 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 15.2 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 2 Kbytes on-chip data SRAM (DSRAM)
  - 4 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 64 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC) for Flash memory and through parity for RAMs

- On-Chip Peripheral Modules
  - Synchronizable 12-bit A/D Converter with up to 8 channels, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Capture/compare unit for flexible PWM signal generation (CCU60)
  - Multi-functional general purpose timer unit with 5 timers
  - Up to 2 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip system timer and on-chip real time clock
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable window watchdog timer and oscillator watchdog
- Up to 28 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP), Single-Pin DAP (SPD) or JTAG interface
- 38-pin Green TSSOP package, 0.5 mm (10.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range[1]:
  - SAF-…: -40°C to 85°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XE160FU please contact your sales representative or local distributor.

1) Not all derivatives are offered in all temperature ranges.

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
19	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_CC60	O2	St/B	**CCU60 Channel 0 Output**
	CCU60_CC60INA	I	St/B	**CCU60 Channel 0 Input**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
20	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
21	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2	St/B	**CCU60 Channel 2 Output**
	CCU60_CC62INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
22	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
33	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O2	St/B	**USIC0 Channel 0 Shift Data Output**
	TDO_A	OH	St/B	**DAP1/JTAG Test Data Output**
	SPD_0	I/OH	St/B	**SPD Input/Output**
	C0	I	St/B	**Configuration Pin 0**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
34	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XE160FU completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pullup device will hold this pin high when nothing is driving it.
1	V_{AREF}	-	PS/B	**Reference Voltage for A/D Converters ADC0**
2	V_{AGND}	-	PS/B	**Reference Ground for A/D Converters ADC0**
31	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDIM} pins must be connected to each other.
10, 29	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins.
9, 30	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane.

2 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

The on-chip Flash memory stores code, constant data, and control data. The on-chip Flash memory consist of 1 module of 64 Kbytes. Each module is organized in 4-Kbyte sectors.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).
The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.
The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

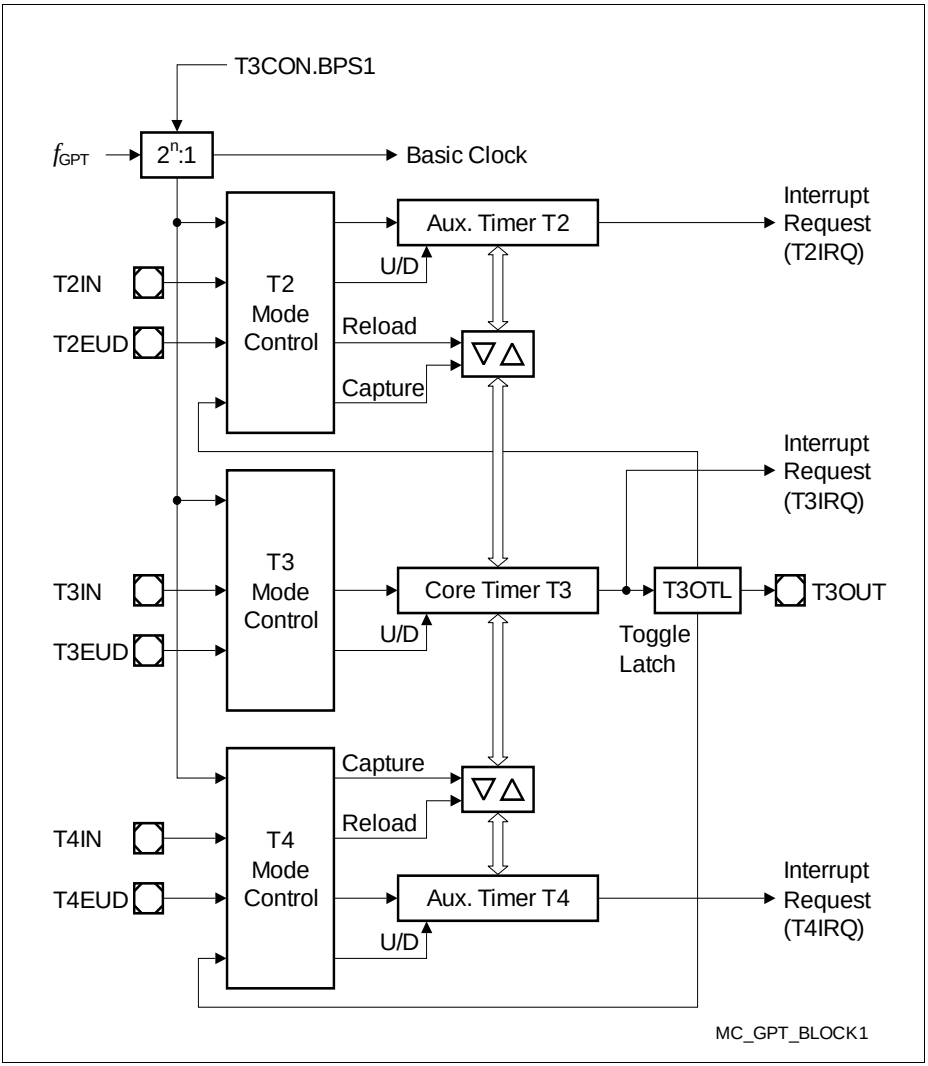

Figure 7 Block Diagram of GPT1

3.10 Real Time Clock

The Real Time Clock (RTC) module of the XE160FU can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

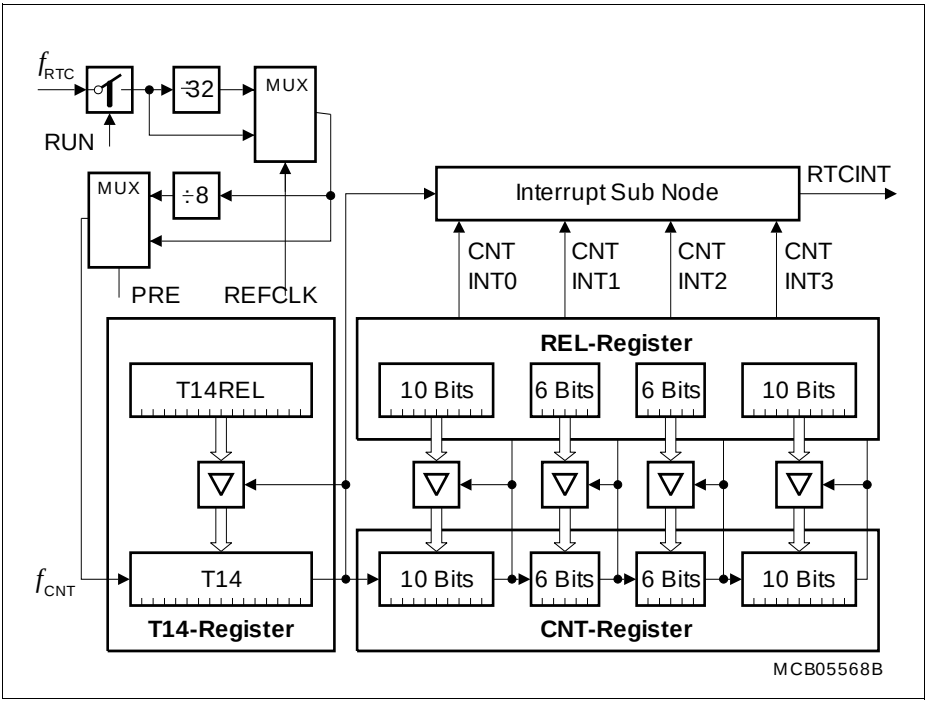

Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.

it overflows. If this is not the case because of a hardware or software failure, the Window Watchdog Timer overflows, generating a reset request.

The Window Watchdog Timer has a ‘programmable window boundary’, it disallows refresh during the Window Watchdog Timer’s count-up. A refresh during this window-boundary will cause the Window Watchdog Timer to also generate a reset request.

The Window Watchdog Timer is a 16-bit timer clocked with either the system clock or the independent wake-up oscillator clock, divided by 16,384 or 256. The Window Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Window Watchdog Timer is reloaded.

When clocked by f_{SYS} = 66 MHz, time intervals between 15.2 ns and 16.3 s can be monitored.

When clocked by f_{WU} = 500 kHz, time intervals between 2.0 µs and 2147.5 s can be monitored.

The default Watchdog Timer interval after power-up is 0.13 s (@ f_{WU} = 500 kHz).

3.15 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XE160FU from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on the EXTCLK pin.

4.3.3 Power Consumption

The power consumed by the XE160FU depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S and leakage current I_{LK} must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in most parts of domain DMP_M stopped.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
After a power reset, the decoupling capacitors for V_{DDIM} are charged with the maximum possible current.

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

Note: Operating Conditions apply.

Table 18 Switching Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT} CC	–	5.5 + 0.4 x f_{SYS} [1]	7 + 0.6 x f_{SYS} [1]	mA	power_mode= active ; voltage_range= both [2][3][4]
Power supply current in stopover mode, EVVRs on	I_{SSO} CC	–	0.7	2.0	mA	power_mode= stopover ; voltage_range= both

1) f_{SYS} in MHz

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) The pad supply voltage only has a minor influence on this parameter.

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XE160FU's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation.
2) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.
3) If a reduced analog reference voltage between 1V and V_{DDPB} / 2 is used, then there are additional decrease in the ADC speed and accuracy.
4) If the analog reference voltage range is below V_{DDPB} but still in the defined range of V_{DDPB} / 2 and V_{DDPB} is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain and Offset errors increase also by the factor 1/k.
5) If the analog reference voltage is > V_{DDPB}, then the ADC converter errors increase.
6) TUE is based on 12-bit conversion.
7) TUE is tested at V_{AREF} = V_{DDPB} = 5.0 V, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

Table 22 ADC Parameters for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input resistance of the selected analog channel	R_{AIN} CC	–	1.4	2.5	kOhm	not subject to production test 1)
Input resistance of the reference input	R_{AREF} CC	–	1.0	2.0	kOhm	not subject to production test 1)
Differential Non-Linearity Error 2)3)4)5)	$\|EA_{DNL}\|$ CC	–	2.5	5.5	LSB	
Gain Error 2)3)4)5)	$\|EA_{GAIN}\|$ CC	–	3.0	8.0	LSB	
Integral Non-Linearity 2)3)4)5)	$\|EA_{INL}\|$ CC	–	2.5	7.5	LSB	
Offset Error 2)3)4)5)	$\|EA_{OFF}\|$ CC	–	2.0	5.5	LSB	
Analog clock frequency	f_{ADCI} SR	2	–	16.7	MHz	Std. reference input (V_{AREF})
		2	–	12.1	MHz	Alt. reference input (CH0)
Total Unadjusted Error 3)4)	|TUE| CC	–	2.5	7.5	LSB	6)7)

Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Table 25 Coding of bit fields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1)]
0000_B	-	out of valid operation range
0001_B	3.0 V	LEV1V: reset request
0010_B - 0101_B	3.1 V - 3.4 V	step width is 0.1 V
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B - 1110_B	4.6 V - 5.0 V	step width is 0.1 V
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ±10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in **Table 26**.

Table 26 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B - 011_B	-	out of valid operation range
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request[2)]
110_B - 111_B	-	out of valid operation range

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

4.6 Flash Memory Parameters

The XE160FU is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE160FU's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 27 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	1[1)]		$N_{FL\_RD} \leq 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycles	$t_{RET} \geq$ 20 years
Flash wait states[2)]	$N_{WSFLASH}$ SR	1	–	–		$f_{SYS} \leq$ 8 MHz
		2	–	–		$f_{SYS} \leq$ 13 MHz
		3	–	–		$f_{SYS} \leq$ 17 MHz
		4	–	–		$f_{SYS} >$ 17 MHz
Erase time per sector/page	t_{ER} CC	–	7[3)]	8.0	ms	
Programming time per page	t_{PR} CC	–	3[3)]	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	years	$N_{ER} \leq$ 1,000 cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycles	

Table 31 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	0.8	mA	Driver_Strength = Medium
		–	–	1.0	mA	Driver_Strength = Strong
		–	–	0.15	mA	Driver_Strength = Weak
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	73 + 0.85 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	6 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Soft
		–	–	33 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	385 + 3.25 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 25 mA.

Table 33 is valid under the following conditions: C_L= 20 pF; *SSC*= master ; voltage_range= lower

Table 33 USIC SSC Master Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 10[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 9[1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-7	–	11	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 34 is valid under the following conditions: C_L= 20 pF; *SSC*= slave ; voltage_range= upper

Table 34 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	

Table 37 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 37 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	100[1)]	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	pad_type= standard
DAP1 valid per DAP0 clock period[2)]	t_{19} CC	87	92	–	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

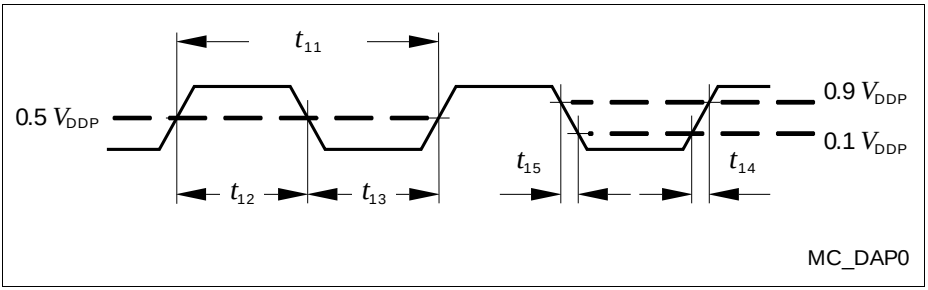

Figure 20 Test Clock Timing (DAP0)

Debug via SPD

The SPD interface will work with standard SPD tools having a sample/output clock frequency deviation of +/- 5% or less.

Note: For further details please refer to application note AP24004 in section SPD Timing Requirements.

Note: Operating Conditions apply.

5 Package and Reliability

The XE166 Family devices use the package type:

- PG-TSSOP (Plastic Green - Thin Shrink Small Outline Package)

The following specifications must be regarded to ensure proper integration of the XE160FU in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 40 Package Parameters (PG-TSSOP-38-8)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Power Dissipation	P_{DISS}	–	0.6	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	73	K/W	–

Package Compatibility Considerations

The XE160FU is a member of the XE166 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

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Published by Infineon Technologies AG