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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f038c6t7

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 38 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 10 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

Table 6. Comparison of I^2C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripheral can be served by the DMA controller.

Table 7. STM32F038x6 I^2C implementation

I^2C features(1)	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with extra output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

3.14 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds one universal synchronous/asynchronous receiver/transmitter (USART1) which communicates at speeds of up to 6 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interface can be served by the DMA controller.

Table 8. STM32F038x6 USART implementation

USART modes/features(1)	USART1
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection	X
Driver Enable	X

1. X = supported.

3.15 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

The SPI is able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 9. STM32F038x6 SPI/I^2S implementation

SPI features(1)	SPI
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I^2S mode	X
TI mode	X

1. X = supported.

3.16 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input-only pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		FTf	5 V-tolerant I/O, FM+ capable
		TTa	3.3 V-tolerant I/O directly connected to ADC
		POR	External power on reset pin with embedded weak pull-up resistor, powered from V_{DDA}
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. Pin definitions

Pin number					Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
1	-	-	-	-	VBAT	S	-	-	Backup power supply	
2	-	-	-	-	PC13	I/O	TC	(1)(2)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)(2)	-	OSC32_IN
4	-	-	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1)(2)	-	OSC32_OUT

Table 13. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-
PB2	-	-	-	-
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	-
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	-
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-
PB8	-	I2C1_SCL	TIM16_CH1	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10	-	I2C1_SCL	TIM2_CH3	-
PB11	EVENTOUT	I2C1_SDA	TIM2_CH4	-
PB12	SPI1_NSS	EVENTOUT	TIM1_BKIN	-
PB13	SPI1_SCK	-	TIM1_CH1N	-
PB14	SPI1_MISO	-	TIM1_CH2N	-
PB15	SPI1_MOSI	-	TIM1_CH3N	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 1.8 V and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

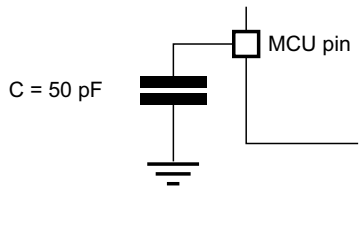
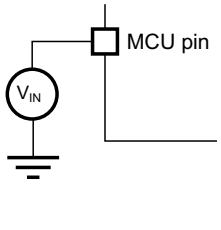


Figure 10. Pin input voltage



6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme

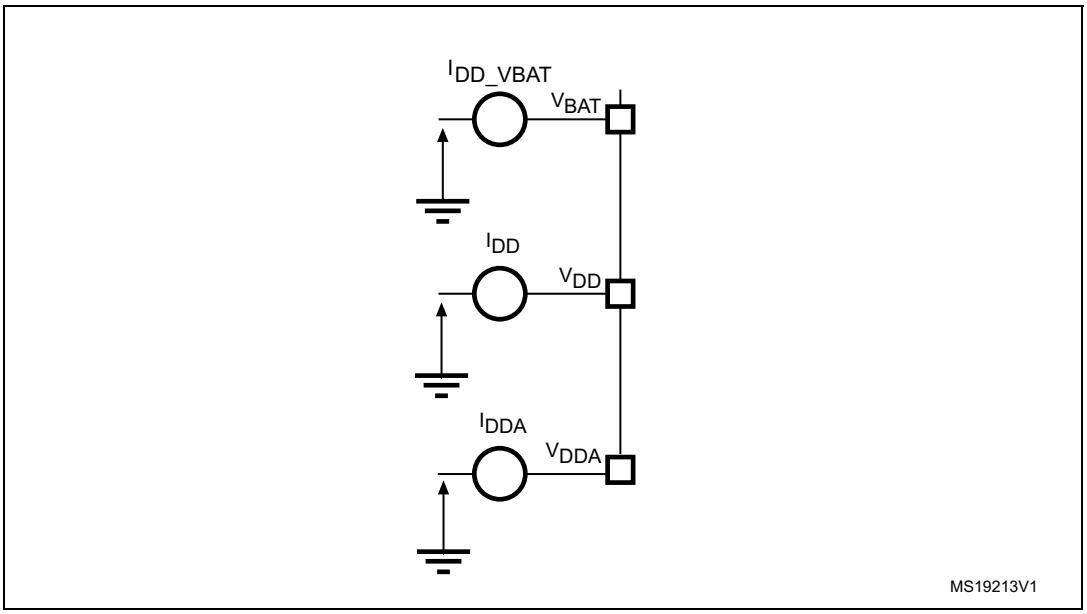


Table 22. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A (2)			Typ	Max @ T_A (2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSE bypass, PLL on	48 MHz	147	170	180	184	160	183	195	199	µA
			32 MHz	101	121	127	129	109	129	137	140	
			24 MHz	79	97	101	103	86	104	110	112	
		HSE bypass, PLL off	8 MHz	1	3	3	3	2	3	3	4	
			1 MHz	1	2	2	2	2	2	3	3	
		HSI clock, PLL on	48 MHz	219	243	256	260	240	267	279	284	
			32 MHz	172	195	203	206	190	210	222	226	
			24 MHz	150	170	177	180	165	186	193	196	
		HSI clock, PLL off	8 MHz	71	83	87	88	81	95	97	98	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.

Table 23. Typical and maximum consumption in Stop mode

Symbol	Parameter	Conditions	Typ. @ V_{DD} = 1.8 V							Max			Unit
			V_{DDA} = 1.8 V	V_{DDA} = 2.0 V	V_{DDA} = 2.4 V	V_{DDA} = 2.7 V	V_{DDA} = 3.0 V	V_{DDA} = 3.3 V	V_{DDA} = 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	All oscillators OFF	0.4							2.3	14.9	35.6	µA
I_{DDA}			0.8	0.8	0.8	0.9	0.9	1.0	1.1	1.5	2.6	3.4	

Table 25. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

Symbol	Parameter	f_{HCLK}	Typical consumption in Run mode		Typical consumption in Sleep mode		Unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	
I_{DD}	Current consumption from V_{DD} supply	48 MHz	18.5	11.6	10.8	2.6	mA
		36 MHz	14.1	8.9	8.2	2.0	
		32 MHz	12.7	8.1	7.3	1.8	
		24 MHz	9.7	6.2	5.6	1.4	
		16 MHz	6.7	4.3	3.9	1.1	
		8 MHz	3.4	2.3	1.9	0.6	
		4 MHz	2.1	1.4	1.3	0.5	
		2 MHz	1.3	0.9	0.9	0.5	
		1 MHz	0.9	0.7	0.7	0.4	
		500 kHz	0.7	0.6	0.6	0.4	
I_{DDA}	Current consumption from V_{DDA} supply	48 MHz	136				µA
		36 MHz	105				
		32 MHz	96				
		24 MHz	76				
		16 MHz	56				
		8 MHz	1				
		4 MHz	1				
		2 MHz	1				
		1 MHz	1				
		500 kHz	1				

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 44: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt

6.3.5 Wakeup time from low-power mode

The wakeup times given in *Table 28* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode.

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*..

Table 28. Low-power mode wakeup timings

Symbol	Parameter	Typ @ V_{DDA}		Max	Unit
		= 1.8 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	3.5	2.8	5.3	µs
$t_{WUSLEEP}$	Wakeup from Sleep mode	4 SYSCLK cycles		-	µs

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 13: High-speed external clock source AC timing diagram*.

Table 29. High-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

1. Guaranteed by design, not tested in production.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 31*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
		V_{DD} = 1.8 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 15*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Table 43. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on all FT, FTf and POR pins	–5	NA	
	Injected current on all TTa, TC and RESET pins	–5	+5	

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under the conditions summarized in *Table 18: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 44. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DDIOx}+0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475\ V_{DDIOx}-0.2^{(1)}$	
		BOOT0	-	-	$0.3\ V_{DDIOx}-0.3^{(1)}$	
		All I/Os except BOOT0 pin	-	-	$0.3\ V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DDIOx}+0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5\ V_{DDIOx}+0.2^{(1)}$	-	-	
		BOOT0	$0.2\ V_{DDIOx}+0.95^{(1)}$	-	-	
		All I/Os except BOOT0 pin	$0.7\ V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(1)}$	-	mV
		FT and FTf I/O	-	$100^{(1)}$	-	
		BOOT0	-	$300^{(1)}$	-	
I_{lkg}	Input leakage current(2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O $V_{DDIOx} \le V_{IN} \le 5$ V	-	-	10	

Figure 19. TC and TTa I/O input characteristics

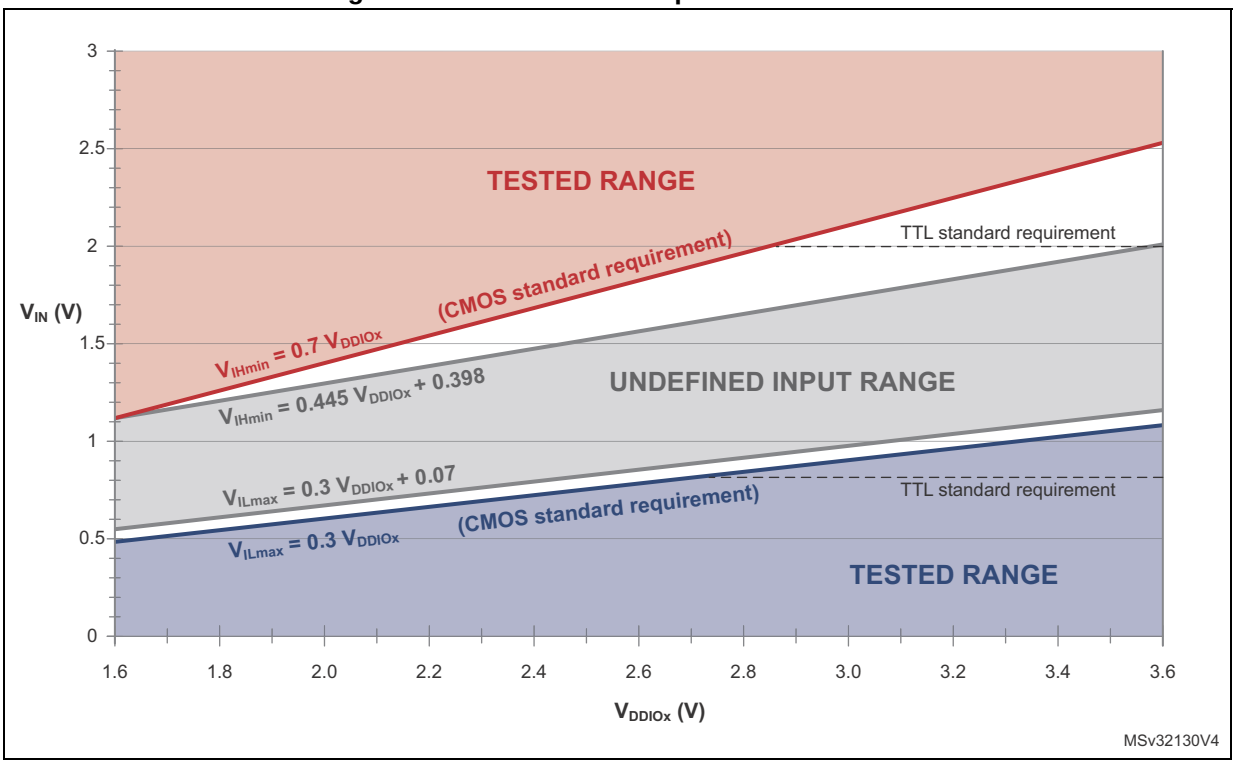
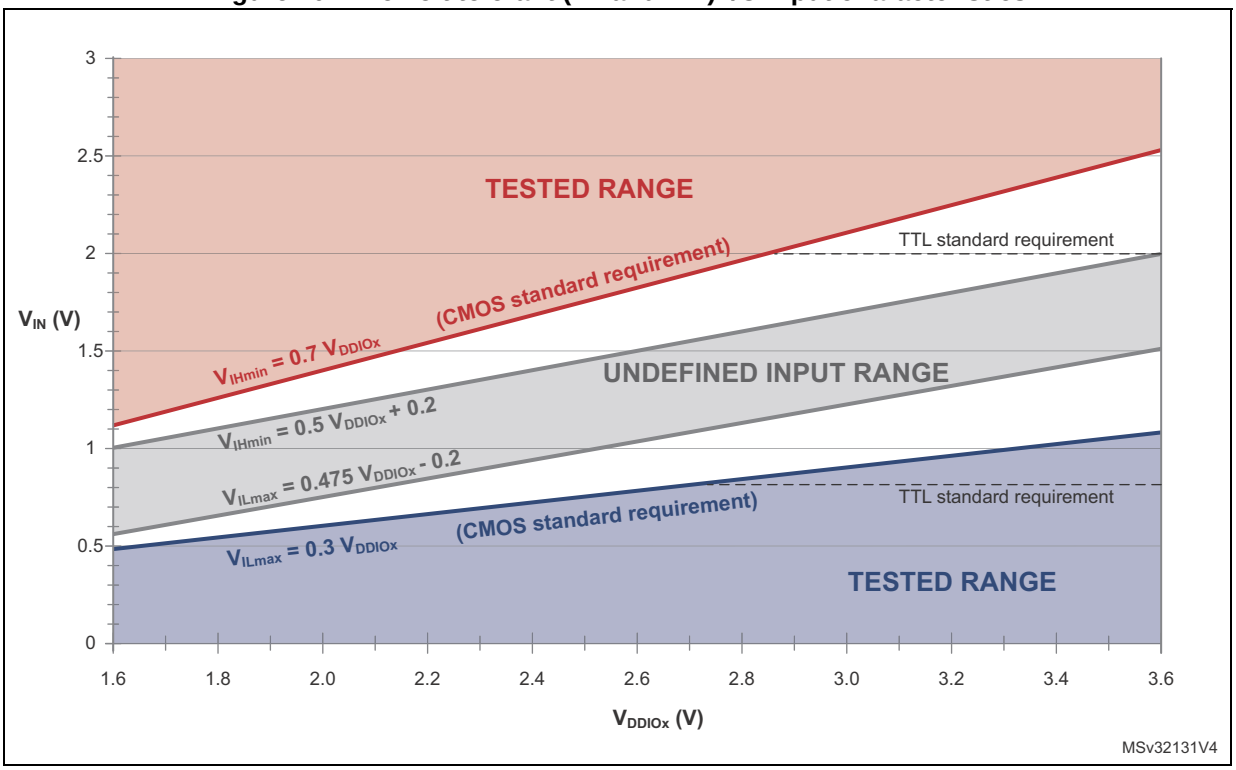


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 15: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 15: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 45. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	V
V_{OLFm+}(3)	Output low level voltage for an FTf I/O pin in Fm+ mode	$\|I_{IO}\|$ = 10 mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 15: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. Data based on characterization results. Not tested in production.
3. Data based on design simulation only. Not tested in production.

Table 49. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$W_{LATENCY}$(2)(4)	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(2)	Trigger conversion latency	f_{ADC} = f_{PCLK}/2 = 14 MHz	0.196			µs
		f_{ADC} = f_{PCLK}/2	5.5			1/f_{PCLK}
		f_{ADC} = f_{PCLK}/4 = 12 MHz	0.219			µs
		f_{ADC} = f_{PCLK}/4	10.5			1/f_{PCLK}
		f_{ADC} = f_{HSI14} = 14 MHz	0.179	-	0.250	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	f_{ADC} = f_{HSI14}	-	1	-	1/f_{HSI14}
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	1/f_{ADC}
t_{STAB}(2)	Stabilization time	-	14			1/f_{ADC}
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			1/f_{ADC}

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 50. R_{AIN} max for f_{ADC} = 14 MHz

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4

Table 55. IWDG min/max timeout period at 40 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 56. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.19 Communication interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.13: I/O port characteristics* for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Figure 25. SPI timing diagram - slave mode and CPHA = 0

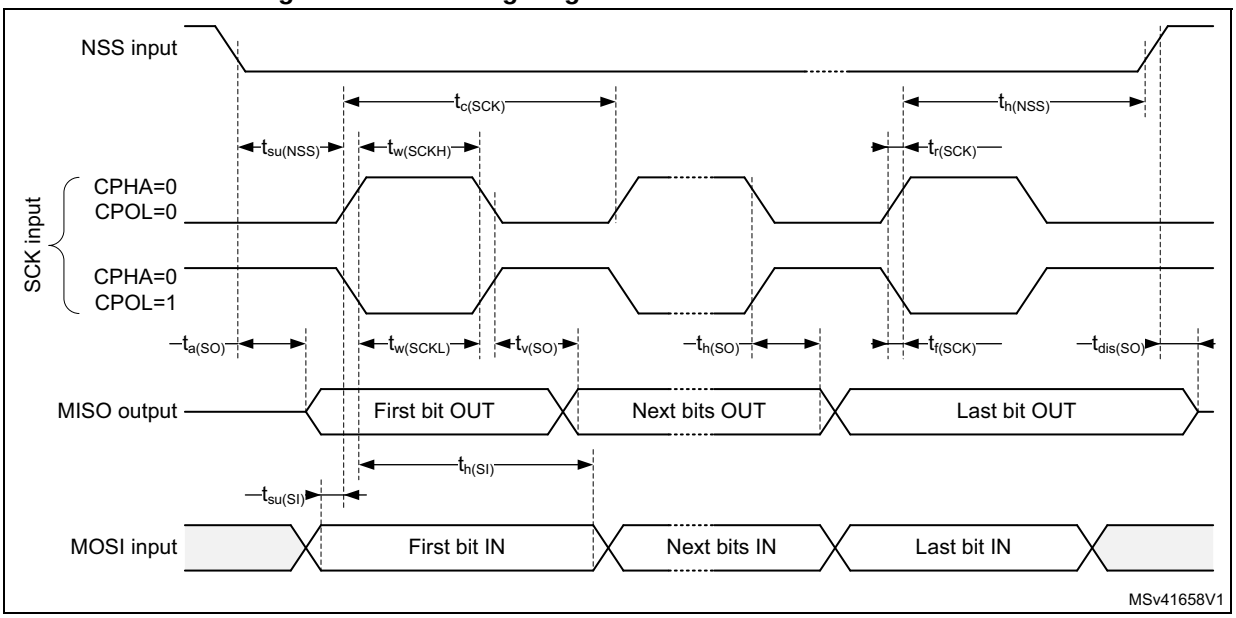
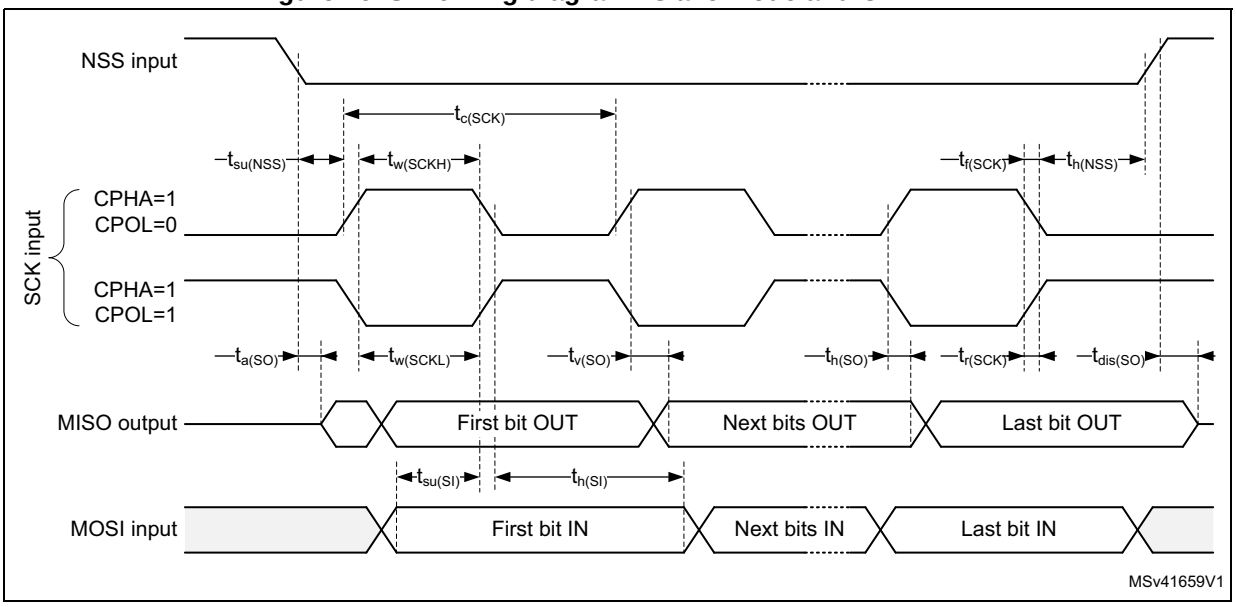
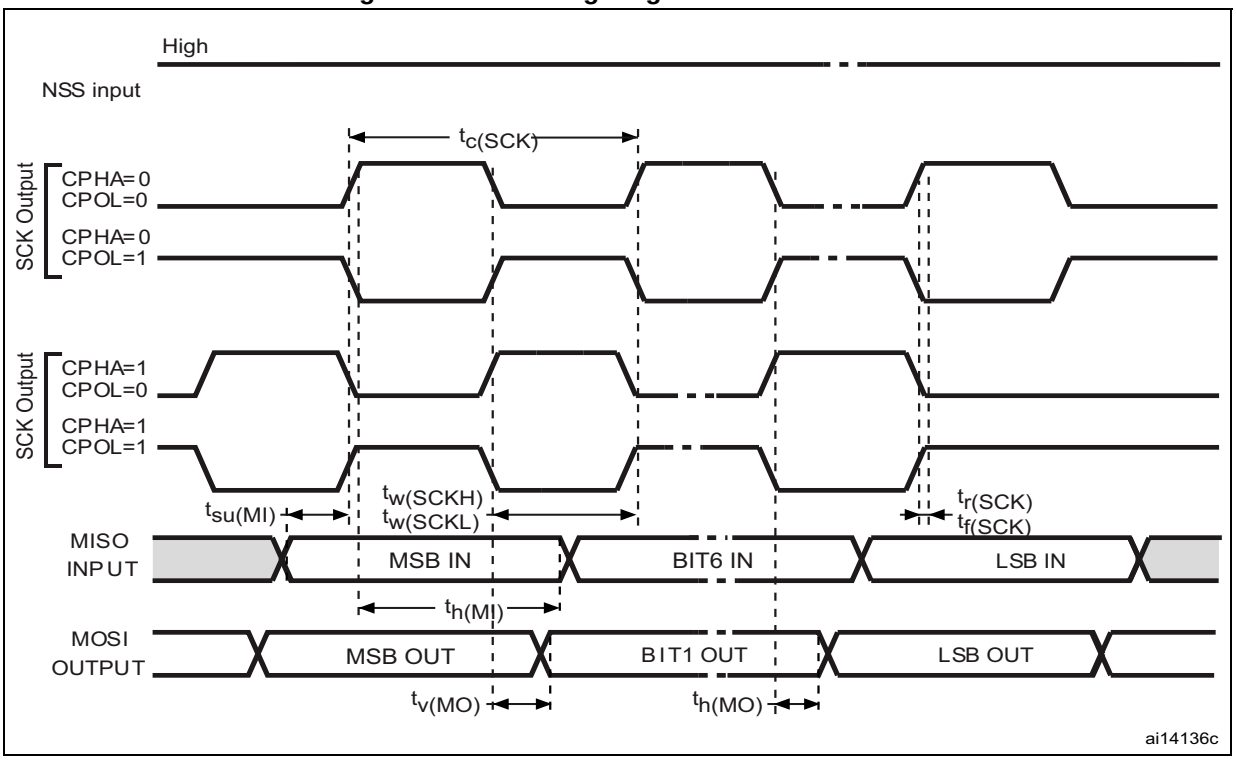


Figure 26. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 27. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 59. I^2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I^2S clock rise time	Capacitive load C_L = 15 pF	-	10	ns
$t_{f(CK)}$	I^2S clock fall time		-	12	
$t_{w(CKH)}$	I^2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I^2S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I^2S slave input clock duty cycle	Slave mode	25	75	%