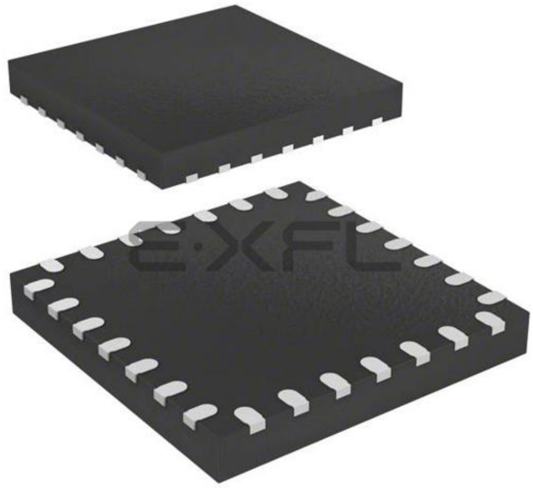

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f038g6u6

Contents

List of tables

3 Functional overview

Figure 1 shows the general block diagram of the STM32F038x6 devices.

3.1 ARM®-Cortex®-M0 core

The ARM® Cortex®-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F038x6 devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 4 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 32 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

Table 14. STM32F038x6 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 0C00 - 0x4800 13FF	2KB	Reserved
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1KB	TIM17
	0x4001 4400 - 0x4001 47FF	1KB	TIM16
	0x4001 3C00 - 0x4001 43FF	2KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1KB	USART1
	0x4001 3400 - 0x4001 37FF	1KB	Reserved
	0x4001 3000 - 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1KB	Reserved
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 0800 - 0x4001 23FF	7KB	Reserved
	0x4001 0400 - 0x4001 07FF	1KB	EXTI
	0x4001 0000 - 0x4001 03FF	1KB	SYSCFG
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 1.8 V and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

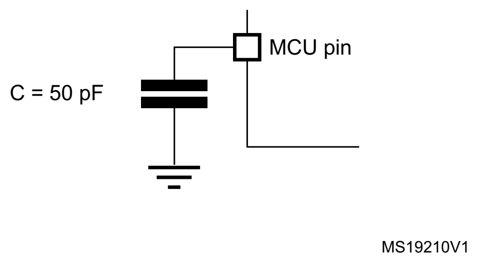
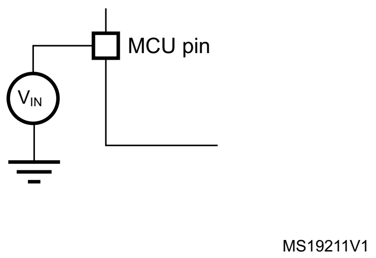
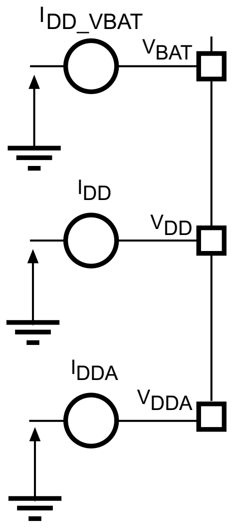


Figure 10. Pin input voltage



6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics* and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 15. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage	–0.3	1.95	V
$V_{DDA}–V_{SS}$	External analog supply voltage	- 0.3	4.0	V
$V_{DD}–V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
$V_{BAT}–V_{SS}$	External backup supply voltage	- 0.3	4.0	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DDIOx} + 4.0 (3)	V
	Input voltage on POR pins	V_{SS} –0.3	4.0	V
	Input voltage on TTa pins	V_{SS} –0.3	4.0	V
	BOOT0	0	9.0	V
	Input voltage on any other pin	V_{SS} –0.3	4.0	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 16: Current characteristics*for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 19. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reference voltage

The parameters given in *Table 20* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 20. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10(1)	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4(1)	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10(1)	mV
T_{Coeff}	Temperature coefficient	-	- 100(1)	-	100(1)	ppm/°C
$T_{VREFINT\_RDY}$(2)	Internal reference voltage temporization	-	1.5	2.5	4.5	ms

1. Guaranteed by design, not tested in production.
2. Guaranteed by design, not tested in production. This parameter is the latency between the time when pin NPOR is set to 1 by the application and the time when the VREFINTRDYF status bit is set to 1 by the hardware.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 22. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSE bypass, PLL on	48 MHz	147	170	180	184	160	183	195	199	µA
			32 MHz	101	121	127	129	109	129	137	140	
			24 MHz	79	97	101	103	86	104	110	112	
		HSE bypass, PLL off	8 MHz	1	3	3	3	2	3	3	4	
			1 MHz	1	2	2	2	2	2	3	3	
		HSI clock, PLL on	48 MHz	219	243	256	260	240	267	279	284	
			32 MHz	172	195	203	206	190	210	222	226	
			24 MHz	150	170	177	180	165	186	193	196	
		HSI clock, PLL off	8 MHz	71	83	87	88	81	95	97	98	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.

Table 23. Typical and maximum consumption in Stop mode

Symbol	Parameter	Conditions	Typ. @ V_{DD} = 1.8 V							Max			Unit
			V_{DDA} = 1.8 V	V_{DDA} = 2.0 V	V_{DDA} = 2.4 V	V_{DDA} = 2.7 V	V_{DDA} = 3.0 V	V_{DDA} = 3.3 V	V_{DDA} = 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	All oscillators OFF	0.4							2.3	14.9	35.6	µA
I_{DDA}			0.8	0.8	0.8	0.9	0.9	1.0	1.1	1.5	2.6	3.4	

High-speed internal (HSI) RC oscillator

Table 33. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 17. HSI oscillator accuracy characterization results for soldered parts

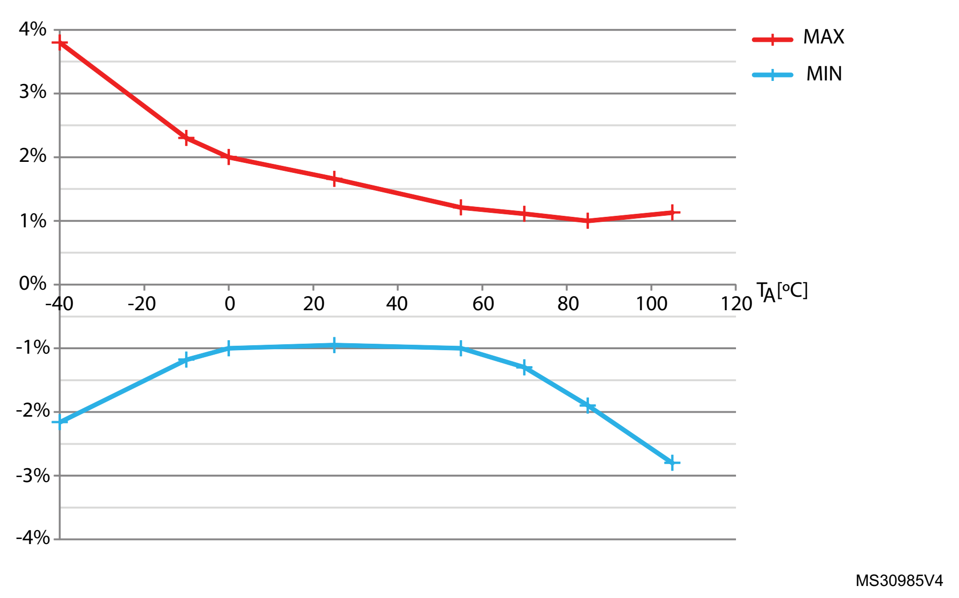


Figure 19. TC and TTa I/O input characteristics

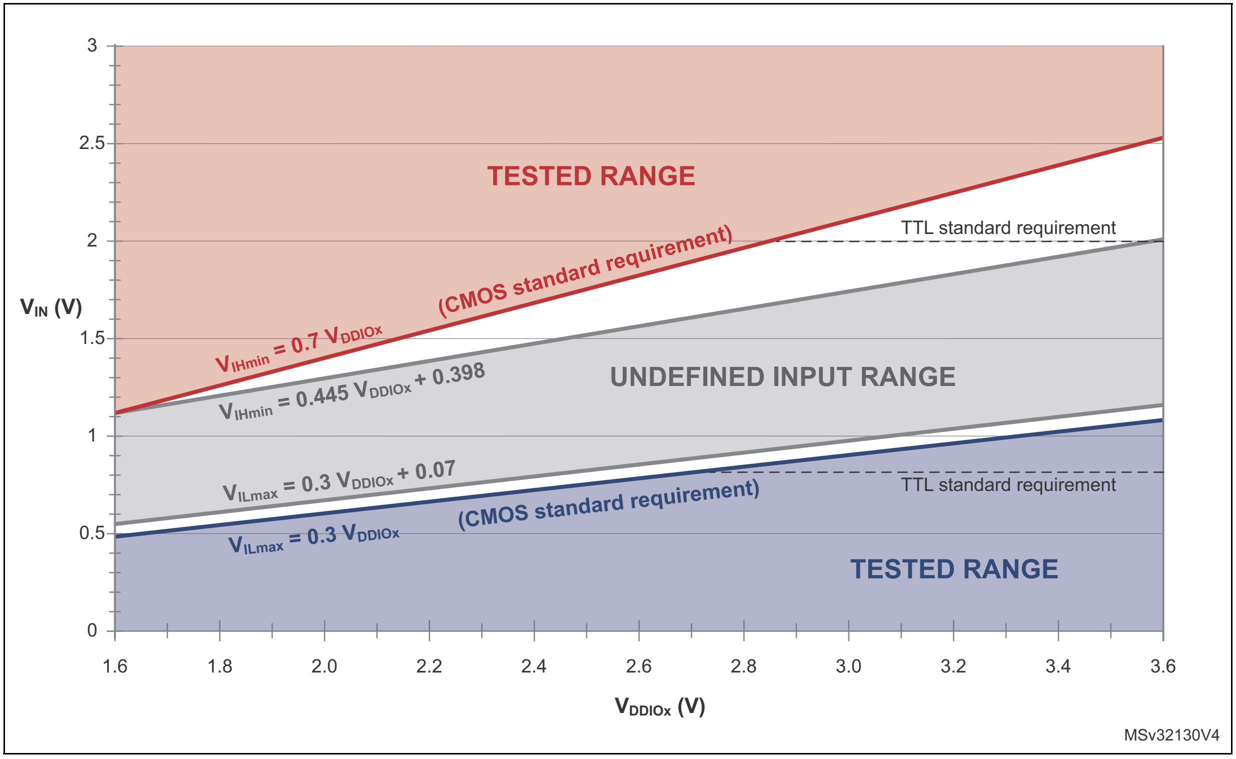
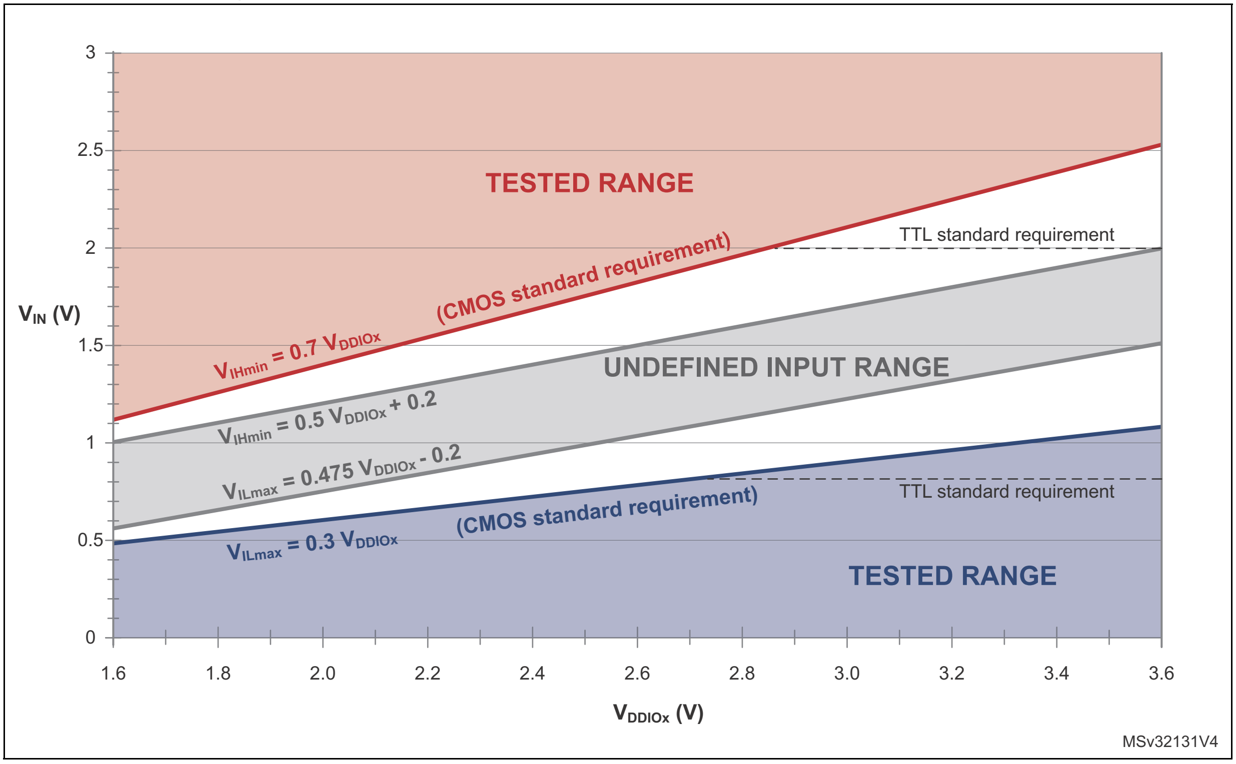


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics



6.3.14 NRST and NPOR pin characteristics

NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

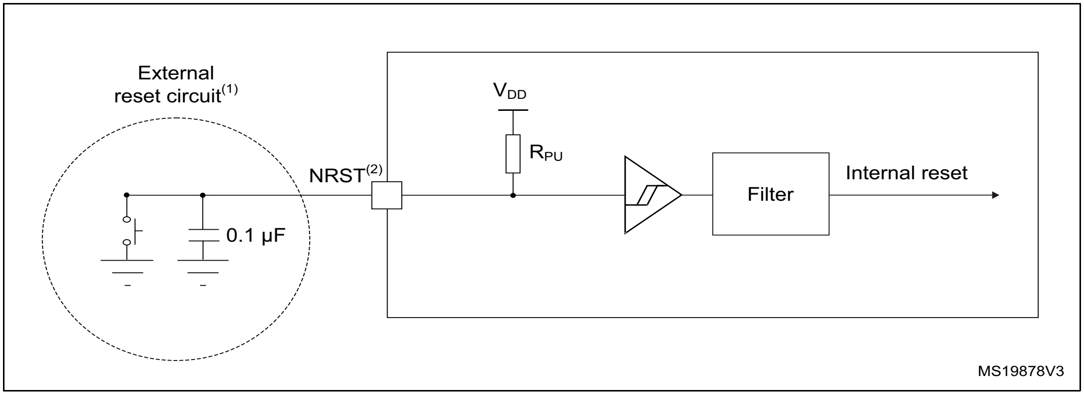
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 47. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3\ V_{DD}+0.07^{(1)}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.445\ V_{DD}+0.398^{(1)}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	700(1)	-	-	ns

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 22. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 47: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

NPOR pin characteristics

The NPOR pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor to the V_{DDA}, R_{PU}.

Unless otherwise specified, the parameters given in *Table 48* below are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

6.3.16 Temperature sensor characteristics

Table 52. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	± 1	± 2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{30}	Voltage at 30 °C (± 5 °C)(2)	1.34	1.43	1.52	V
t_{START}(1)	ADC_IN16 buffer startup time	-	-	10	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	4	-	-	µs

1. Guaranteed by design, not tested in production.
2. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 3: Temperature sensor calibration values*.

6.3.17 V_{BAT} monitoring characteristics

Table 53. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	kΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	–1	-	+1	%
t_{S_vbat}(1)	ADC sampling time when reading the V_{BAT}	4	-	-	µs

1. Guaranteed by design, not tested in production.

6.3.18 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 54. TIMx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	1365	-	µs
	32-bit counter maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	-	s

Table 55. IWDG min/max timeout period at 40 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 56. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.19 Communication interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.13: I/O port characteristics* for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 57. I^{2}C analog filter characteristics[1]

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50[2]	260[3]	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I^{2}S characteristics

Unless otherwise specified, the parameters given in *Table 58* for SPI or in *Table 59* for I^{2}S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 18: General operating conditions*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^{2}S).

Table 58. SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$[2]	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$[3]	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

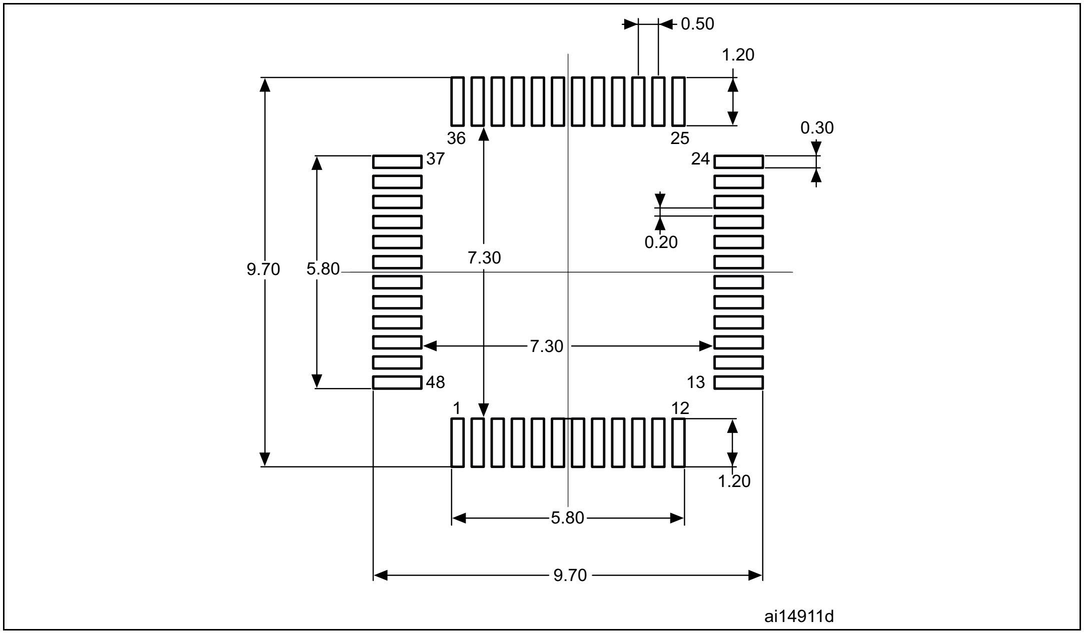
1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Table 60. LQFP48 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 31. Recommended footprint for LQFP48 package



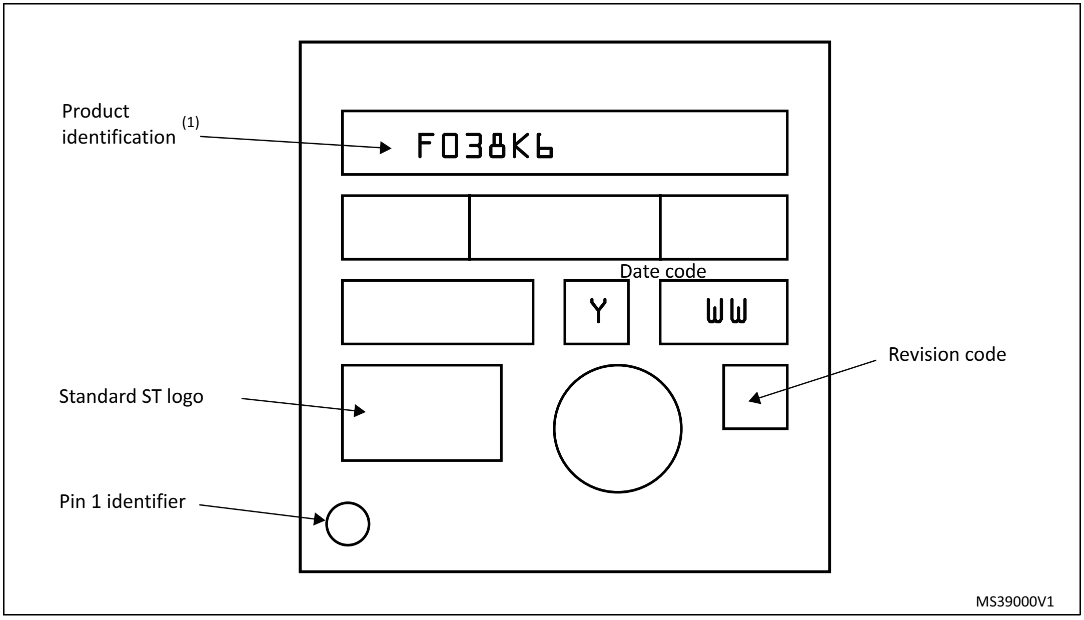
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 35. UFQFPN32 package marking example

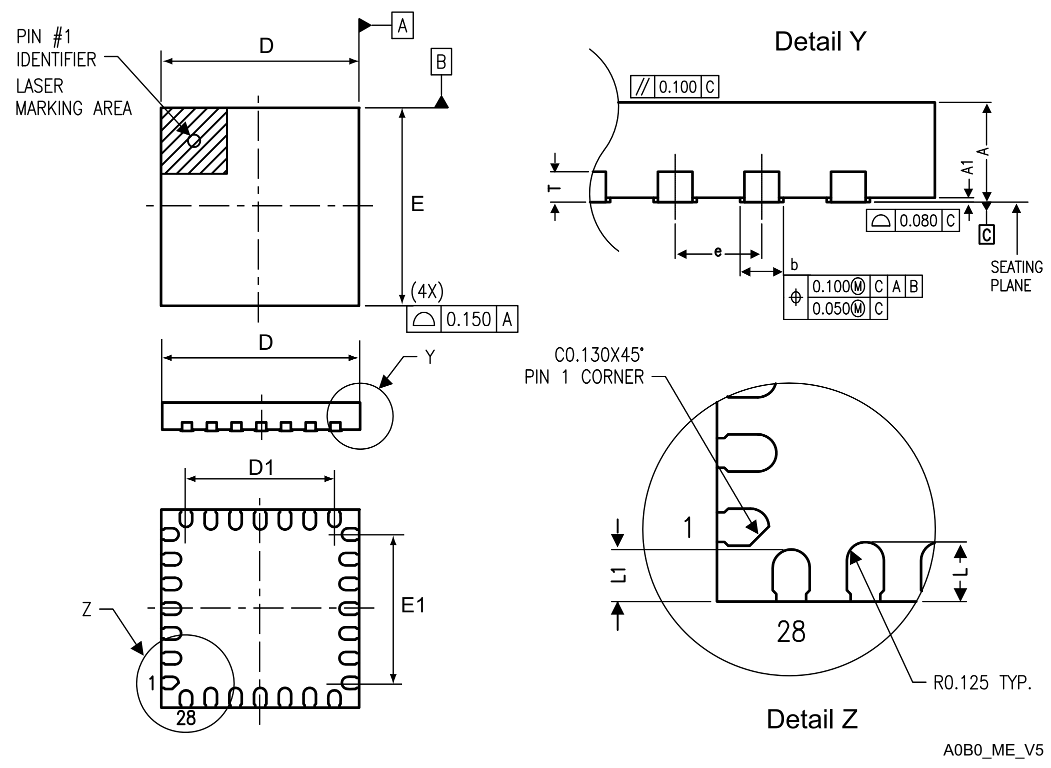


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 UFQFPN28 package information

UFQFPN28 is a 28-lead, 4x4 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 36. UFQFPN28 package outline



1. Drawing is not to scale.

Table 62. UFQFPN28 package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

7.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F038x6 at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 80 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

$P_{INTmax} = 50 \text{ mA} \times 3.5 \text{ V} = 175 \text{ mW}$

$P_{IOmax} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} + 8 \times 20 \text{ mA} \times 1.3 \text{ V} = 272 \text{ mW}$

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

$P_{Dmax} = 175 + 272 = 447 \text{ mW}$

Using the values obtained in *Table 66* T_{Jmax} is calculated as follows:

– For LQFP48, 55 °C/W

$T_{Jmax} = 80\ °C + (55°C/W \times 447 \text{ mW}) = 80\ °C + 24.585\ °C = 104.585\ °C$

This is within the range of the suffix 6 version parts ($–40 < T_J < 105$ °C) see *Table 18: General operating conditions*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

Note: With this given P_{Dmax} we can find the TAmax allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: $T_{Amax} = T_{Jmax} - (55°C/W \times 447 \text{ mW}) = 105-24.585 = 80.415\ °C$

Suffix 7: $T_{Amax} = T_{Jmax} - (55°C/W \times 447 \text{ mW}) = 125-24.585 = 100.415\ °C$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.