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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	12MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36902gfhsww

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules

- CPU and System-Control Modules
- On-Chip Peripheral Modules

The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

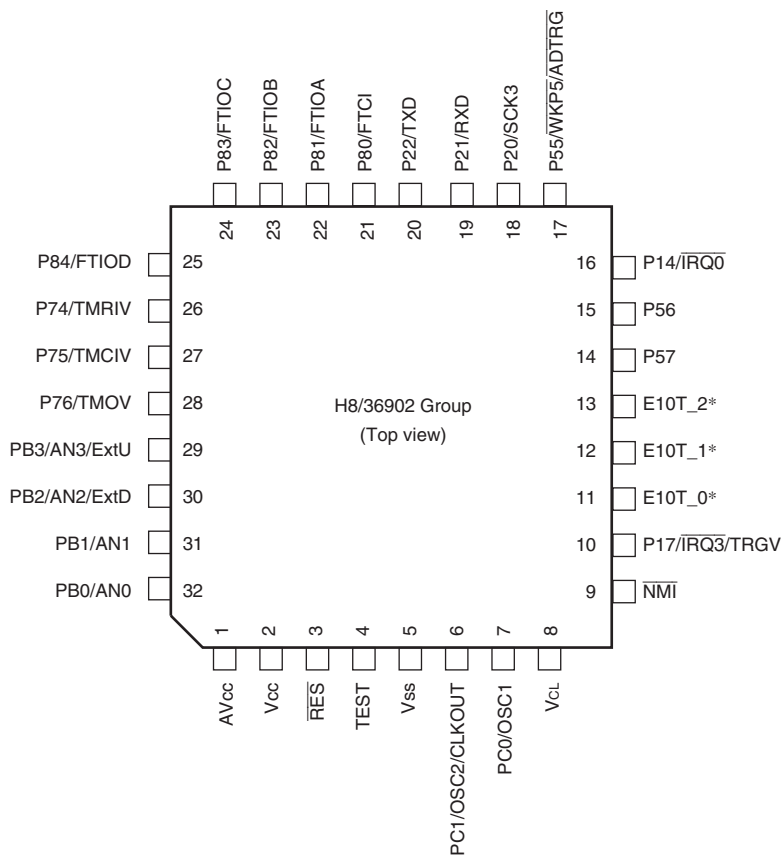
- i) Feature
- ii) Input/Output Pin
- iii) Register Description
- iv) Operation
- v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

11. Index



Note: * Can also be used for the E7 or E8 emulator.

Figure 1.4 Pin Arrangement of H8/36902 Group (FP-32A)

(2) Register Indirect—@ERn

The register field of the instruction code specifies an address register (ERn), the lower 24 bits of which contain the address of the operand on memory.

(3) Register Indirect with Displacement—@(d:16, ERn) or @(d:24, ERn)

A 16-bit or 24-bit displacement contained in the instruction is added to an address register (ERn) specified by the register field of the instruction, and the lower 24 bits of the sum the address of a memory operand. A 16-bit displacement is sign-extended when added.

(4) Register Indirect with Post-Increment or Pre-Decrement—@ERn+ or @-ERn

- Register indirect with post-increment—@ERn+

The register field of the instruction code specifies an address register (ERn) the lower 24 bits of which contains the address of a memory operand. After the operand is accessed, 1, 2, or 4 is added to the address register contents (32 bits) and the sum is stored in the address register. The value added is 1 for byte access, 2 for word access, or 4 for longword access. For the word or longword access, the register value should be even.

- Register indirect with pre-decrement—@-ERn

The value 1, 2, or 4 is subtracted from an address register (ERn) specified by the register field in the instruction code, and the lower 24 bits of the result is the address of a memory operand. The result is also stored in the address register. The value subtracted is 1 for byte access, 2 for word access, or 4 for longword access. For the word or longword access, the register value should be even.

(5) Absolute Address—@aa:8, @aa:16, @aa:24

The instruction code contains the absolute address of a memory operand. The absolute address may be 8 bits long (@aa:8), 16 bits long (@aa:16), 24 bits long (@aa:24)

For an 8-bit absolute address, the upper 16 bits are all assumed to be 1 (H'FFFF). For a 16-bit absolute address the upper 8 bits are a sign extension. A 24-bit absolute address can access the entire address space.

The access ranges of absolute addresses for the group of this LSI are those shown in table 2.11, because the upper 8 bits are ignored.

7.3.2 Programming/Erasing in User Program Mode

On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user program/erase control program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the user program/erase control program or a program that provides the user program/erase control program from external memory. As the flash memory itself cannot be read during programming/erasing, transfer the user program/erase control program to on-chip RAM, as in boot mode. Figure 7.2 shows a sample procedure for programming/erasing in user program mode.

Prepare a user program/erase control program in accordance with the description in section 7.4, Flash Memory Programming/Erasing.

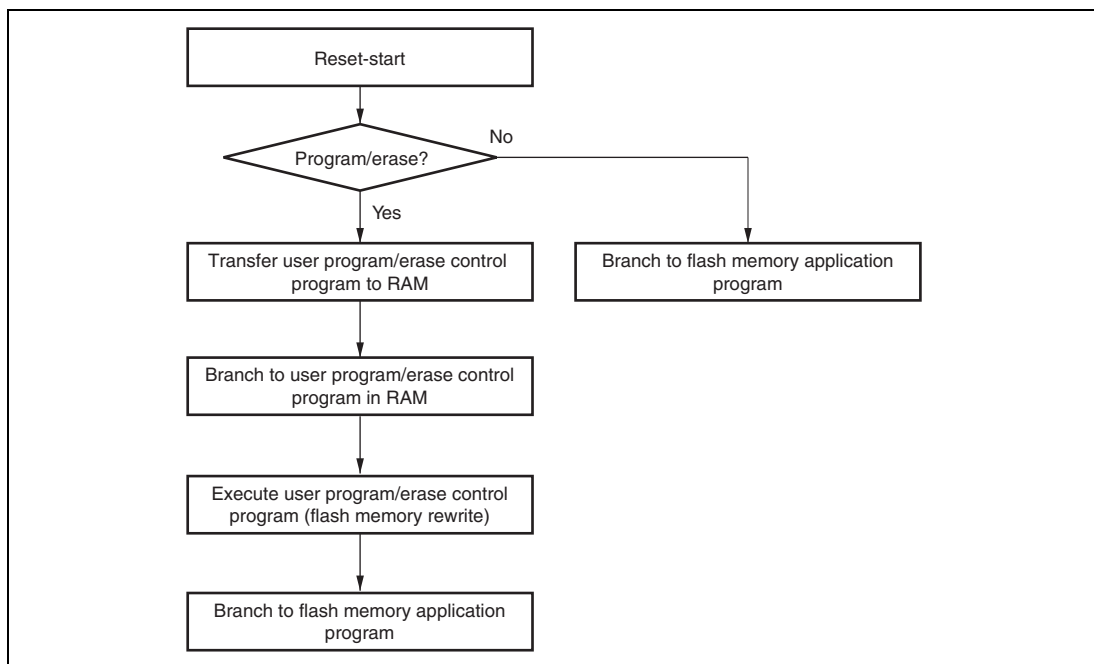


Figure 7.2 Programming/Erasing Flowchart Example in User Program Mode

10.3 Operation

10.3.1 Interval Timer Operation

When bit TMB17 in TMB1 is cleared to 0, timer B1 functions as an 8-bit interval timer. Upon reset, TCB1 is cleared to H'00 and bit TMB17 is cleared to 0, so up-counting and interval timing resume immediately. The operating clock of timer B1 is selected from seven internal clock signals output by prescaler S. The selection is made by the TMB12 to TMB10 bits in TMB1.

After the count value in TMB1 reaches H'FF, the next clock signal input causes timer B1 to overflow, setting flag IRRTB1 in IRR2 to 1. If IENTB1 in IENR2 is 1, an interrupt is requested to the CPU.

At overflow, TCB1 returns to H'00 and starts counting up again. During interval timer operation (TMB17 = 0), when a value is set in TLB1, the same value is set in TCB1.

10.3.2 Auto-Reload Timer Operation

Setting bit TMB17 in TMB1 to 1 causes timer B1 to function as an 8-bit auto-reload timer. When a reload value is set in TLB1, the same value is loaded into TCB1, becoming the value from which TCB1 starts its count. After the count value in TCB1 reaches H'FF, the next clock signal input causes timer B1 to overflow. The TLB1 value is then loaded into TCB1, and the count continues from that value. The overflow period can be set within a range from 1 to 256 input clocks, depending on the TLB1 value.

The clock sources and interrupts in auto-reload mode are the same as in interval mode. In auto-reload mode (TMB17 = 1), when a new value is set in TLB1, the TLB1 value is also loaded into TCB1.

10.4 Timer B1 Operating Modes

Table 10.1 shows the timer B1 operating modes.

Table 10.1 Timer B1 Operating Modes

Operating Mode		Reset	Active	Sleep	Subsleep	Standby
TCB1	Interval	Reset	Functions	Functions	Halted	Halted
	Auto-reload	Reset	Functions	Functions	Halted	Halted
TMB1		Reset	Functions	Retained	Retained	Retained

11.3.2 Time Constant Registers A and B (TCORA, TCORB)

TCORA and TCORB have the same function.

TCORA and TCORB are 8-bit read/write registers.

TCORA and TCNTV are compared at all times. When the TCORA and TCNTV contents match, CMFA is set to 1 in TCSR.V. If CMIEA is also set to 1 in TCR.V0, a CPU interrupt is requested. Note that they must not be compared during the T3 state of a TCORA write cycle.

Timer output from the TMOV pin can be controlled by the identifying signal (compare match A) and the settings of bits OS3 to OS0 in TCSR.V.

TCORA and TCORB are initialized to H'FF.

11.3.3 Timer Control Register V0 (TCRV0)

TCRV0 selects the input clock signals of TCNTV, specifies the clearing conditions of TCNTV, and controls each interrupt request.

Bit	Bit Name	Initial Value	R/W	Description
7	CMIEB	0	R/W	Compare Match Interrupt Enable B When this bit is set to 1, interrupt request from the CMFB bit in TCSR.V is enabled.
6	CMIEA	0	R/W	Compare Match Interrupt Enable A When this bit is set to 1, interrupt request from the CMFA bit in TCSR.V is enabled.
5	OVIE	0	R/W	Timer Overflow Interrupt Enable When this bit is set to 1, interrupt request from the OVF bit in TCSR.V is enabled.

11.6 Usage Notes

The following types of contention or operation can occur in timer V operation.

1. Writing to registers is performed in the T3 state of a TCNTV write cycle. If a TCNTV clear signal is generated in the T3 state of a TCNTV write cycle, as shown in figure 11.11, clearing takes precedence and the write to the counter is not carried out. If counting-up is generated in the T3 state of a TCNTV write cycle, writing takes precedence.
2. If a compare match is generated in the T3 state of a TCORA or TCORB write cycle, the write to TCORA or TCORB takes precedence and the compare match signal is inhibited. Figure 11.12 shows the timing.
3. If compare matches A and B occur simultaneously, any conflict between the output selections for compare match A and compare match B is resolved by the following priority: toggle output > output 1 > output 0.
4. Depending on the timing, TCNTV may be incremented by a switch between different internal clock sources. When TCNTV is internally clocked, an increment pulse is generated from the falling edge of an internal clock signal, that is divided system clock (ϕ). Therefore, as shown in figure 11.13 the switch is from a high clock signal to a low clock signal, the switchover is seen as a falling edge, causing TCNTV to increment. TCNTV can also be incremented by a switch between internal and external clocks.

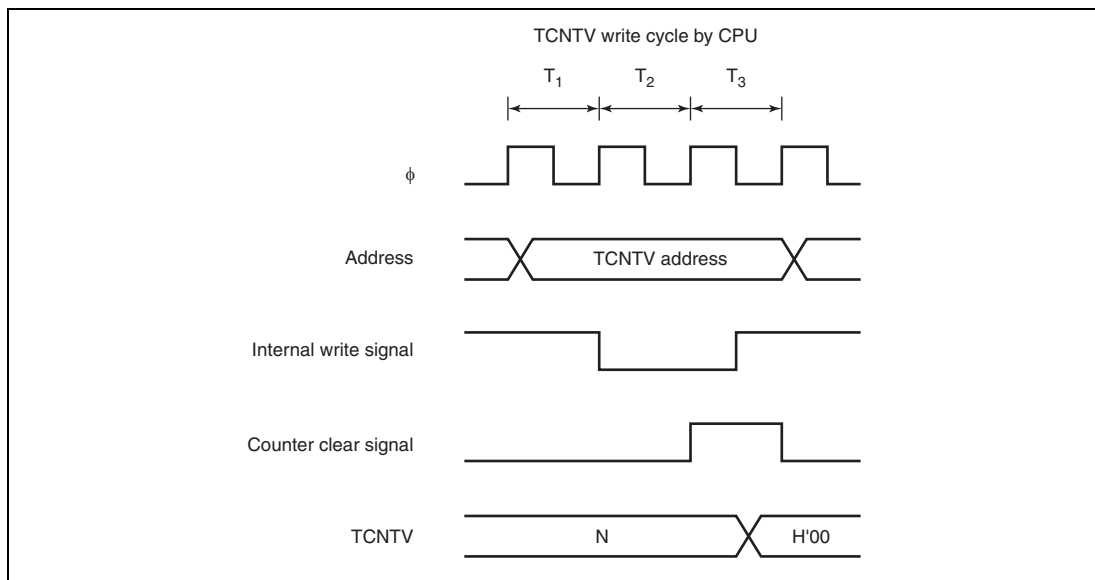


Figure 11.11 Contention between TCNTV Write and Clear

12.5.5 Buffer Operation Timing

Figures 12.19 and 12.20 show the buffer operation timing.

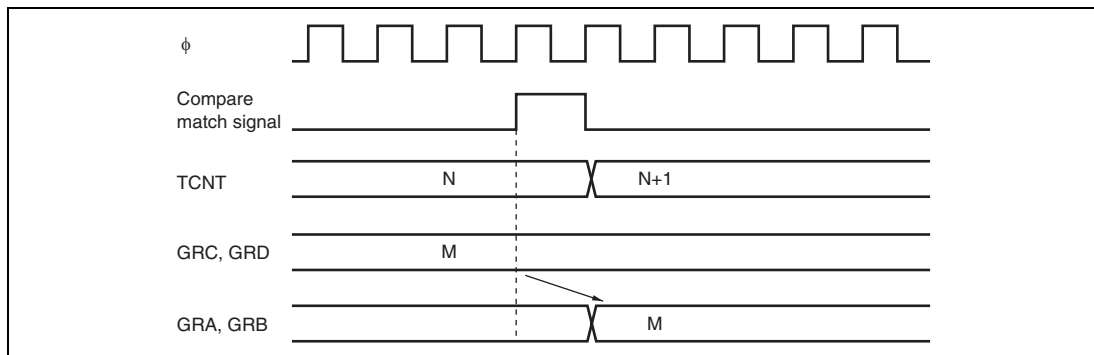


Figure 12.19 Buffer Operation Timing (Compare Match)

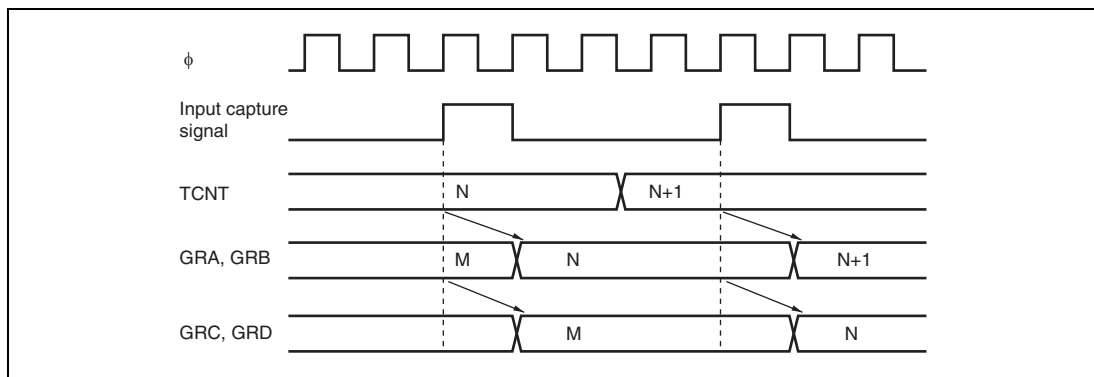
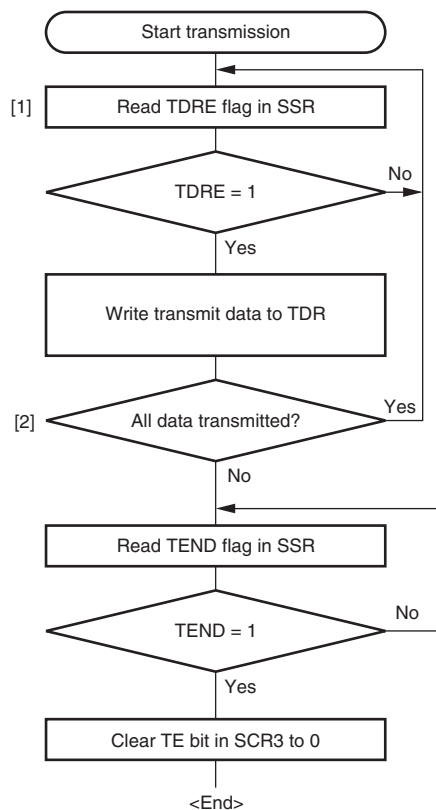


Figure 12.20 Buffer Operation Timing (Input Capture)



- [1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0 and clocks are output to start the data transmission.
- [2] To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.

Figure 14.12 Sample Serial Transmission Flowchart (Clocked Synchronous Mode)

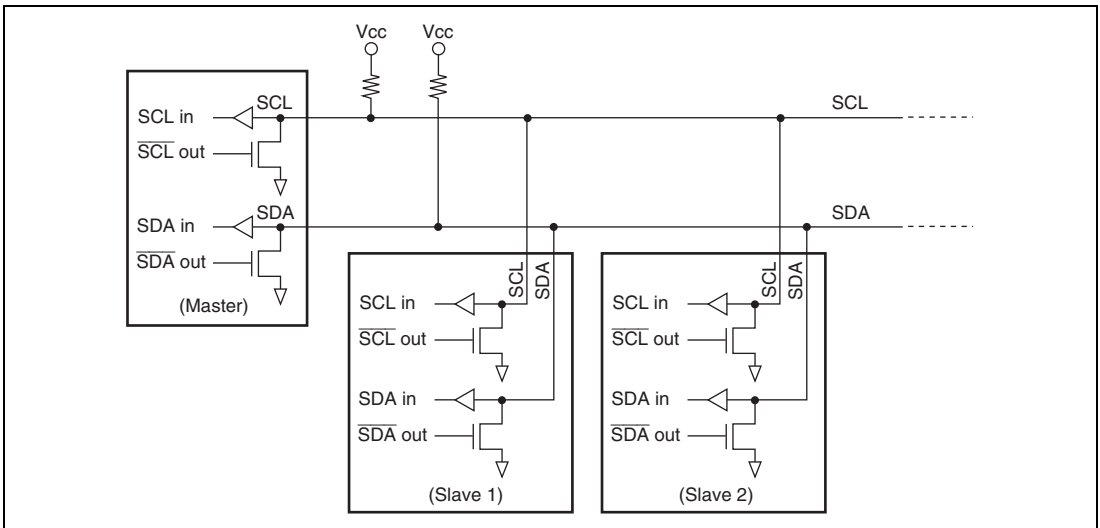


Figure 15.2 External Circuit Connections of I/O Pins

15.2 Input/Output Pins

Table 15.1 summarizes the input/output pins used by the I²C bus interface 2.

Table 15.1 Pin Configuration

Name	Abbreviation	I/O	Function
Serial clock	SCL	I/O	I ² C serial clock input/output
Serial data	SDA	I/O	I ² C serial data input/output

Bit	Bit Name	Initial Value	R/W	Description
3	SCLO	1	R	This bit monitors SCL output level. When SCLO is 1, SCL pin outputs high. When SCLO is 0, SCL pin outputs low.
2	—	1	—	Reserved This bit is always read as 1.
1	IICRST	0	R/W	IIC Control Part Reset This bit resets the control part except for I ² C registers. If this bit is set to 1 when hang-up occurs because of communication failure during I ² C operation, I ² C control part can be reset without setting ports and initializing registers.
0	—	1	—	Reserved This bit is always read as 1.

15.3.3 I²C Bus Mode Register (ICMR)

ICMR selects whether the MSB or LSB is transferred first, performs master mode wait control, and selects the transfer bit count.

Bit	Bit Name	Initial Value	R/W	Description
7	MLS	0	R/W	MSB-First/LSB-First Select 0: MSB-first 1: LSB-first Set this bit to 0 when the I ² C bus format is used.
6	WAIT	0	R/W	Wait Insertion Bit In master mode with the I ² C bus format, this bit selects whether to insert a wait after data transfer except the acknowledge bit. When WAIT is set to 1, after the fall of the clock for the final data bit, low period is extended for two transfer clocks. If WAIT is cleared to 0, data and acknowledge bits are transferred consecutively with no wait inserted. The setting of this bit is invalid in slave mode with the I ² C bus format or with the clocked synchronous serial format.
5, 4	—	All 1	—	Reserved These bits are always read as 1.

15.4 Operation

The I²C bus interface can communicate either in I²C bus mode or clocked synchronous serial mode by setting FS in SAR.

15.4.1 I²C Bus Format

Figure 15.3 shows the I²C bus formats. Figure 15.4 shows the I²C bus timing. The first frame following a start condition always consists of 8 bits.

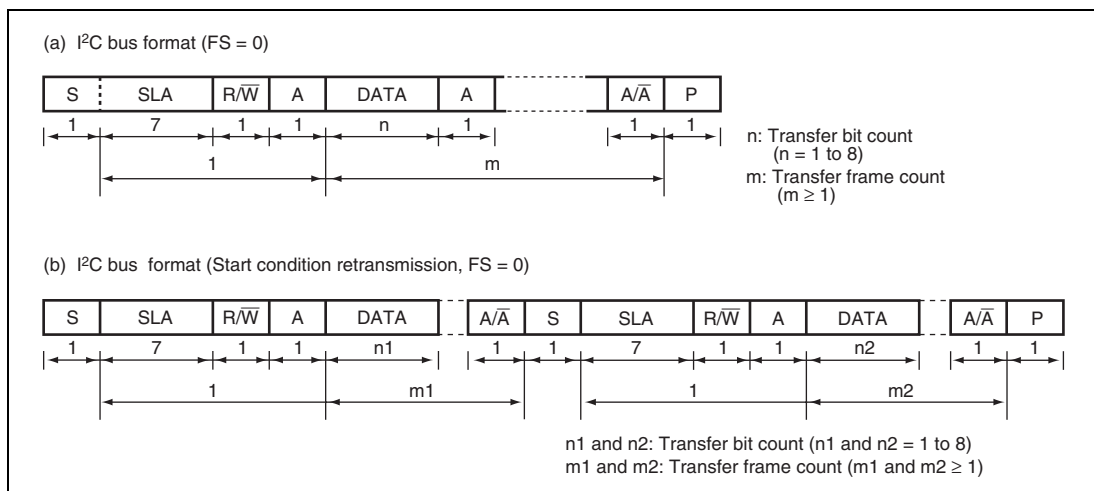


Figure 15.3 I²C Bus Formats

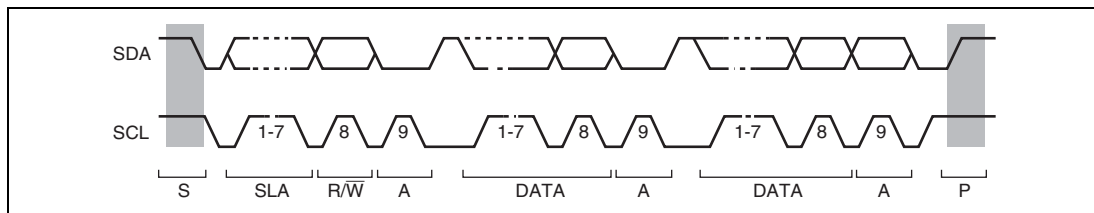


Figure 15.4 I²C Bus Timing

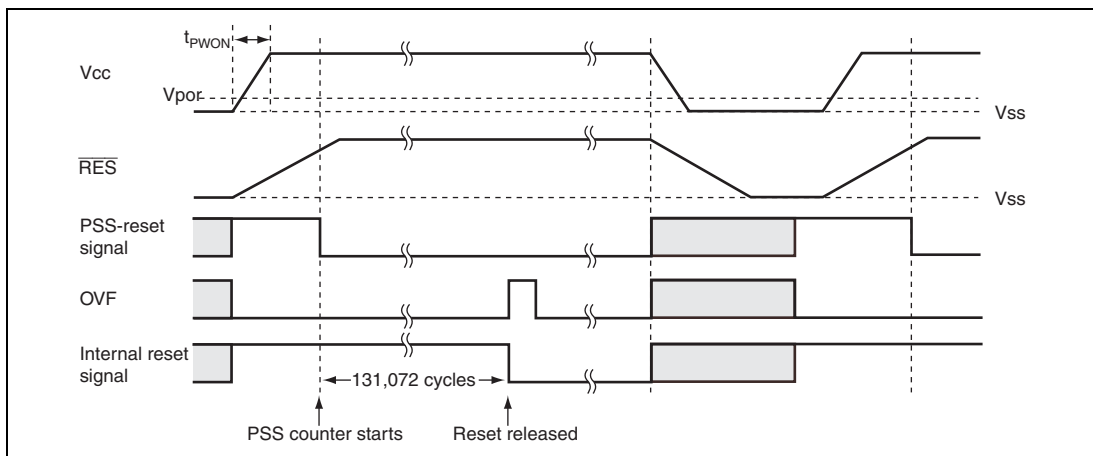


Figure 17.3 Operational Timing of Power-On Reset Circuit

17.3.2 Low-Voltage Detection Circuit

(1) LVDR (Reset by Low Voltage Detection) Circuit

Figure 17.4 shows the timing of the operation of the LVDR circuit. The LVDR circuit is enabled after a power-on reset is released. To cancel the LVDR circuit, first the LVDRE bit in LVDCR should be cleared to 0 and then the LVDE bit in LVDCR and, if necessary, the BGRE bit should be cleared to 0. The LVDE and the BGRE bits must not be cleared to 0 simultaneously with the LVDRE bit because incorrect operation may occur. To restart the LVDR circuit, set the LVDE bit and the BGRE bit to 1, wait for 50 μ s (t_{LVDRON}) given by a software timer until the reference voltage and the low-voltage-detection power supply have settled, then set the LVDRE bit to 1. After that, the output settings of ports must be made.

When the power-supply voltage falls below the V_{reset} voltage (2.3 V or 3.6 V (Typ.)), the LVDR circuit clears the \overline{LVDRES} signal to 0, and resets prescaler S. The low-voltage detection reset state remains in place until a power-on reset is generated. When the power-supply voltage rises above the V_{reset} voltage again, prescaler S starts counting. It counts 131,072 clock (ϕ) cycles, and then releases the internal reset signal. In this case, the LVDE, BGRE, VDDII, LVDSEL, and LVDRE bits in LVDCR are not initialized.

Note that if the power supply voltage (V_{cc}) falls below $V_{LVDRmin} = 1.0$ V and then rises from that point, the low-voltage detection reset may not occur.

If the power supply voltage (V_{cc}) falls below $V_{por} = 100$ mV, a power-on reset occurs.

(4) Operating Procedures for Enabling/Disabling LVDR and LVDI Circuits

The low-voltage detection circuit is enabled after reset. To enable or disable the low-voltage detection circuit correctly, follow the procedure described below. Figure 17.7 shows the timing for the operation and release of the low-voltage detection circuit.

1. To disable the low-voltage detection circuit, clear all of the LVDRE, LVDDE, and LVDUE bits to 0. Then, clear the LVDE and BGRE bits to 0. Set the VDDII bit in LVDCR if necessary. The LVDE and BGRE bits must not be cleared to 0 at the same timing as the LVDRE, LVDDE, and LVDUE bits because incorrect operation may occur.
2. To enable the low-voltage detection circuit, set the LVDE and BGRE bits in LVDCR to 1. When the voltages input on the ExtU and ExtD pins are used as the compared voltage, clear the LVDDII bit to 0.
3. Wait for $50\ \mu\text{s}$ (t_{LVON}) given by a software timer until the reference voltage and the low-voltage-detection power supply have settled. Then, clear the LVDDF and LVDUF bits in LVDSR to 0 and set the LVDRE, LVDDE, and LVDUE bits in LVDCR to 1, if necessary.

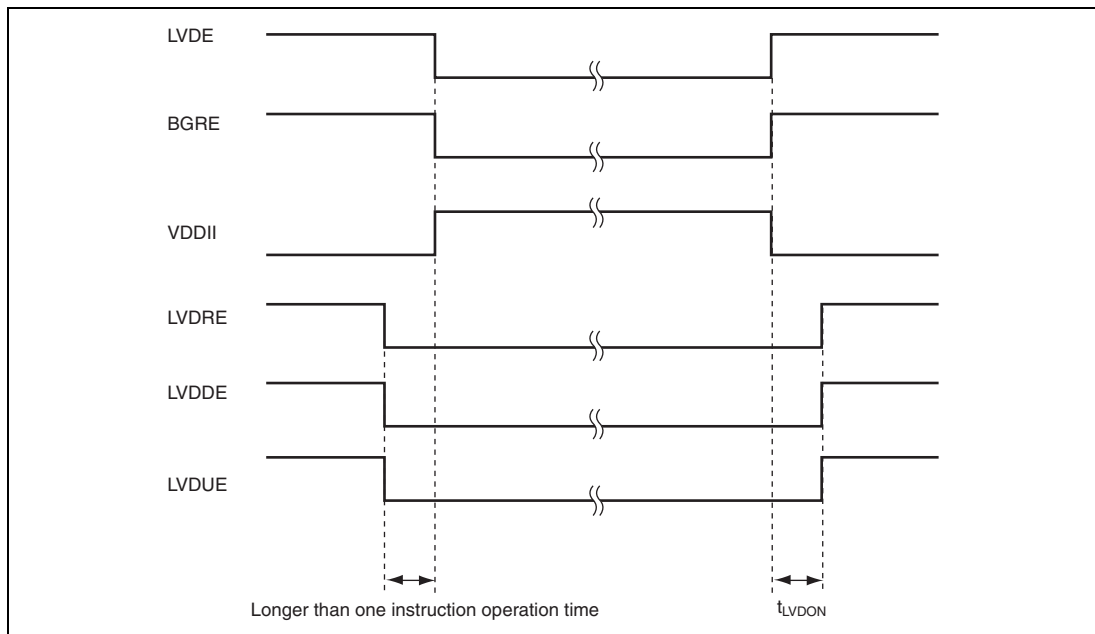


Figure 17.7 Timing for Enabling/Disabling of Low-Voltage Detection Circuit

Section 19 List of Registers

The register list gives information on the on-chip I/O register addresses, how the register bits are configured, and the register states in each operating mode. The information is given as shown below.

1. Register addresses (address order)
 - Registers are listed from the lower allocation addresses.
 - Registers are classified by functional modules.
 - The data bus width is indicated.
 - The number of access states is indicated.
2. Register bits
 - Bit configurations of the registers are described in the same order as the register addresses.
 - Reserved bits are indicated by — in the bit name column.
 - When registers consist of 16 bits, bits are described from the MSB side.
3. Register states in each operating mode
 - Register states are described in the same order as the register addresses.
 - The register states described here are for the basic operating modes. If there is a specific reset for an on-chip peripheral module, refer to the section on that on-chip peripheral module.

20.4 Operation Timing

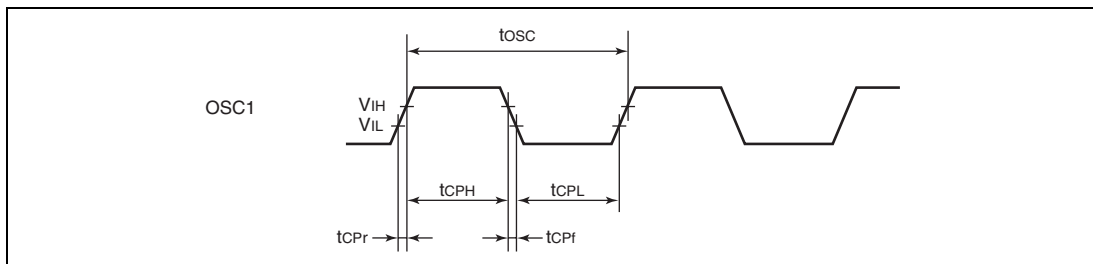


Figure 20.1 System Clock Input Timing

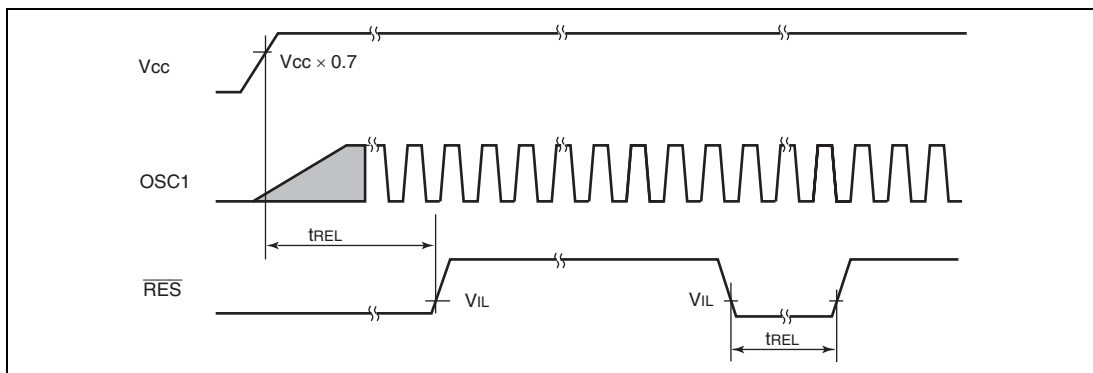


Figure 20.2 \overline{RES} Low Width Timing

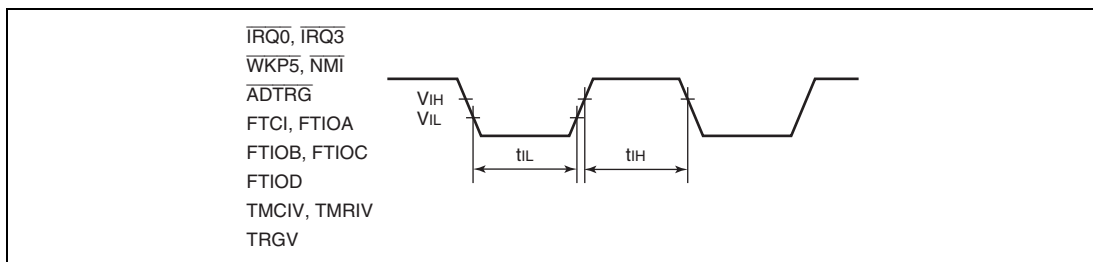


Figure 20.3 Input Timing

Instruction Mnemonic		Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
SUBX	SUBX #xx:8, Rd	1					
	SUBX. Rs, Rd	1					
TRAPA	TRAPA #xx:2	2	1	2			4
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
	XOR.W #xx:16, Rd	2					
	XOR.W Rs, Rd	1					
	XOR.L #xx:32, ERd	3					
	XOR.L ERs, ERd	2					
XORC	XORC #xx:8, CCR	1					

Notes: 1. n: Specified value in R4L and R4. The source and destination operands are accessed n+1 times respectively.
 2. Cannot be used in this LSI.

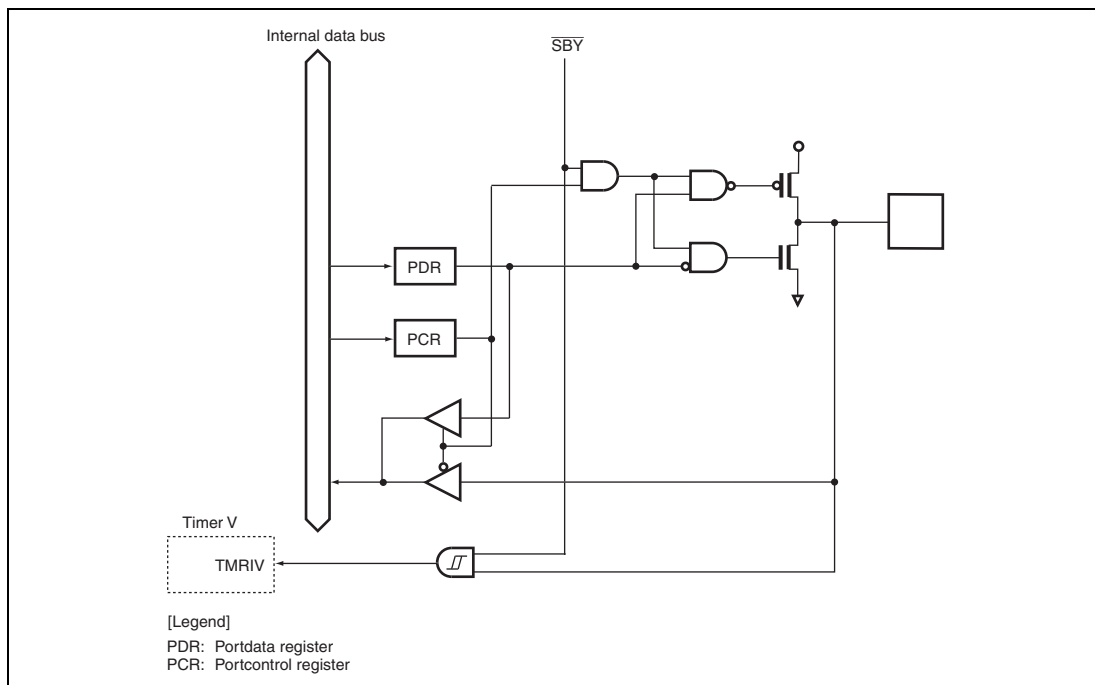


Figure B.10 Port 7 Block Diagram (P74)

