



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

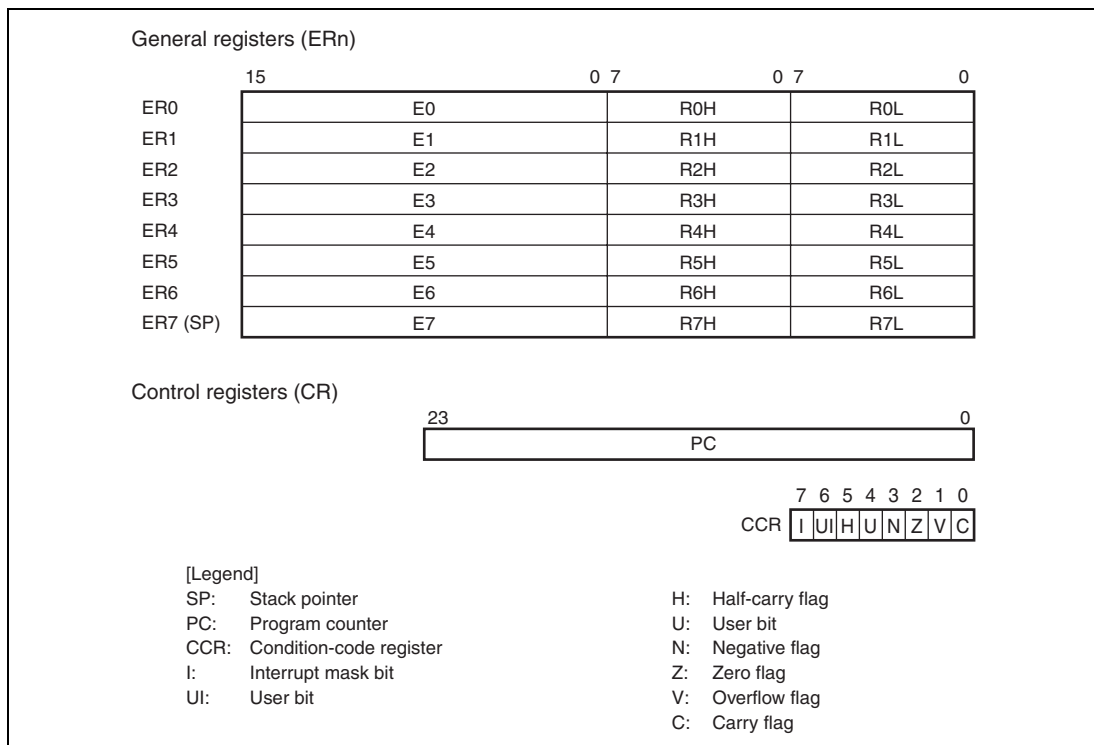
#### Details

Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	12MHz
Connectivity	I <sup>2</sup> C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/df36912gfhv">https://www.e-xfl.com/product-detail/renesas-electronics-america/df36912gfhv</a>



## 2.2 Register Configuration

The H8/300H CPU has the internal registers shown in figure 2.2. There are two types of registers; general registers and control registers. The control registers are a 24-bit program counter (PC), and an 8-bit condition code register (CCR).



**Figure 2.2 CPU Registers**

**Table 2.6 Bit Manipulation Instructions (1)**

<b>Instruction</b>	<b>Size*</b>	<b>Function</b>
BSET	B	$1 \rightarrow \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle$ Sets a specified bit in a general register or memory operand to 1. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BCLR	B	$0 \rightarrow \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle$ Clears a specified bit in a general register or memory operand to 0. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BNOT	B	$\neg \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle \rightarrow \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle$ Inverts a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BTST	B	$\neg \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle \rightarrow Z$ Tests a specified bit in a general register or memory operand and sets or clears the Z flag accordingly. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BAND	B	$C \wedge \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle \rightarrow C$ ANDs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIAND	B	$C \wedge \neg \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle \rightarrow C$ ANDs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BOR	B	$C \vee \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle \rightarrow C$ ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIOR	B	$C \vee \neg \langle \text{bit-No.} \rangle \text{ of } \langle \text{EAd} \rangle \rightarrow C$ ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.

Note: \* Refers to the operand size.

B: Byte

**Table 2.9 Block Data Transfer Instructions**

<b>Instruction</b>	<b>Size</b>	<b>Function</b>
EEPMOV.B	—	if R4L $\neq$ 0 then Repeat @ER5+ $\rightarrow$ @ER6+, R4L-1 $\rightarrow$ R4L Until R4L = 0 else next;
EEPMOV.W	—	if R4 $\neq$ 0 then Repeat @ER5+ $\rightarrow$ @ER6+, R4-1 $\rightarrow$ R4 Until R4 = 0 else next;  Transfers a data block. Starting from the address set in ER5, transfers data for the number of bytes set in R4L or R4 to the address location set in ER6.  Execution of the next instruction begins as soon as the transfer is completed.

## 2.4.2 Basic Instruction Formats

H8/300H CPU instructions consist of 2-byte (1-word) units. An instruction consists of an operation field (op field), a register field (r field), an effective address extension (EA field), and a condition field (cc).

Figure 2.7 shows examples of instruction formats.

### (1) Operation Field

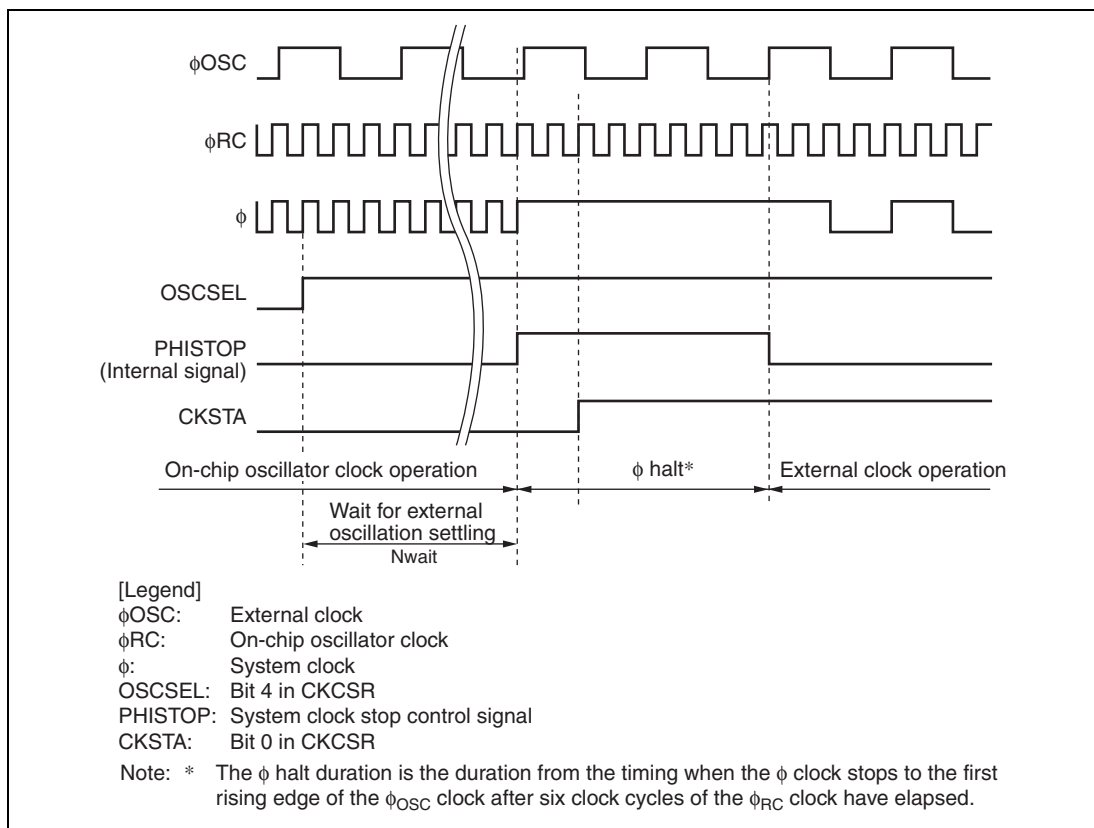
Indicates the function of the instruction, the addressing mode, and the operation to be carried out on the operand. The operation field always includes the first four bits of the instruction. Some instructions have two operation fields.

### (2) Register Field

Specifies a general register. Address registers are specified by 3 bits, and data registers by 3 bits or 4 bits. Some instructions have two register fields. Some have no register field.

### 5.3.2 Clock Change Timing

The timing for changing clocks are shown in figures 5.5 and 5.6.



**Figure 5.5 Timing Chart of Switching On-chip Oscillator Clock to External Clock**

## 7.2 Register Descriptions

The flash memory has the following registers.

- Flash memory control register 1 (FLMCR1)
- Flash memory control register 2 (FLMCR2)
- Erase block register 1 (EBR1)
- Flash memory enable register (FENR)

### 7.2.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is a register that makes the flash memory change to program mode, program-verify mode, erase mode, or erase-verify mode. For details on register setting, refer to section 7.4, Flash Memory Programming/Erasing.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	SWE	0	R/W	Software Write Enable When this bit is set to 1, flash memory programming/erasing is enabled. When this bit is cleared to 0, other FLMCR1 register bits and all EBR1 bits cannot be set.
5	ESU	0	R/W	Erase Setup When this bit is set to 1, the flash memory changes to the erase setup state. When it is cleared to 0, the erase setup state is cancelled. Set this bit to 1 before setting the E bit to 1 in FLMCR1.
4	PSU	0	R/W	Program Setup When this bit is set to 1, the flash memory changes to the program setup state. When it is cleared to 0, the program setup state is cancelled. Set this bit to 1 before setting the P bit in FLMCR1.
3	EV	0	R/W	Erase-Verify When this bit is set to 1, the flash memory changes to erase-verify mode. When it is cleared to 0, erase-verify mode is cancelled.

3. When the boot program is initiated, the chip measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. The chip then calculates the bit rate of transmission from the host, and adjusts the SCI3 bit rate to match that of the host. The reset should end with the RxD pin high. The RxD and TxD pins should be pulled up on the board if necessary. After the reset is complete, it takes approximately 100 states before the chip is ready to measure the low-level period.
4. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate the completion of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and the chip. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 7.3.
5. In boot mode, a part of the on-chip RAM area is used by the boot program. The area H'F980 to H'FEF is the area to which the programming control program is transferred from the host. The boot program area cannot be used until the execution state in boot mode switches to the programming control program.
6. Before branching to the programming control program, the chip terminates transfer operations by SCI3 (by clearing the RE and TE bits in SCR3 to 0), however the adjusted bit rate value remains set in BRR. Therefore, the programming control program can still use it for transfer of write data or verify data with the host. The TxD pin is high (PCR22 = 1, P22 = 1). The contents of the CPU general registers are undefined immediately after branching to the programming control program. These registers must be initialized at the beginning of the programming control program, as the stack pointer (SP), in particular, is used implicitly in subroutine calls, etc.
7. Boot mode can be cleared by a reset. End the reset after driving the reset pin low, waiting at least 20 states, and then setting the TEST pin and  $\overline{\text{NMI}}$  pin. Boot mode is also cleared when a WDT overflow occurs.
8. Do not change the TEST pin and  $\overline{\text{NMI}}$  pin input levels in boot mode.



### 9.7.3 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- PC1/OSC2/CLKOUT pin

Register		CKCSR		PCRC	Pin Function
Bit Name	PMRC1	PMRC0	PCRC1		
Setting value	0	X	0	PC1 input pin	
			1	PC1 output pin	
	1	0	X	CLKOUT output pin	
		1	X	OSC2 oscillation pin	

[Legend]

X: Don't care

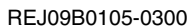
- PC0/OSC1 pin

Register		CKCSR	PCRC	Pin Function
Bit Name	PMRC0	PCRC0		
Setting value	0	0		PC0 input pin
		1		PC0 output pin
	1	X		OSC1 oscillation pin

[Legend]

X: Don't care





## 12.2 Input/Output Pins

Table 12.2 summarizes the timer W pins.

**Table 12.2 Pin Configuration**

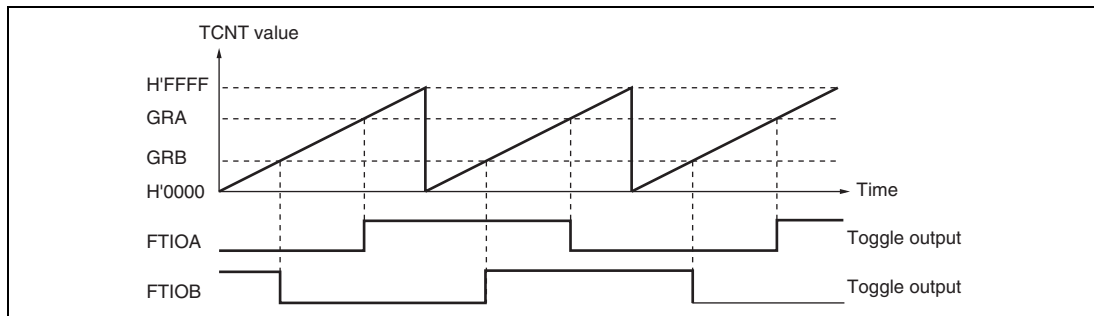
Name	Abbreviation	Input/Output	Function
External clock input	FTCI	Input	External clock input pin
Input capture/output compare A	FTIOA	Input/output	Output pin for GRA output compare or input pin for GRA input capture
Input capture/output compare B	FTIOB	Input/output	Output pin for GRB output compare, input pin for GRB input capture, or PWM output pin in PWM mode
Input capture/output compare C	FTIOC	Input/output	Output pin for GRC output compare, input pin for GRC input capture, or PWM output pin in PWM mode
Input capture/output compare D	FTIOD	Input/output	Output pin for GRD output compare, input pin for GRD input capture, or PWM output pin in PWM mode

## 12.3 Register Descriptions

The timer W has the following registers.

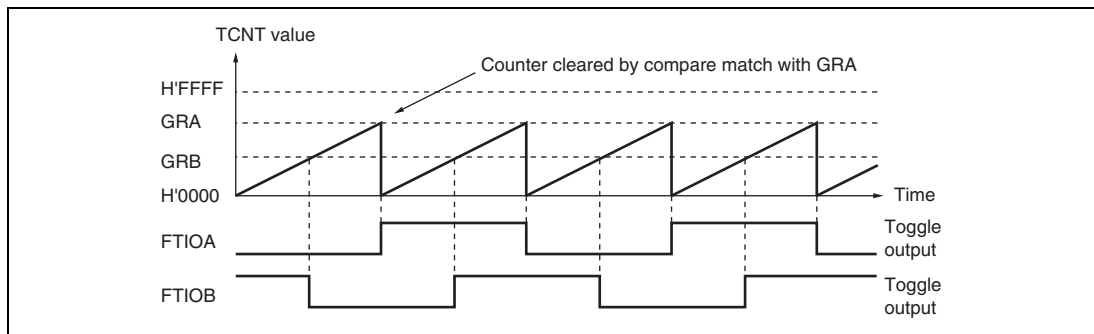
- Timer mode register W (TMRW)
- Timer control register W (TCRW)
- Timer interrupt enable register W (TIERW)
- Timer status register W (TSRW)
- Timer I/O control register 0 (TIOR0)
- Timer I/O control register 1 (TIOR1)
- Timer counter (TCNT)
- General register A (GRA)
- General register B (GRB)
- General register C (GRC)
- General register D (GRD)

Figure 12.5 shows an example of toggle output when TCNT operates as a free-running counter, and toggle output is selected for both compare match A and B.

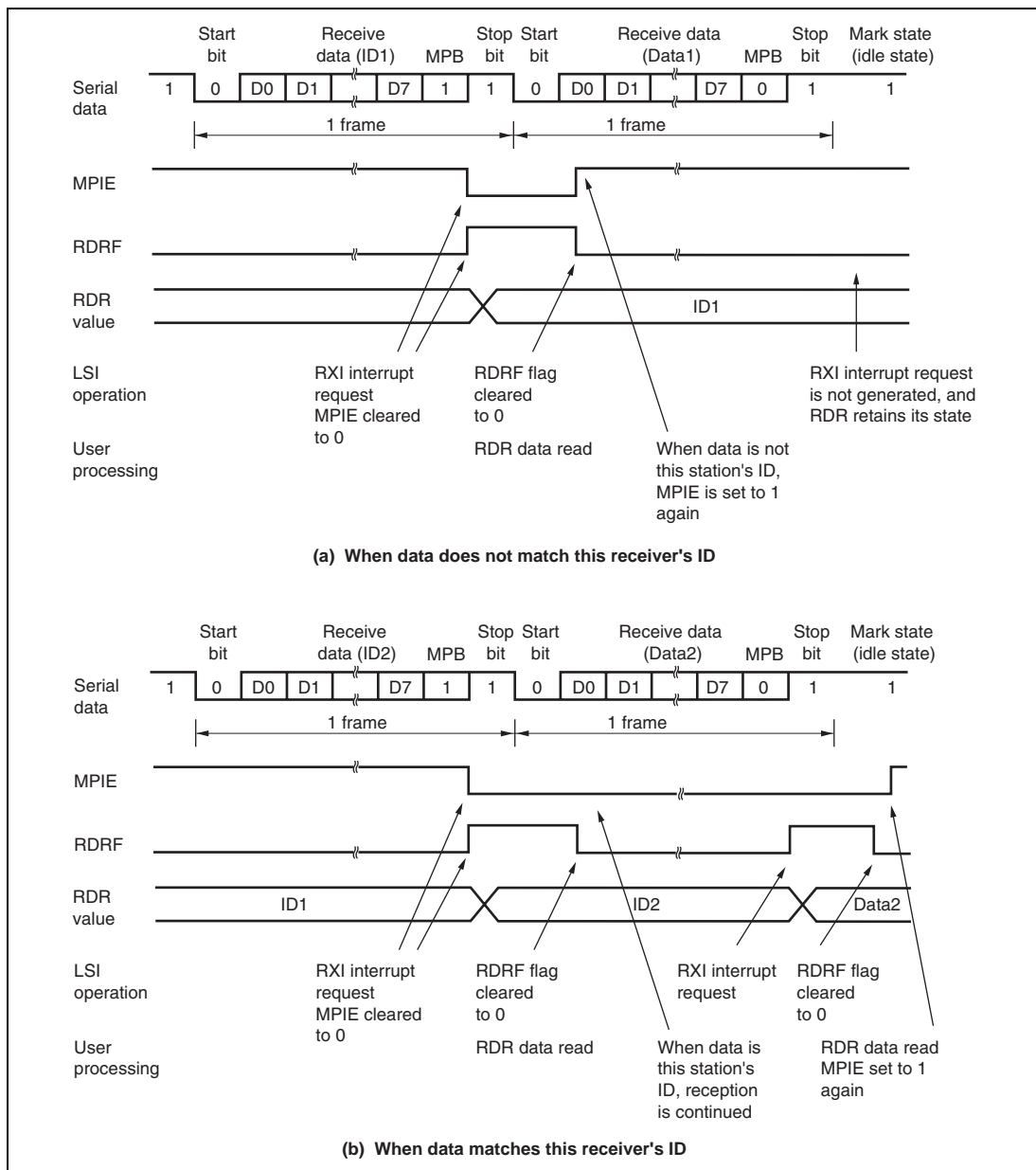


**Figure 12.5 Toggle Output Example (TOA = 0, TOB = 1)**

Figure 12.6 shows another example of toggle output when TCNT operates as a periodic counter, cleared by compare match A. Toggle output is selected for both compare match A and B.



**Figure 12.6 Toggle Output Example (TOA = 0, TOB = 1)**



**Figure 14.19 Example of SCI3 Reception Using Multiprocessor Format  
(Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)**

### 15.3.7 I<sup>2</sup>C Bus Transmit Data Register (ICDRT)

ICDRT is an 8-bit readable/writable register that stores the transmit data. When ICDRT detects the space in the shift register (ICDRS), it transfers the transmit data which is written in ICDRT to ICDRS and starts transferring data. If the next transfer data is written to ICDRT during transferring data of ICDRS, continuous transfer is possible. If the MLS bit of ICMR is set to 1 and when the data is written to ICDRT, the MSB/LSB inverted data is read. The initial value of ICDRT is H'FF.

### 15.3.8 I<sup>2</sup>C Bus Receive Data Register (ICDRR)

ICDRR is an 8-bit register that stores the receive data. When data of one byte is received, ICDRR transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, therefore the CPU cannot write to this register. The initial value of ICDRR is H'FF.

### 15.3.9 I<sup>2</sup>C Bus Shift Register (ICDRS)

ICDRS is a register that is used to transfer/receive data. In transmission, data is transferred from ICDRT to ICDRS and the data is sent from the SDA pin. In reception, data is transferred from ICDRS to ICDRR after data of one byte is received. This register cannot be read directly from the CPU.

## [Legend]

- S: Start condition. The master device drives SDA from high to low while SCL is high.
- SLA: Slave address
- R/W: Indicates the direction of data transfer: from the slave device to the master device when R/W is 1, or from the master device to the slave device when R/W is 0.
- A: Acknowledge. The receive device drives SDA to low.
- DATA: Transfer data
- P: Stop condition. The master device drives SDA from low to high while SCL is high.

### 15.4.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal. For master transmit mode operation timing, refer to figures 15.5 and 15.6. The transmission procedure and operations in master transmit mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MLS and WAIT bits in ICMR and the CKS3 to CKS0 bits in ICCR1 to 1. (Initial setting)
2. Read the BBSY flag in ICCR2 to confirm that the bus is free. Set the MST and TRS bits in ICCR1 to select master transmit mode. Then, write 1 to BBSY and 0 to SCP using MOV instruction. (Start condition issued) This generates the start condition.
3. After confirming that TDRE in ICSR has been set, write the transmit data (the first byte data show the slave address and  $R/\overline{W}$ ) to ICDRT. At this time, TDRE is automatically cleared to 0, and data is transferred from ICDRT to ICDRS. TDRE is set again.
4. When transmission of one byte data is completed while TDRE is 1, TEND in ICSR is set to 1 at the rise of the 9th transmit clock pulse. Read the ACKBR bit in ICIER, and confirm that the slave device has been selected. Then, write second byte data to ICDRT. When ACKBR is 1, the slave device has not been acknowledged, so issue the stop condition. To issue the stop condition, write 0 to BBSY and SCP using MOV instruction. SCL is fixed low until the transmit data is prepared or the stop condition is issued.
5. The transmit data after the second byte is written to ICDRT every time TDRE is set.
6. Write the number of bytes to be transmitted to ICDRT. Wait until TEND is set (the end of last byte data transmission) while TDRE is 1, or wait for NACK (NACKF in ICSR = 1) from the receive device while ACKF in ICIER is 1. Then, issue the stop condition to clear TEND or NACKF.
7. When the STOP bit in ICSR is set to 1, the operation returns to the slave receive mode.



## Section 17 Band-Gap Circuit, Power-On Reset, and Low-Voltage Detection Circuits

This LSI can include a band-gap circuit (BGR, band-gap regulator), a power-on reset circuit and low-voltage detection circuit.

BGR supplies a reference voltage to the on-chip oscillator and low-voltage detection circuit. Figure 17.1 shows the block diagram of how BGR is allocated.

The low-voltage detection (LVD) circuit consists of two circuits: LVDI (interrupt by low voltage detection) and LVDR (reset by low voltage detection) circuits.

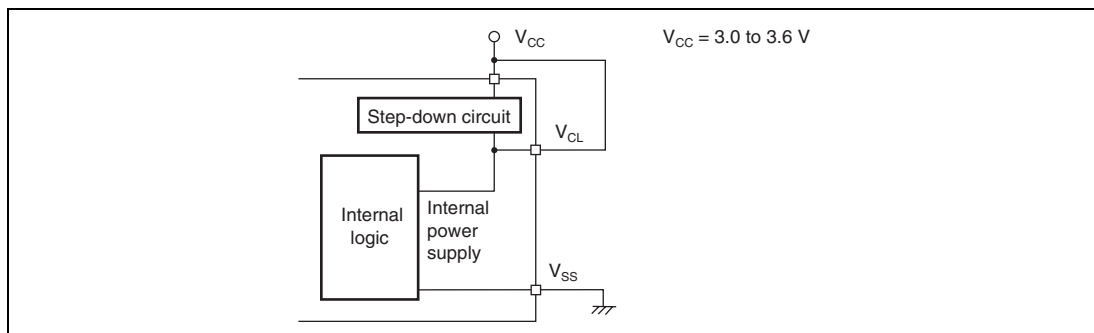
This circuit is used to prevent abnormal operation (program runaway) from occurring due to the power supply voltage fall and to recreate the state before the power supply voltage fall when the power supply voltage rises again.

Even if the power supply voltage falls, the unstable state when the power supply voltage falls below the guaranteed operating voltage can be removed by entering standby mode when exceeding the guaranteed operating voltage and during normal operation. Thus, system stability can be improved. If the power supply voltage falls more, the reset state is automatically entered. If the power supply voltage rises again, the reset state is held for a specified period, then active mode is automatically entered.

Figure 17.2 is a block diagram of the power-on reset circuit and the low-voltage detection circuit.

## 18.2 When Not Using Internal Power Supply Step-Down Circuit

When the internal power supply step-down circuit is not used, connect the external power supply to the  $V_{CL}$  pin and  $V_{CC}$  pin, as shown in figure 18.2. The external power supply is then input directly to the internal power supply. The permissible range for the power supply voltage is 3.0 V to 3.6 V. Operation cannot be guaranteed if a voltage outside this range (less than 3.0 V or more than 3.6 V) is input.



**Figure 18.2 Power Supply Connection when Internal Step-Down Circuit is Not Used**

## 20.2.6 Power-Supply-Voltage Detection Circuit Characteristics

**Table 20.8 Power-Supply-Voltage Detection Circuit Characteristics**

$V_{SS} = 0.0 \text{ V}$ ,  $T_a = -20 \text{ to } +75^\circ\text{C}$ , unless otherwise indicated.

Item	Symbol	Test Condition	Values			Unit
			Min.	Typ.	Max.	
Power-supply falling detection voltage	Vint(D)	LVDSEL = 0	3.3	3.7	4.3	V
Power-supply rising detection voltage	Vint(U)	LVDSEL = 0	3.6	4.0	4.5	V
Reset detection voltage 1* <sup>1</sup>	Vreset1	LVDSEL = 0	2.0	2.3	2.7	V
Reset detection voltage 2* <sup>2</sup>	Vreset2	LVDSEL = 1	3.0	3.6	4.2	V
Lower-limit voltage of LVDR operation* <sup>3</sup>	$V_{LVDRmin}$		1.0	—	—	V
LVD stabilization time	$t_{LVDRON}$		50	—	—	$\mu\text{s}$
Current consumption in standby mode	$I_{STBY}$	LVDE = 1, BGRE = 1 Vcc = 5.0 V	—	—	350	$\mu\text{A}$

- Notes: 1. This voltage should be used when the falling and rising voltage detection function is used.
2. Select the low-voltage reset 2 when only the low-voltage detection reset is used.
3. When the power-supply voltage (Vcc) falls below  $V_{LVDRmin} = 1.0 \text{ V}$  and then rises, a reset may not occur. Therefore sufficient evaluation is required.

## 20.2.7 LVDI External Voltage Detection Circuit Characteristics

**Table 20.9 LVDI External Voltage Detection Circuit Characteristics**

$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$ ,  $AV_{CC} = 3.0 \text{ to } 5.5 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_a = -20 \text{ to } +75^\circ\text{C}$

Item	Symbol	Test Condition	Values			Unit
			Min.	Typ.	Max.	
ExtD/ExtU input detection voltage	Vexd		0.85	1.15	1.45	V
ExtD/ExtU input voltage range	VextD/U	VextD > VextU	-0.3	—	Lower voltage, either $AV_{CC} + 0.3$ or $V_{CC} + 0.3$	V

Instruction	Mnemonic	Instruction	Branch	Stack	Byte Data	Word Data	Internal
		Fetch	Addr. Read	Operation	Access	Access	Operation
		I	J	K	L	M	N
MULXS	MULXS.B Rs, Rd	2					12
	MULXS.W Rs, ERd	2					20
MULXU	MULXU.B Rs, Rd	1					12
	MULXU.W Rs, ERd	1					20
NEG	NEG.B Rd	1					
	NEG.W Rd	1					
	NEG.L ERd	1					
NOP	NOP	1					
NOT	NOT.B Rd	1					
	NOT.W Rd	1					
	NOT.L ERd	1					
OR	OR.B #xx:8, Rd	1					
	OR.B Rs, Rd	1					
	OR.W #xx:16, Rd	2					
	OR.W Rs, Rd	1					
	OR.L #xx:32, ERd	3					
	OR.L ERs, ERd	2					
ORC	ORC #xx:8, CCR	1					
POP	POP.W Rn	1				1	2
	POP.L ERn	2				2	2
PUSH	PUSH.W Rn	1				1	2
	PUSH.L ERn	2				2	2
ROTL	ROTL.B Rd	1					
	ROTL.W Rd	1					
	ROTL.L ERd	1					
ROTR	ROTR.B Rd	1					
	ROTR.W Rd	1					
	ROTR.L ERd	1					
ROTXL	ROTXL.B Rd	1					
	ROTXL.W Rd	1					
	ROTXL.L ERd	1					



**Figure B.6 (1) Port 5 Block Diagram (P57, P56) (for H8/36912 Group)**