STMicroelectronics - STM32F777BIT6 Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	159
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f777bit6

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions

Pin Number										Pin name (function after reset	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F777xx						STM32F778Ax STM32F779xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
1	1	A2	1	1	A3	E10	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	A1	2	2	A2	F10	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-

Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F777xx						STM32F778Ax STM32F779xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180(1)	LQFP176	LQFP208	TFBGA216						
-	-	-	-	60	L6	-	-	60	L6	VSS	S	-	-	-	-
34	46	R5	56	61	R5	P10	56	61	R5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC1_IN8, ADC2_IN8
35	47	R4	57	62	R4	J8	57	62	R4	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC1_IN9, ADC2_IN9
36	48	M6	58	63	M5	J7	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, DFSDM1_CKIN1, EVENTOUT	-
-	-	-	-	64	G4	NC	-	64	G4	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	65	R6	NC	-	65	R6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	66	R7	NC	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	67	P7	NC	-	67	P7	PJ2	I/O	FT	-	DSI_TE, LCD_R3, EVENTOUT	-
-	-	-	-	68	N8	NC	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	69	M9	NC	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	R6	59	70	P8	N9	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	P6	60	71	M6	K7	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-

Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F777xx						STM32F778Ax STM32F779xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180(1)	LQFP176	LQFP208	TFBGA216						
71	104	B15	123	146	B15	D1	127	146	B15	PA12	I/O	FT	-	TIM1_ETR, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	105	A15	124	147	A15	D2	128	147	A15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	106	F13	125	148	E11	C1	129	148	E11	VCAP_2	S	-	-	-	-
74	107	F12	126	149	F10	C2	130	149	F10	VSS	S	-	-	-	-
75	108	G13	127	150	F11	B2	131	150	F11	VDD	S	-	-	-	-
-	-	E12	128	151	E12	F6	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	E13	129	152	E13	F7	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	D13	130	153	D13	E5	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	E14	131	154	E14	E4	132	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	D14	132	155	D14	B3	133	155	D14	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	C14	133	156	C14	C3	-	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-

1. Applicable only for STM32F7x9 sales types.
2. All main power (V_{DD}, V_{DDA}, $V_{DDSDMMC}$, V_{DDUSB}, V_{DDDSI}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
3. V_{IN} maximum value must always be respected. Refer to *Table 15* for the values of the maximum allowed injected current.
4. Include V_{REF-} pin.

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	420	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	−420	
ΣI_{VDDUSB}	Total current into V_{DDUSB} power line (source)	25	
$\Sigma I_{VDDSDMMC}$	Total current into $V_{DDSDMMC}$ power line (source)	60	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
$I_{VDDSDMMC}$	Maximum current into $V_{DDSDMMC}$ power line (source): PG[12:9], PD[7:6]	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	−100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/Os and control pin	−25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins (2)	120	
	Total output current sunk by sum of all USB I/Os	25	
	Total output current sunk by sum of all SDMMC I/Os	120	
	Total output current sourced by sum of all I/Os and control pins except USB I/Os(2)	−120	
$I_{INJ(PIN)}$	Injected current on FT, FTf, RST and B pins (3)	−5/+0	
	Injected current on TTa pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 14: Voltage characteristics* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	– 65 to +150	°C
T_J	Maximum junction temperature	125	

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 108 MHz)	TIM1	24.1	23.8	19.6	µA/MHz
	TIM8	24.5	24.2	20.0	
	USART1	17.7	17.4	14.3	
	USART6	11.9	11.8	9.4	
	ADC1(5)	4.5	4.7	3.5	
	ADC2(5)	4.5	4.7	3.3	
	ADC3(5)	4.5	4.6	3.3	
	SDMMC1	8.4	8.3	6.9	
	SDMMC2	8.2	8.2	6.4	
	SPI1/I2S1(3)	3.9	3.6	3.1	
	SPI4	3.9	3.6	3.1	
	SYSCFG	2.5	2.2	1.9	
	TIM9	8.0	8.0	6.2	
	TIM10	5.0	5.1	3.7	
	TIM11	6.9	6.9	5.3	
	SPI5	2.7	2.8	1.8	
	SPI6	3.1	3.2	2.2	
	SAI1	3.2	3.3	2.2	
	DFSDM1	10.9	10.7	9.0	
	SAI2	3.9	3.9	2.8	
	MDIO	7.1	7.0	5.8	
	LTDC	51.2	50.3	41.8	
	DSI	8.5	8.4	8.1	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.75 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 56. Flash memory programming (single bank configuration nDBANK=1) (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

Table 57. Flash memory programming (dual bank configuration nDBANK=0)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	250	600	
		Program/erase parallelism (PSIZE) = x 32	-	200	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1100	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	800	1400	
		Program/erase parallelism (PSIZE) = x 32	-	500	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2.1	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.5	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	

Table 71. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.18.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 71*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 72. ADC static accuracy at f_{ADC} = 18 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Guaranteed by characterization results.

Table 73. ADC static accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, $V_{DDA} - V_{REF} < 1.2$ V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Guaranteed by characterization results.

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.
- The 20mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load Cload supported in Fm+, which is given by these formulas:

  $Tr(SDA/SCL)=0.8473xR_pxC_{load}$

  $R_p(min)= (VDD-V_{OL}(max))/I_{OL}(max)$

Where Rp is the I2C lines pull-up. Refer to Section 5.3.20: I/O port characteristics for the I2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to *Table 84* for the analog filter characteristics:

Table 84. I2C analog filter characteristics(1)

Symbol	**Parameter**	**Min**	**Max**	**Unit**
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	70(3)	ns

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

Figure 56. ULPI timing diagram

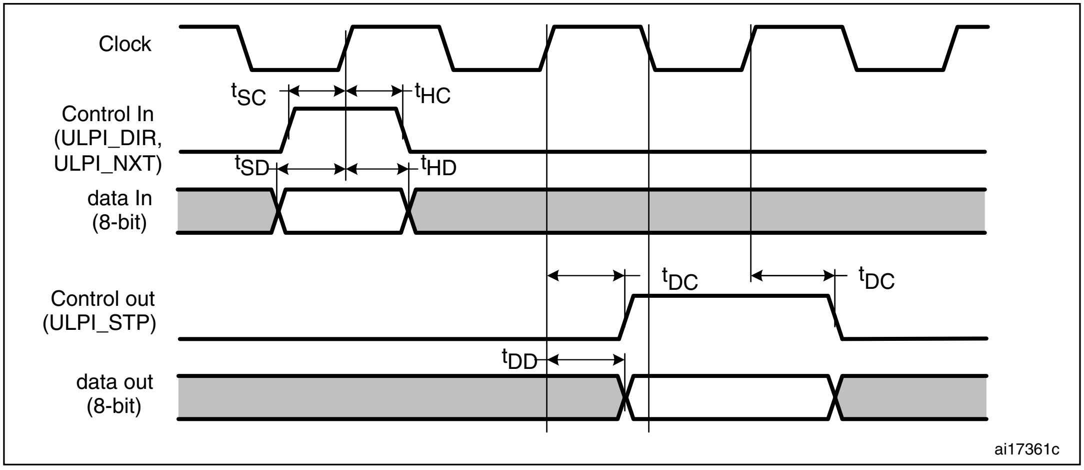


Table 95. Dynamic characteristics: USB ULPI(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	2	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	1.5	-	-	
t_{SD}	Data in setup time	-	2	-	-	
t_{HD}	Data in hold time	-	1	-	-	
t_{DC}/t_{DD}	Data/control output delay	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$, $C_L = 20\text{ pF}$	-	6.5	8	
		-	-	6.5	11	
		$1.7\text{ V} < V_{DD} < 3.6\text{ V}$, $C_L = 15\text{ pF}$	-			

1. Guaranteed by characterization results.

Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 96*, *Table 97* and *Table 98* for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output characteristics.

Table 96 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 57* shows the corresponding timing diagram.

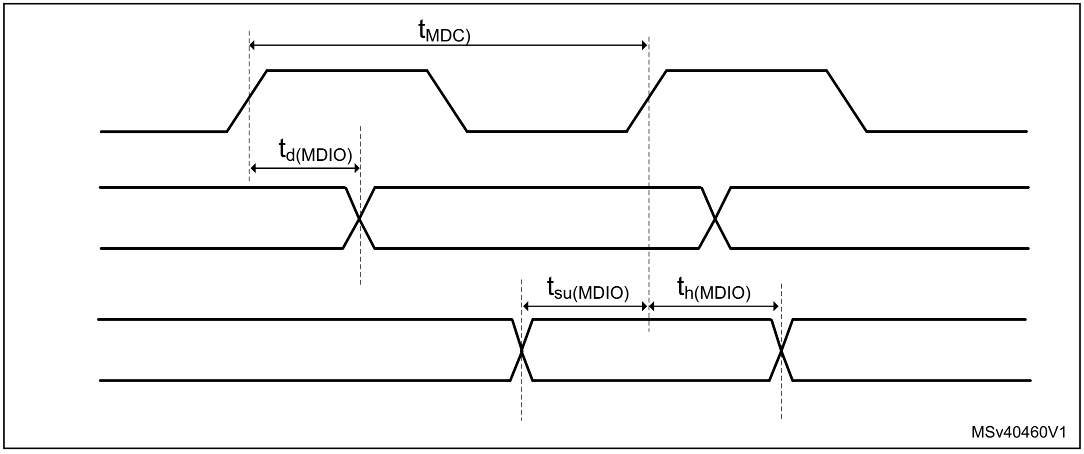
1. Guaranteed by characterization results.

Table 99. MDIO Slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{sDC}	Management Data clock	-	-	40	MHz
$t_{d(MDIO)}$	Management Data input/output **output valid time**	7	8	20	ns
$t_{su(MDIO)}$	Management Data input/output **setup time**	4	-	-	
$t_{h(MDIO)}$	Management Data input/output **hold time**	1	-	-	

The MDIO controller is mapped on APB2 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{PCLK2} \geq 1.5 * F_{MDC}$

Figure 60. MDIO Slave timing diagram



CAN (controller area network) interface

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

5.3.30 FMC characteristics

Unless otherwise specified, the parameters given in *Table 100* to *Table 113* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

1. Guaranteed by characterization results.

Table 107. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK} - 1$	$9T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK} - 0.5$	$7T_{HCLK} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} + 2$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} - 1$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

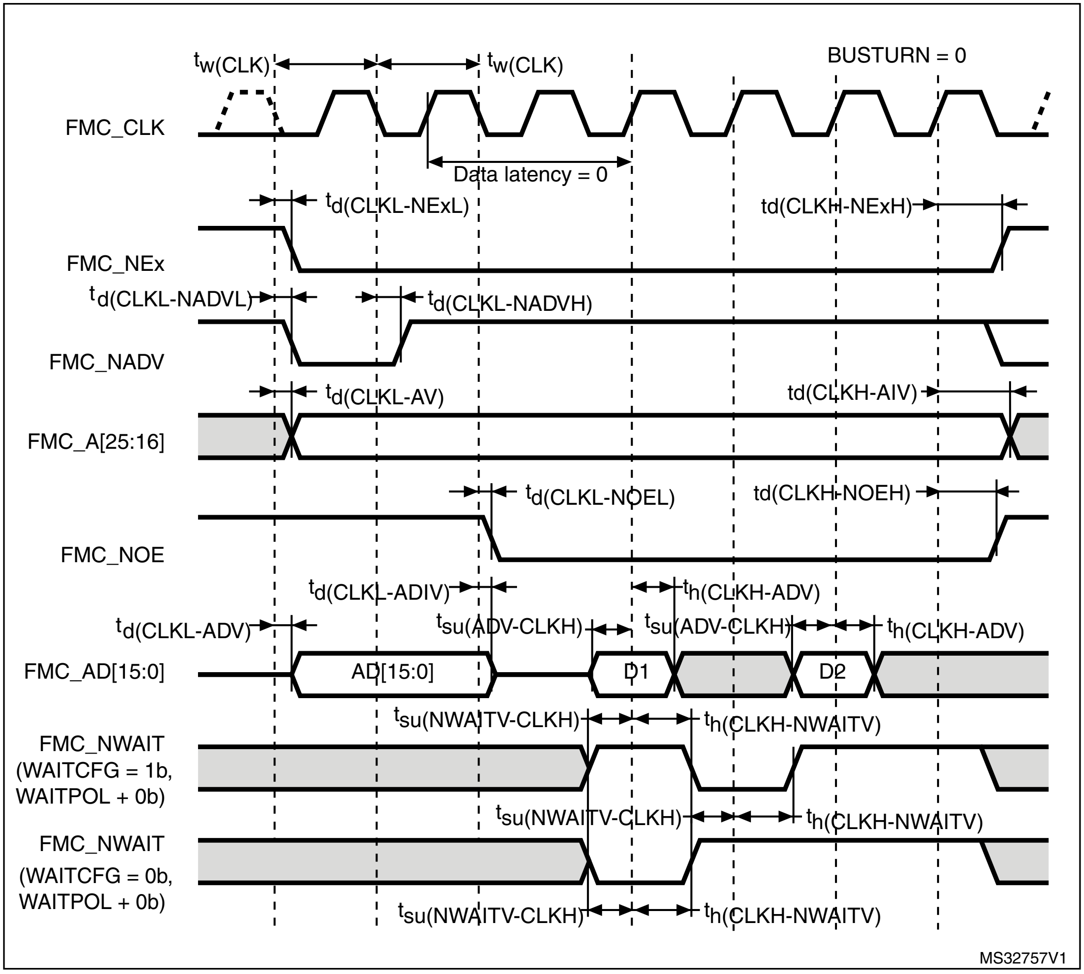
Figure 65 through *Figure 68* represent synchronous waveforms and *Table 108* through *Table 111* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all the timing tables, the T_{HCLK} is the HCLK clock period.

- For 2.7 V≤ V_{DD}≤ 3.6 V, maximum FMC_CLK = 100 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
- For 1.71 V≤ V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Figure 65. Synchronous multiplexed NOR/PSRAM read timings



1. Guaranteed by characterization results.

Figure 68. Synchronous non-multiplexed PSRAM write timings

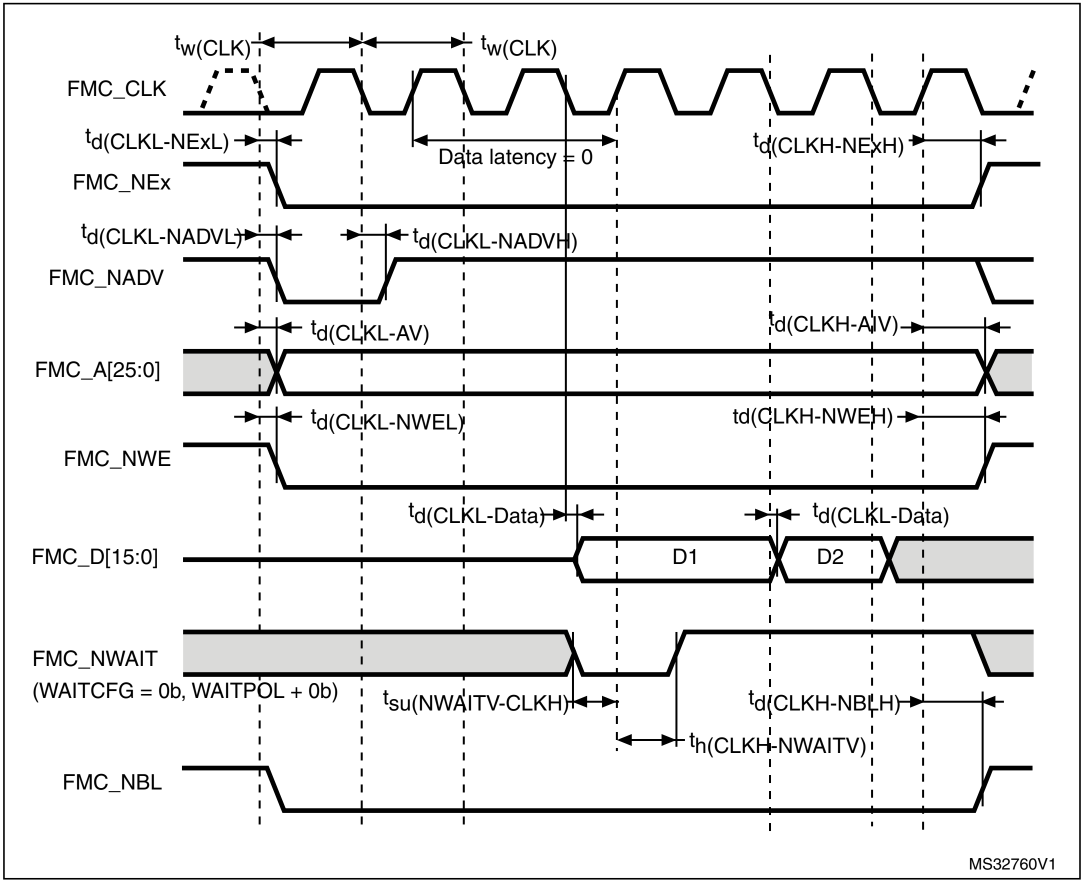


Figure 69. NAND controller waveforms for read access

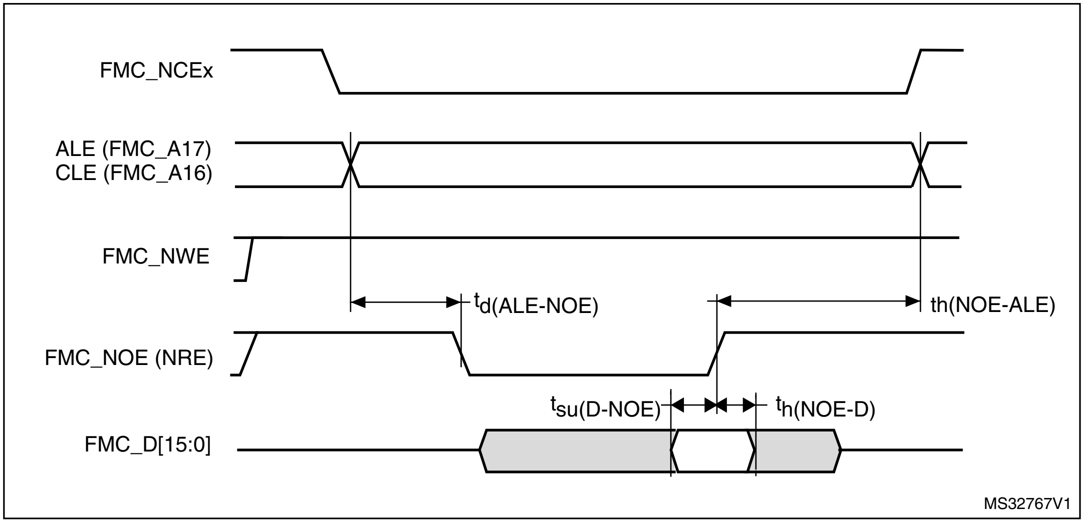
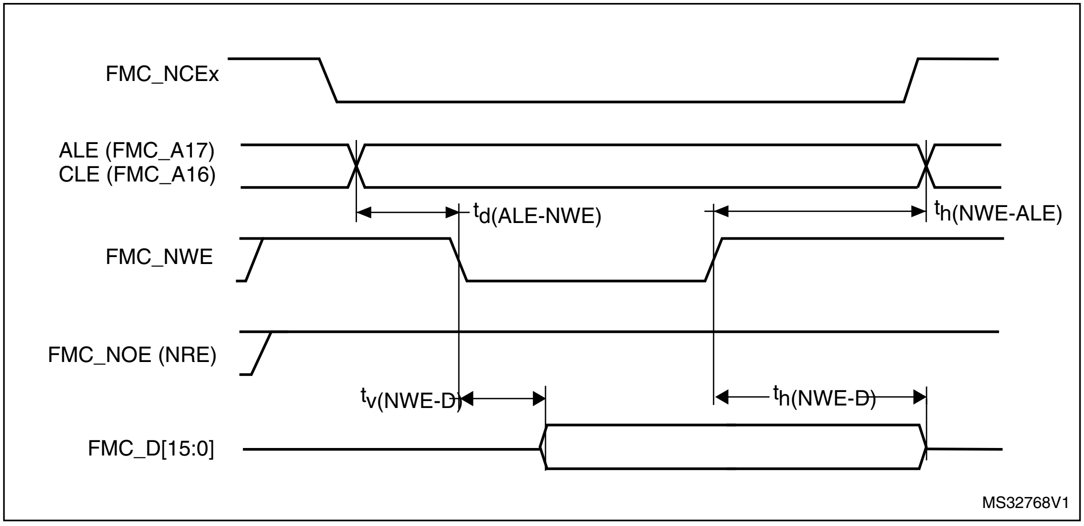


Figure 70. NAND controller waveforms for write access



5.3.35 DFSDM timing diagrams

Figure 80. Channel transceiver timing diagrams

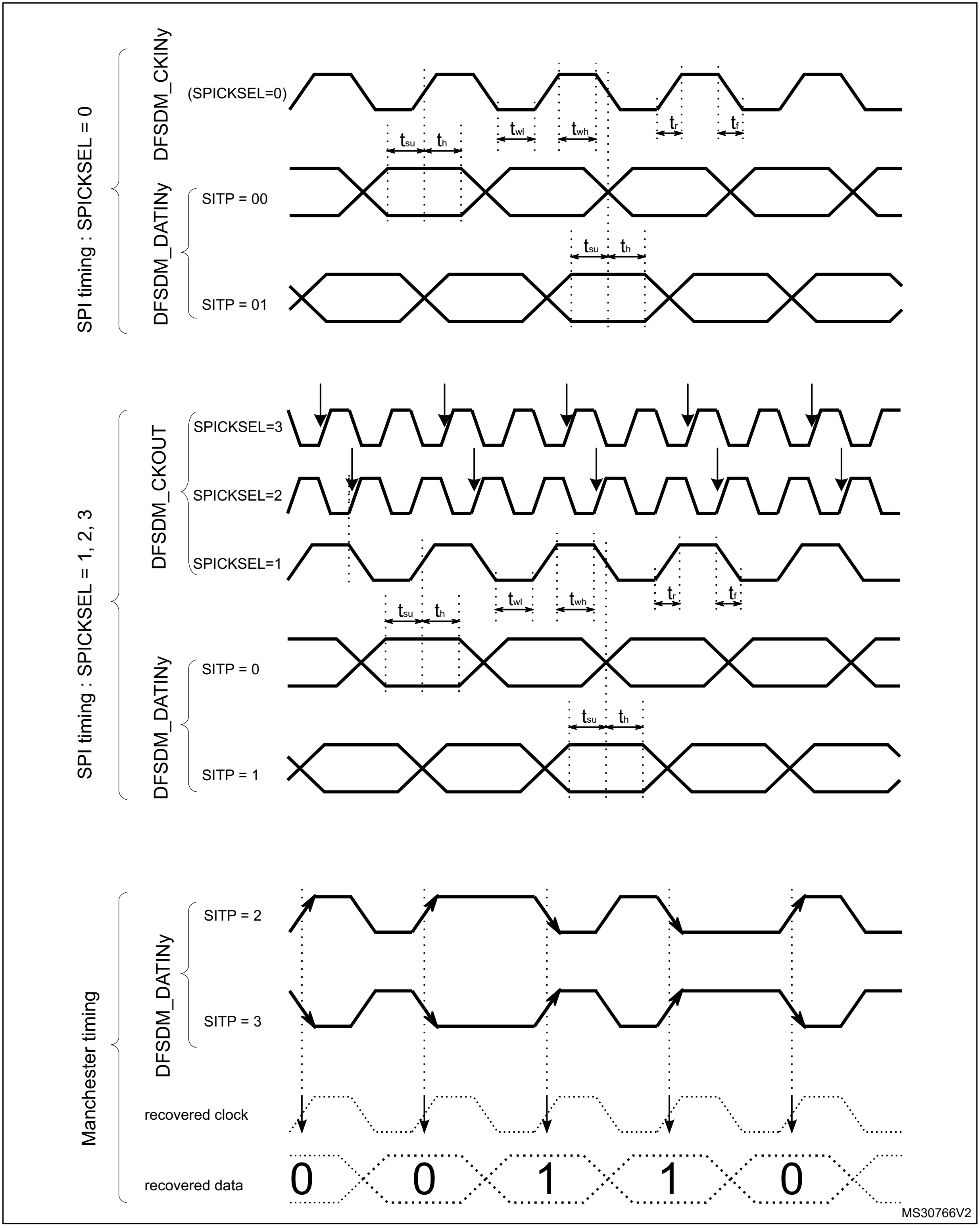
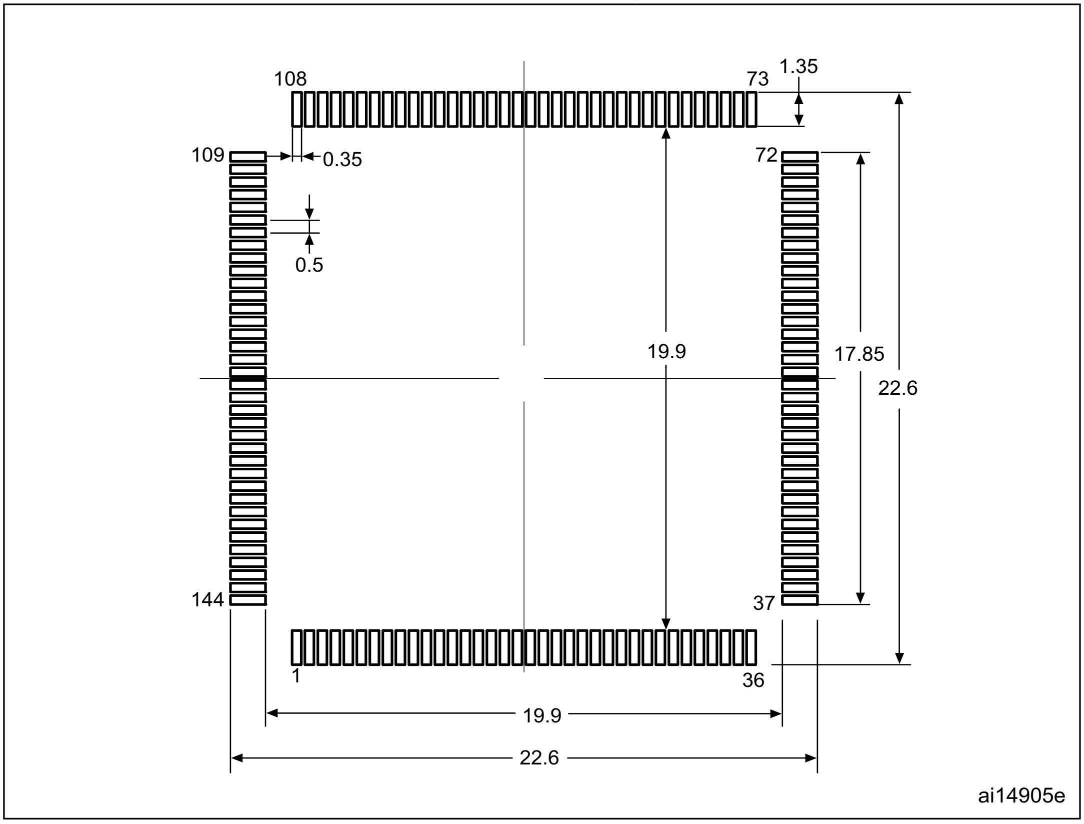


Figure 87. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 127. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0060
b	0.170	-	0.270	0.0067	-	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488
E	23.900	-	24.100	0.9409	-	0.9488
e	-	0.500	-	-	0.0197	-
HD	25.900	-	26.100	1.0200	-	1.0276
HE	25.900	-	26.100	1.0200	-	1.0276
L	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
ZD	-	1.250	-	-	0.0492	-
ZE	-	1.250	-	-	0.0492	-
ccc	-	-	0.080	-	-	0.0031
k	0 °	-	7 °	0 °	-	7 °

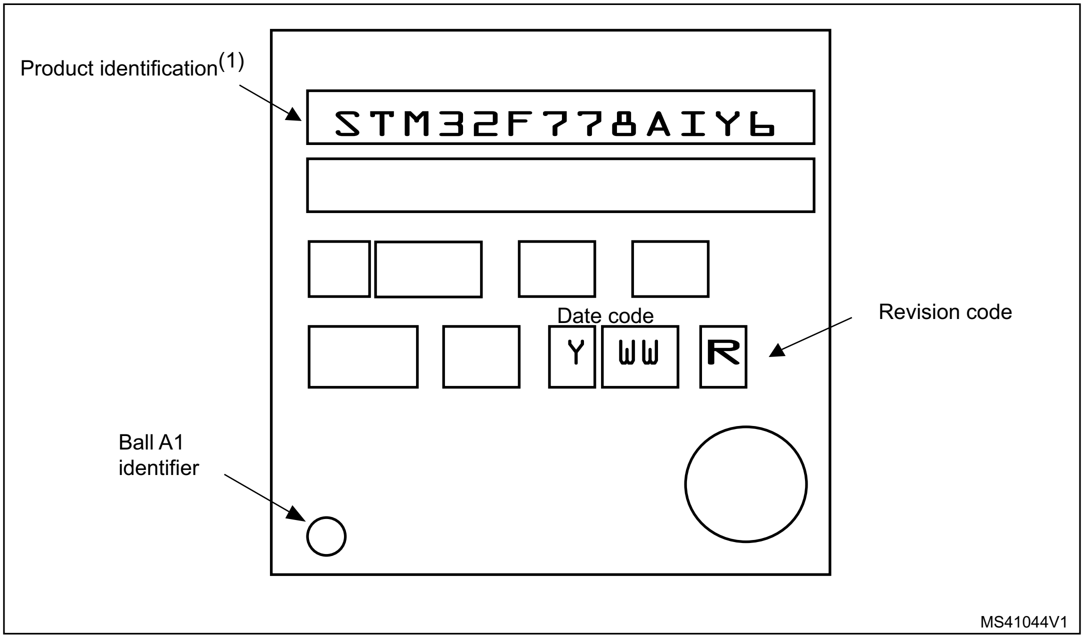
1. Values in inches are converted from mm and rounded to 4 decimal digits.

WLCSP180 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

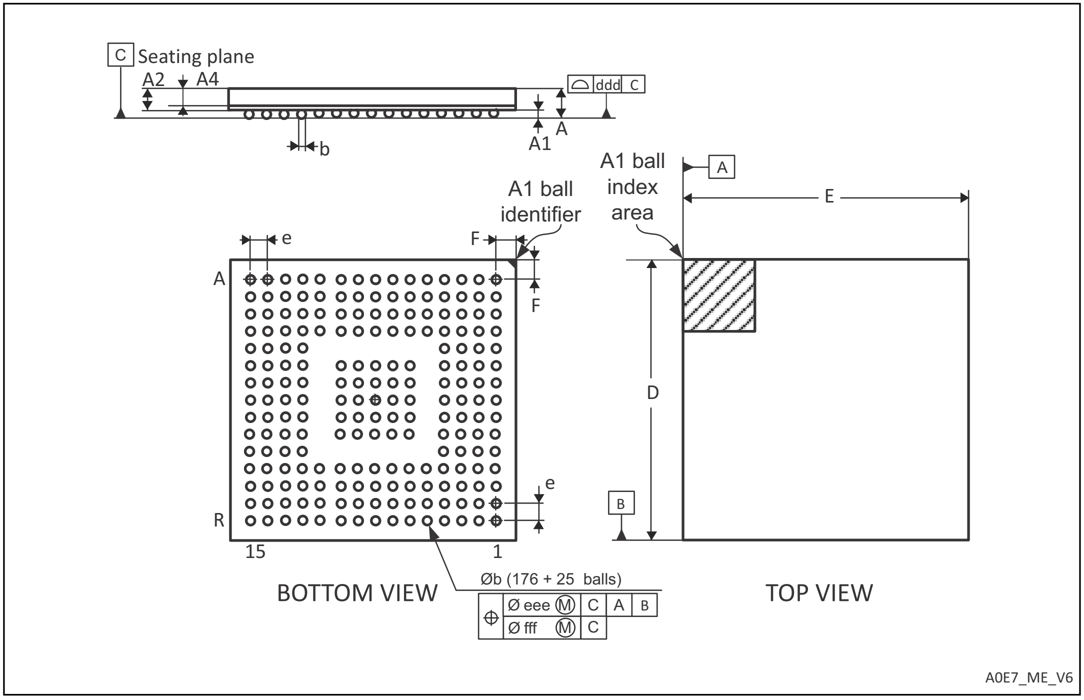
Figure 97. WLCSP180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.6 UFBGA176+25, 10 x 10, 0.65 mm ultra thin fine-pitch ball grid array package information

Figure 98. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 131. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.