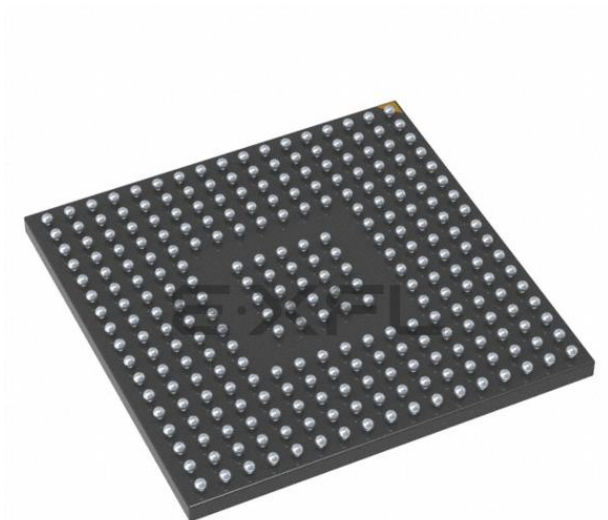




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Details

Product Status	Active
Core Processor	ARM® Cortex® -M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	132
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UF BGA
Supplier Device Package	176+25UF BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f777iik6

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2.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP100	Yes	No	Yes	No
LQFP144, LQFP208			Yes PDR_ON set to V _{DD}	Yes PDR_ON set to V _{SS}
LQFP176, UFBGA176, TFBGA216	Yes BYPASS_REG set to V _{SS}	Yes BYPASS_REG set to V _{DD}		
WLCSP180	Yes ⁽¹⁾			

1. Available only on dedicated part number. Refer to [Section 7: Ordering information](#).

2.20 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

2.31 SD/SDIO/MMC card host interface (SDMMC)

SDMMC host interfaces are available, that support the MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDMMC Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

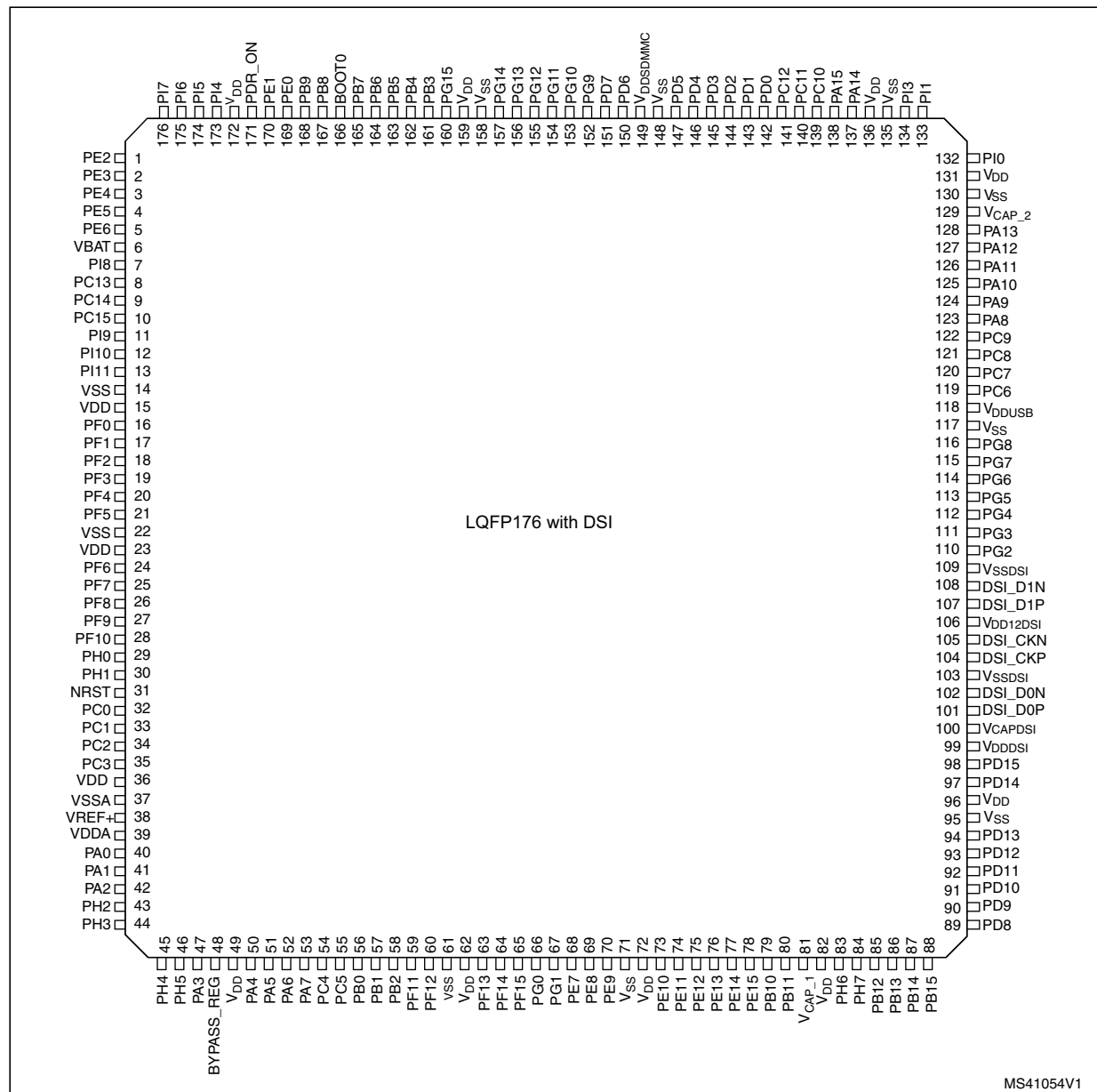
2.32 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

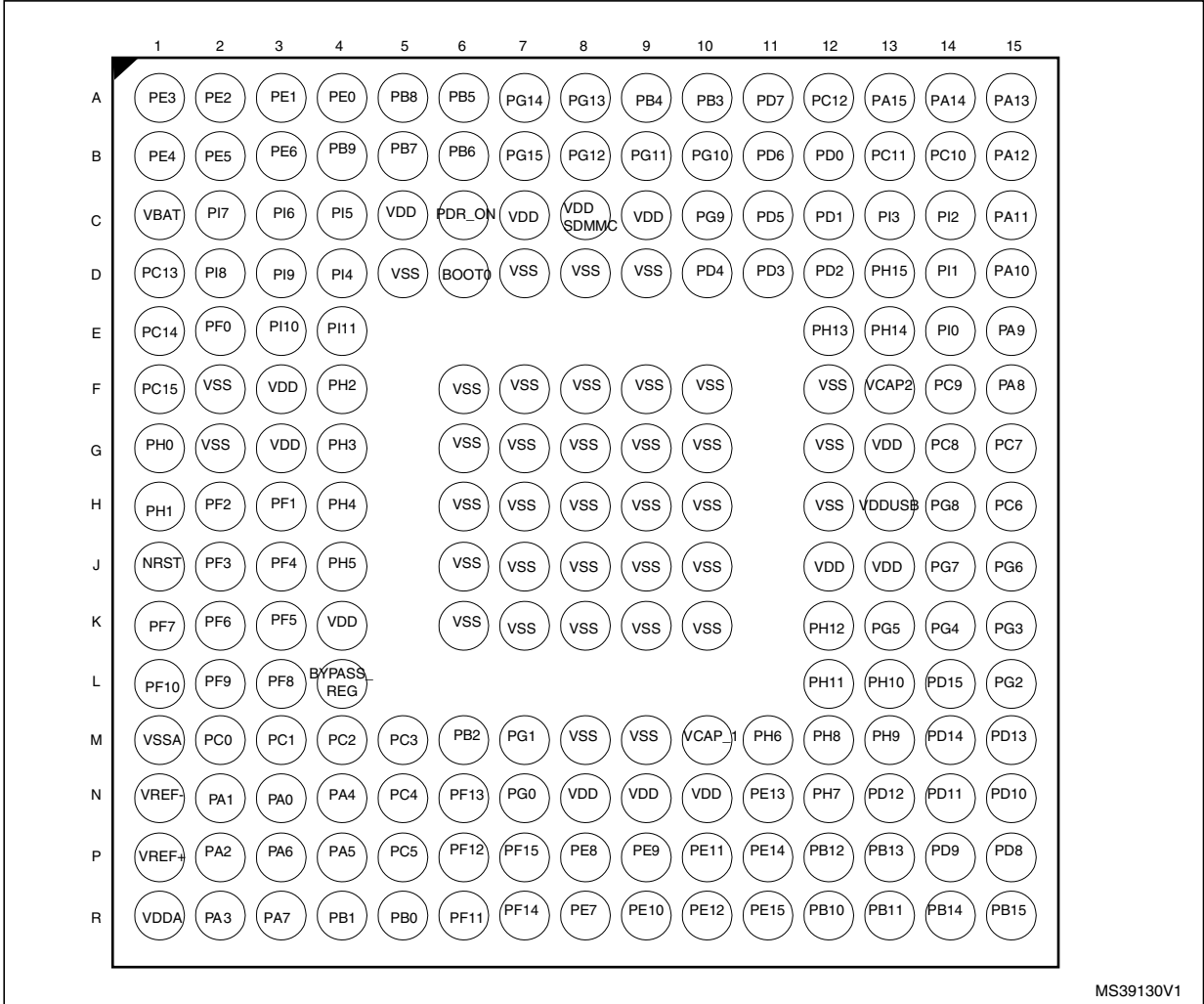
- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

Figure 14. STM32F779xx LQFP176 pinout



1. The above figure shows the package top view.

Figure 18. STM32F77xxx UFBGA176 ballout



MS39130V1

1. The above figure shows the package top view.

Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F777xx						STM32F778Ax STM32F779xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 ⁽¹⁾	LQFP176	LQFP208	TFBGA216						
96	140	B4	168	199	B4	D9	168	199	B4	PB9	I/O	FT	-	I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN7, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	A4	169	200	A6	C9	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A3	170	201	A5	B10	170	201	A5	PE1	I/O	FT	-	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	D5	-	202	F6	A11	-	202	F6	VSS	S	-	-	-	-
-	143	C6	171	203	E5	C10	171	203	E5	PDR_ON	S	-	-	-	-
100	144	C5	172	204	E7	B11	172	204	E7	VDD	S	-	-	-	-
-	-	D4	173	205	C3	D10	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCLK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	D3	D11	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	D6	C11	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	D4	B12	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	DA8	D8	D8
PE12	D9	DA9	D9	D9
PE13	D10	DA10	D10	D10
PE14	D11	DA11	D11	D11
PE15	D12	DA12	D12	D12
PD8	D13	DA13	D13	D13
PD9	D14	DA14	D14	D14
PD10	D15	DA15	D15	D15
PH8	D16	-	-	D16
PH9	D17	-	-	D17
PH10	D18	-	-	D18
PH11	D19	-	-	D19
PH12	D20	-	-	D20
PH13	D21	-	-	D21
PH14	D22	-	-	D22
PH15	D23	-	-	D23
PI0	D24	-	-	D24
PI1	D25	-	-	D25
PI2	D26	-	-	D26
PI3	D27	-	-	D27
PI6	D28	-	-	D28
PI7	D29	-	-	D29
PI9	D30	-	-	D30
PI10	D31	-	-	D31
PD7	NE1	NE1	-	-
PG6	NE3	-	-	-
PG9	NE2	NE2	NCE	-
PG10	NE3	NE3	-	-
PG11	-	-	-	-
PG12	NE4	NE4	-	-
PD3	CLK	CLK	-	-
PD4	NOE	NOE	NOE	-
PD5	NWE	NWE	NWE	-
PD6	NWAIT	NWAIT	NWAIT	-

Table 12. STM32F777xx, STM32F778Ax and STM32F779xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMCC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port A	PA11	-	TIM1_C_H4	-	-	-	SPI2_NS/S12S2_WS	UART4_RX	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVEN TOUT
	PA12	-	TIM1_ETR	-	-	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVEN TOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA15	JTDI	TIM2_C_H1/TIM2_ETR	-	-	HDMI-CEC	SPI1_NS/S12S1_WS	SPI3_NS/S12S3_WS	SPI6_NSS	UART4_RTS	-	-	CAN3_TX	UART7_TX	-	-	EVEN TOUT
Port B	PB0	-	TIM1_C_H2N	TIM3_C_H3	TIM8_CH2N	-	-	DFSDM1_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVEN TOUT
	PB1	-	TIM1_C_H3N	TIM3_C_H4	TIM8_CH3N	-	-	DFSDM1_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVEN TOUT
	PB2	-	-	-	-	-	-	SAI1_SDA	SPI3_MOSI/I2S3_SD	-	QUADSPI_CLK	DFSDM1_CKIN1	-	-	-	-	EVEN TOUT
	PB3	JTDO/TRACESWO	TIM2_C_H2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	-	SDMMC2_D2	CAN3_RX	UART7_RX	-	-	EVEN TOUT
	PB4	NJTRST	-	TIM3_C_H1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NS/S12S2_WS	SPI6_MISO	-	SDMMC2_D3	CAN3_TX	UART7_TX	-	-	EVEN TOUT
	PB5	-	UART5_RX	TIM3_C_H2	-	I2C1_SMB	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	SPI6_MOSI	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SD_CKE1	DCMI_D10	LCD_G7	EVEN TOUT
	PB6	-	UART5_TX	TIM4_C_H1	HDMI-CEC	I2C1_SCL	-	DFSDM1_DATIN5	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	I2C4_SCL	FMC_SD_NE1	DCMI_D5	-	EVEN TOUT



Table 12. STM32F777xx, STM32F778Ax and STM32F779xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C4/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port F	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVEN TOUT
	PF13	-	-	-	-	I2C4_SMB	-	DFSDM1_DATAIN6	-	-	-	-	-	FMC_A7	-	-	EVEN TOUT
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM1_CKIN6	-	-	-	-	-	FMC_A8	-	-	EVEN TOUT
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVEN TOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVEN TOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVEN TOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVEN TOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVEN TOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	-	-	EVEN TOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVEN TOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FMC_NE3	DCMI_D12	LCD_R7	EVEN TOUT
	PG7	-	-	-	-	-	-	SAI1_MCLK_A	-	USART6_CK	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVEN TOUT

Table 13. STM32F777xx, STM32F778Ax and STM32F779xx register boundary addresses⁽¹⁾ (continued)

Bus	Boundary address	Peripheral
	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	HDMI-CEC
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	I2C4
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	SPDIFRX
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	CAN3
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

1. The gray color is used for reserved Flash memory addresses.

Table 28. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode), regulator ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I _{DD}	Supply current in RUN mode	All peripherals enabled ⁽²⁾⁽³⁾	216	176	194	240	-	mA
			200	164	181	227	255	
			180	149	163	198	220	
			168	133	145	178	198	
			144	106	116	143	161	
			60	54	60	87	105	
			25	27	31	58	76	
		All peripherals disabled ⁽³⁾	216	77	88	135	-	
			200	72	82	129	157	
			180	67	75	110	131	
			168	60	67	99	120	
			144	50	56	83	101	
			60	29	34	60	78	
			25	15	19	45	63	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 31. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Single bank mode, ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator OFF

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ		Max ⁽¹⁾						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and VDD supply	All Peripherals Enabled ⁽²⁾⁽³⁾	180	152	1	167	2	200	2	220	2	mA
			168	136	1	148	2	179	2	198	2	
			144	105	1	115	2	141	2	158	2	
			60	47	1	53	2	79	2	96	2	
			25	22	1	27	2	53	2	70	2	
		All Peripherals Disabled ⁽³⁾	180	74	1	83	2	116	2	136	2	
			168	65	1	73	2	104	2	123	2	
			144	50	1	57	2	83	2	100	2	
			60	22	1	27	2	53	2	70	2	
			25	10	1	14	2	41	2	58	2	

1. Guaranteed by characterization results.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 32. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode, ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator OFF

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ		Max ⁽¹⁾						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and VDD supply	All Peripherals Enabled ⁽²⁾⁽³⁾	180	152	1	167	2	200	2	220	2	mA
			168	136	1	148	2	179	2	198	2	
			144	105	1	115	2	141	2	158	2	
			60	47	1	53	2	79	2	96	2	
			25	22	1	27	2	53	2	70	2	
		All Peripherals Disabled ⁽³⁾	180	74	1	82	2	114	2	137	2	
			168	65	1	73	2	104	2	123	2	
			144	50	1	57	2	83	2	100	2	
			60	22	1	27	2	53	2	70	2	
			25	10	1	14	2	41	2	58	2	

5.3.11 PLL characteristics

The parameters given in [Table 47](#) and [Table 48](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 47. Main PLL characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f _{PLL_IN}	PLL input clock ⁽¹⁾	-		0.95 ⁽²⁾	1	2.10	MHz
f _{PLL_OUT}	PLL multiplier output clock	-		24	-	216	
f _{PLL48_OUT}	48 MHz PLL multiplier output clock	-		-	48	75	
f _{VCO_OUT}	PLL VCO output	-		100	-	432	
t _{LOCK}	PLL lock time	VCO freq = 192 MHz		75	-	200	μs
		VCO freq = 432 MHz		100	-	300	
Jitter ⁽³⁾	Cycle-to-cycle jitter	System clock 216 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
I _{DD(PLL)} ⁽⁴⁾	PLL power consumption on V _{DD}	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
I _{D_{DA}(PLL)} ⁽⁴⁾	PLL power consumption on V _{D_{DA}}	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

Table 49. PLLISAI characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LOCK}	PLLISAI lock time	VCO freq = 192 MHz	75	-	200	μs
		VCO freq = 432 MHz	100	-	300	
Jitter ⁽³⁾	Master SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-
			peak to peak	-	± 280	-
	FS clock jitter	Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples	-	90	-	ps
		Cycle to cycle at 48 KHz on 1000 samples	-	400	-	ps
$I_{\text{DD(PLLISAI)}}^{(4)}$	PLLISAI power consumption on V_{DD}	VCO freq = 192 MHz	0.15	-	0.40	mA
		VCO freq = 432 MHz	0.45		0.75	
$I_{\text{DDA(PLLISAI)}}^{(4)}$	PLLISAI power consumption on V_{DDA}	VCO freq = 192 MHz	0.30	-	0.40	mA
		VCO freq = 432 MHz	0.55		0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

5.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 61: EMI characteristics](#)). It is available only on the main PLL.

Table 50. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15} - 1$	-

1. Guaranteed by design.

Equation 1

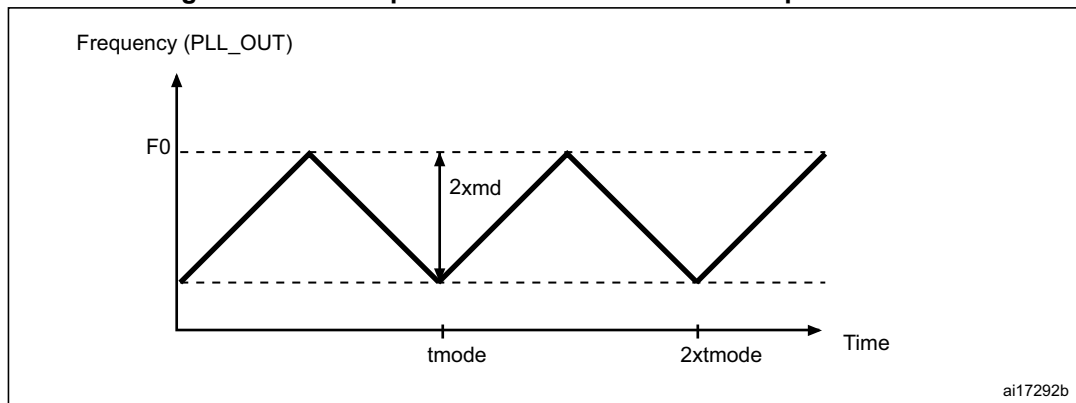
The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL_IN}} / (4 \times f_{\text{Mod}})]$$

$f_{\text{PLL_IN}}$ and f_{Mod} must be expressed in Hz.

As an example:

Figure 35. PLL output clock waveforms in down spread mode



5.3.13 MIPI D-PHY characteristics

The parameters given in [Table 51](#) and [Table 52](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 51. MIPI D-PHY characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Hi-Speed Input/Output Characteristics						
U _{INST}	UI instantaneous	-	2	-	12.5	ns
V _{CMTX}	HS transmit common mode voltage	-	150	200	250	mV
ΔV _{CMTX}	V _{CMTX} mismatch when output is Differential-1 or Differential-0	-	-	-	5	
V _{OD}	HS transmit differential voltage	-	140	200	270	
ΔV _{OD}	V _{OD} mismatch when output is Differential-1 or Differential-0	-	-	-	14	
V _{OHHS}	HS output high voltage	-	-	-	360	
Z _{OS}	Single ended output impedance	-	40	50	62.5	Ω
ΔZ _{OS}	Single ended output impedance mismatch	-	-	-	10	%
t _{HSr} & t _{HSf}	20%-80% rise and fall time	-	100	-	0.35*UI	ps
LP Receiver Input Characteristics						
V _{IL}	Logic 0 input voltage (not in ULP State)	-	-	-	550	mV
V _{IL-ULPS}	Logic 0 input voltage in ULP State	-	-	-	300	
V _{IH}	Input high level voltage	-	880	-	-	
V _{hys}	Voltage hysteresis	-	25	-	-	
LP Emitter Output Characteristics						

**Table 56. Flash memory programming (single bank configuration
nDBANK=1) (continued)**

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
V _{prog}	Programming voltage	32-bit program operation	2.7	-	3	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

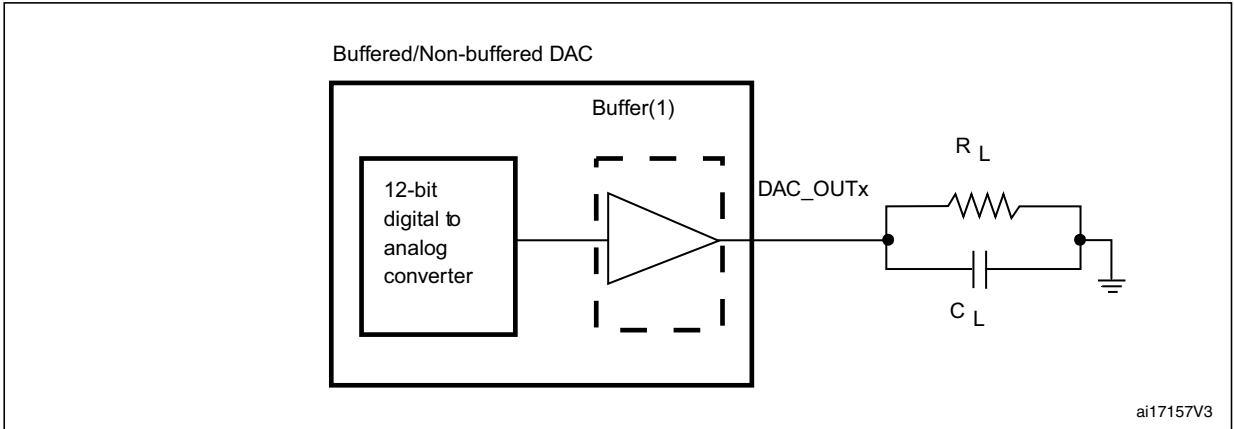
1. Guaranteed by characterization results.

2. The maximum programming time is measured after 100K erase operations.

**Table 57. Flash memory programming (dual bank configuration
nDBANK=0)**

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t _{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100 ⁽²⁾	μs
t _{ERASE16KB}	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	250	600	
		Program/erase parallelism (PSIZE) = x 32	-	200	500	
t _{ERASE64KB}	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1100	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	800	1400	
		Program/erase parallelism (PSIZE) = x 32	-	500	1100	
t _{ERASE128KB}	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2.1	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.5	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t _{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	

Figure 45. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.29 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0410 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

Table 83. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode		2	MHz
		Fast-mode	Analog filter ON DNF=0	8	
			Analog filter OFF DNF=1	9	
		Fast-mode Plus	Analog filter ON DNF=0	16	
			Analog filter OFF DNF=1	16	

Figure 65. Synchronous multiplexed NOR/PSRAM read timings

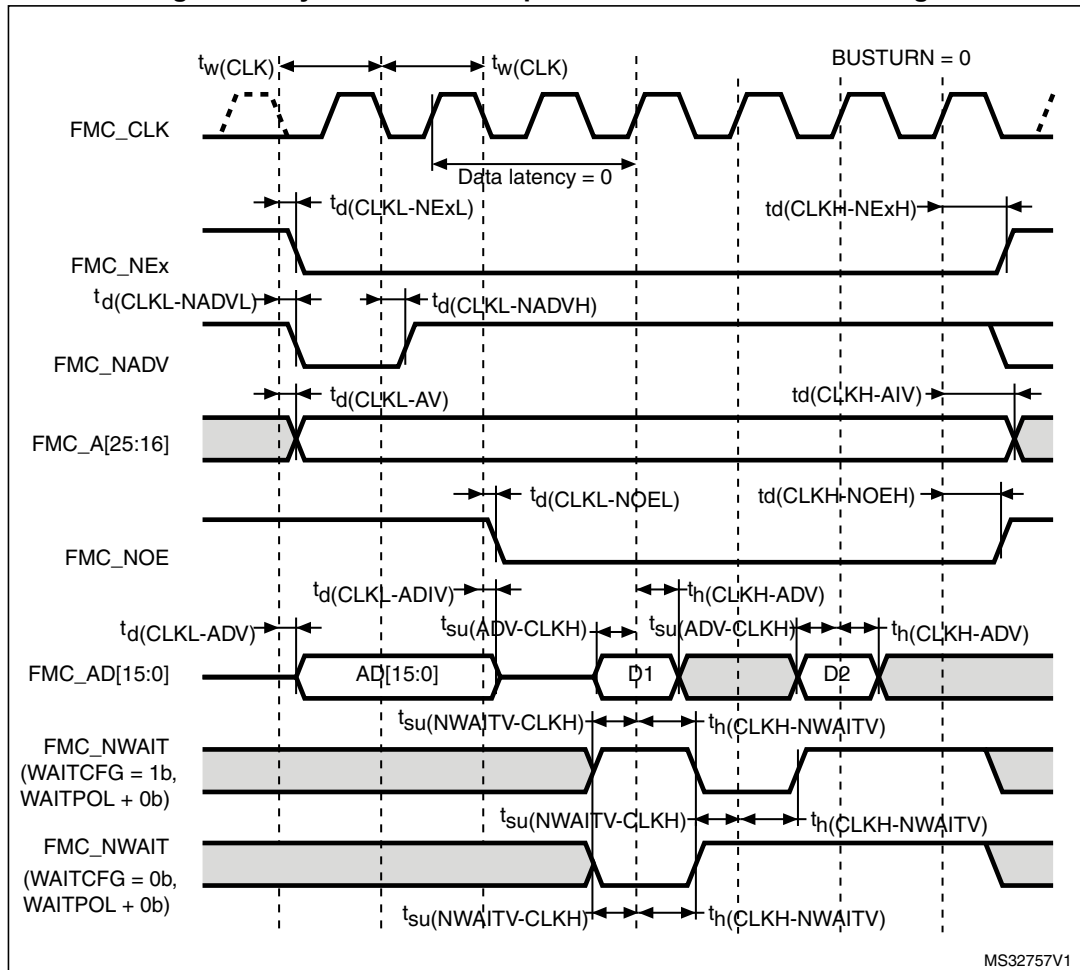


Figure 71. NAND controller waveforms for common memory read access

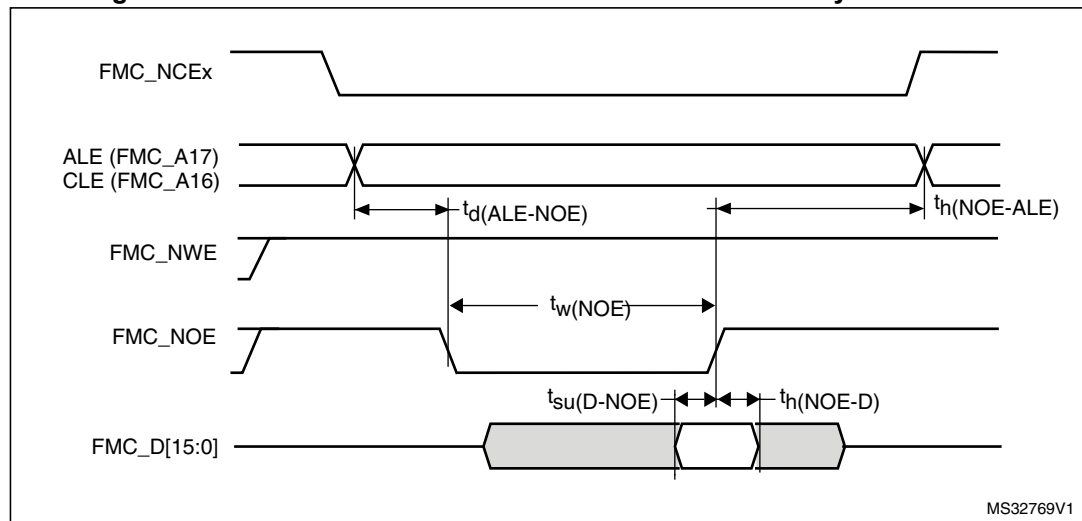
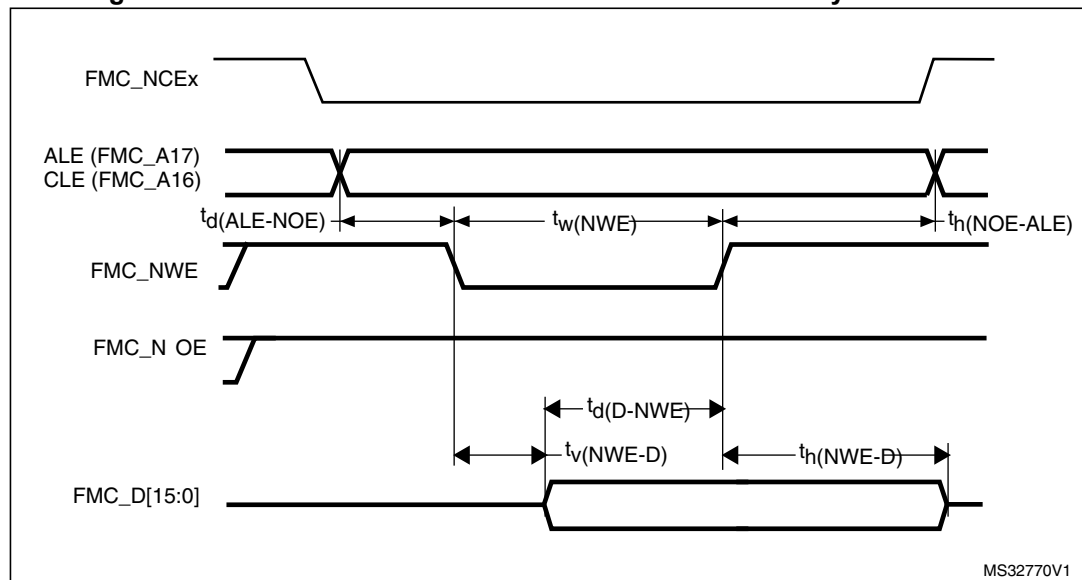


Figure 72. NAND controller waveforms for common memory write access

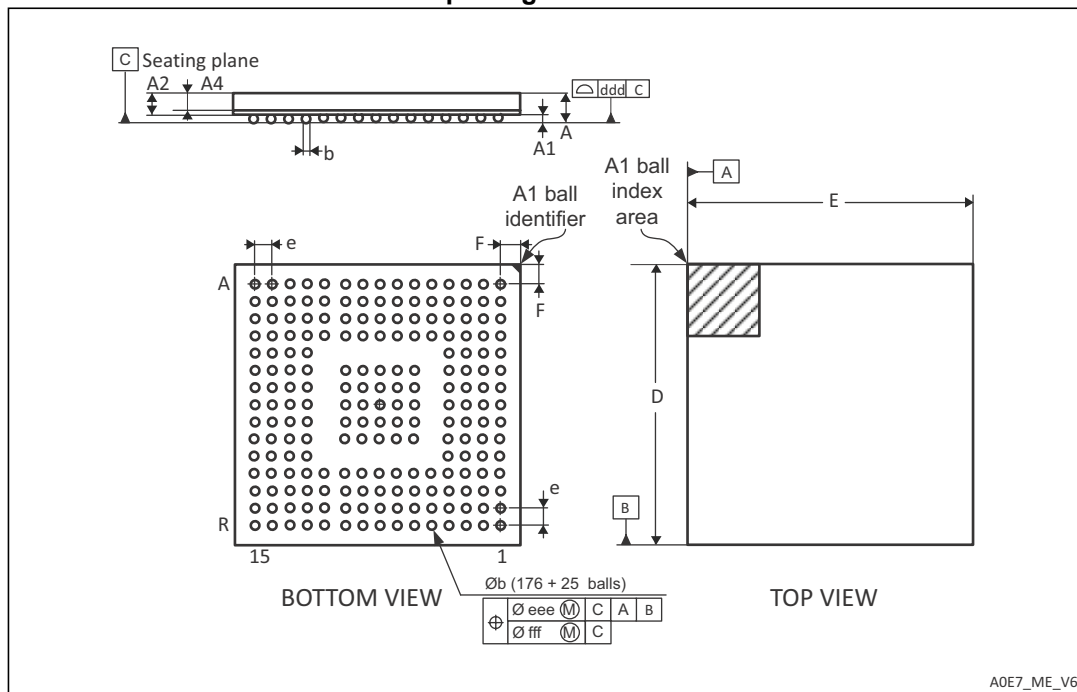
Table 112. Switching characteristics for NAND Flash read cycles⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FMC_NOE low width	$4T_{HCLK} - 0.5$	$4T_{HCLK} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15:0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15:0] valid data after FMC_NOE high	0	-	
$t_d(ALE-NOE)$	FMC_ALE valid before FMC_NOE low	-	$3T_{HCLK} + 1$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{HCLK} - 2$	-	

1. Guaranteed by characterization results.

6.6 UFBGA176+25, 10 x 10, 0.65 mm ultra thin fine-pitch ball grid array package information

Figure 98. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 131. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.