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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 216MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 82 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f777vit6 |

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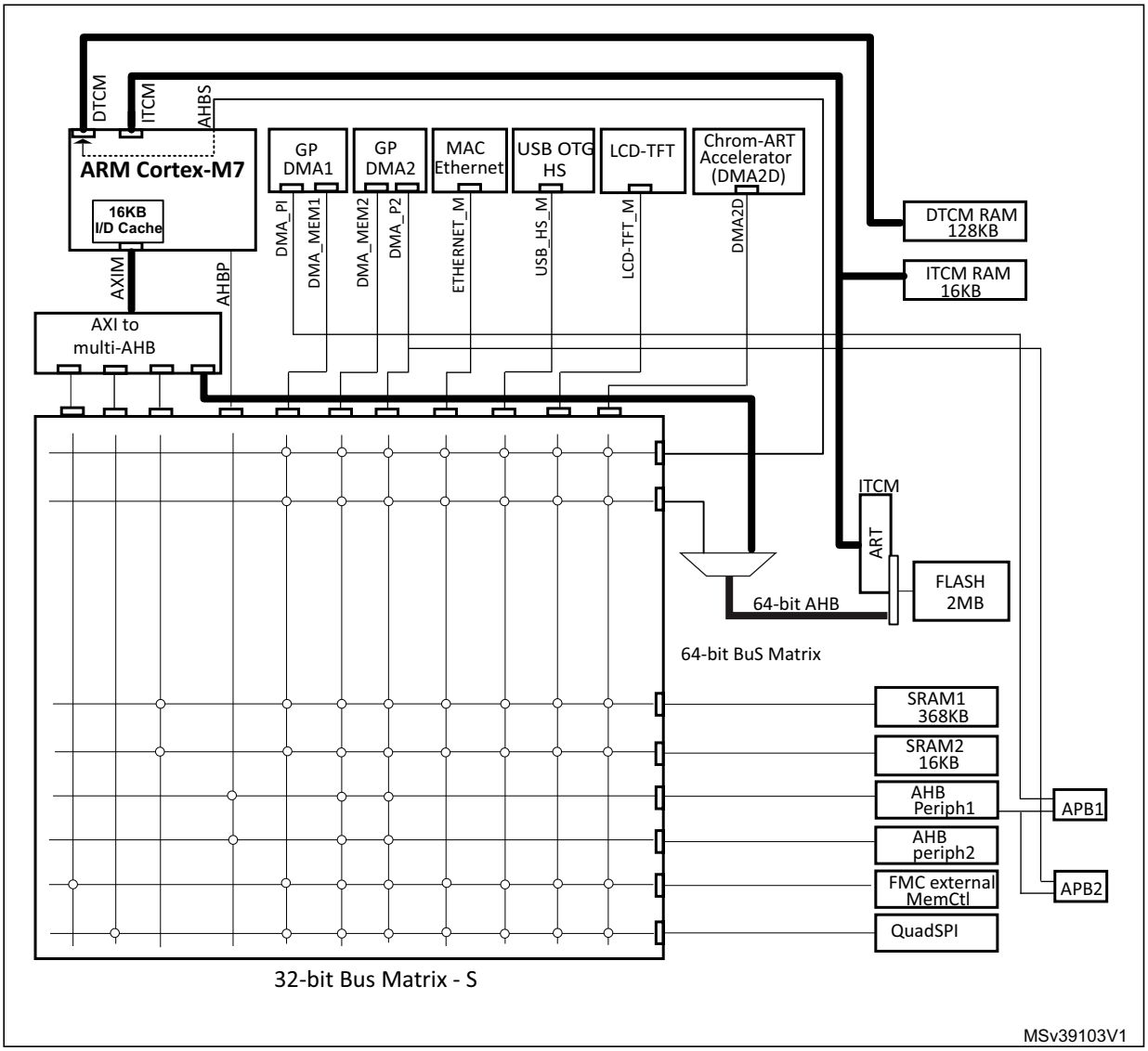
FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

**Figure 3. STM32F777xx, STM32F778Ax and STM32F779xx AXI-AHB bus matrix architecture(1)**




1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

**Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F777xx | | | | | | STM32F778Ax STM32F779xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 3 | 3 | B1 | 3 | 3 | A1 | C12 | 3 | 3 | A1 | PE4 | I/O | FT | - | TRACED1, SPI4_NSS, SAI1_FS_A, DFSDM1_DATIN3, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT | - |
| 4 | 4 | B2 | 4 | 4 | B1 | D12 | 4 | 4 | B1 | PE5 | I/O | FT | - | TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, DFSDM1_CKIN3, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT | - |
| 5 | 5 | B3 | 5 | 5 | B2 | E11 | 5 | 5 | B2 | PE6 | I/O | FT | - | TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCLK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT | - |
| - | - | - | - | - | G6 | - | - | - | G6 | VSS | S | - | - | - | - |
| - | - | - | - | - | F5 | - | - | - | F5 | VDD | S | - | - | - | - |
| 6 | 6 | C1 | 6 | 6 | C1 | C13 | 6 | 6 | C1 | VBAT | S | - | - | - | - |
| - | - | D2 | 7 | 7 | C2 | NC | 7 | 7 | C2 | PI8 | I/O | FT | (2) | EVENTOUT | RTC_TAMP2/RTC_TS/ WKUP5 |
| 7 | 7 | D1 | 8 | 8 | D1 | D13 | 8 | 8 | D1 | PC13 | I/O | FT | (2) | EVENTOUT | RTC_TAMP1/RTC_TS/ RTC_OUT/ WKUP4 |
| 8 | 8 | E1 | 9 | 9 | E1 | E12 | 9 | 9 | E1 | PC14-OSC32_IN | I/O | FT | (2) (3) | EVENTOUT | OSC32_IN |
| 9 | 9 | F1 | 10 | 10 | F1 | E13 | 10 | 10 | F1 | PC15-OSC32_OUT | I/O | FT | (2) (3) | EVENTOUT | OSC32_OUT |
| - | - | - | - | - | G5 | - | - | - | G5 | VDD | S | - | - | - | - |

**Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F777xx | | | | | | STM32F778Ax STM32F779xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 65 | 98 | G14 | 117 | 140 | G14 | G8 | 121 | 140 | G14 | PC8 | I/O | FT | - | TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, FMC_NE2/FMC_NCE, SDMMC1_D0, DCMI_D2, EVENTOUT | |
| 66 | 99 | F14 | 118 | 141 | F14 | E1 | 122 | 141 | F14 | PC9 | I/O | FT | - | MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT | -- |
| 67 | 100 | F15 | 119 | 142 | F15 | E2 | 123 | 142 | F15 | PA8 | I/O | FT | - | MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, CAN3_RX, UART7_RX, LCD_B3, LCD_R6, EVENTOUT | - |
| 68 | 101 | E15 | 120 | 143 | E15 | F4 | 124 | 143 | E15 | PA9 | I/O | FT | - | TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, LCD_R5, EVENTOUT | OTG_FS_VBUS |
| 69 | 102 | D15 | 121 | 144 | D15 | F5 | 125 | 144 | D15 | PA10 | I/O | FT | - | TIM1_CH3, USART1_RX, LCD_B4, OTG_FS_ID, MDIOS_MDIO, DCMI_D1, LCD_B1, EVENTOUT | - |
| 70 | 103 | C15 | 122 | 145 | C15 | E3 | 126 | 145 | C15 | PA11 | I/O | FT | - | TIM1_CH4, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT | - |

**Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F777xx | | | | | | STM32F778Ax STM32F779xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 96 | 140 | B4 | 168 | 199 | B4 | D9 | 168 | 199 | B4 | PB9 | I/O | FT | - | I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN7, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT | - |
| 97 | 141 | A4 | 169 | 200 | A6 | C9 | 169 | 200 | A6 | PE0 | I/O | FT | - | TIM4_ETR, LPTIM1_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT | - |
| 98 | 142 | A3 | 170 | 201 | A5 | B10 | 170 | 201 | A5 | PE1 | I/O | FT | - | LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT | - |
| 99 | - | D5 | - | 202 | F6 | A11 | - | 202 | F6 | VSS | S | - | - | - | - |
| - | 143 | C6 | 171 | 203 | E5 | C10 | 171 | 203 | E5 | PDR_ON | S | - | - | - | - |
| 100 | 144 | C5 | 172 | 204 | E7 | B11 | 172 | 204 | E7 | VDD | S | - | - | - | - |
| - | - | D4 | 173 | 205 | C3 | D10 | 173 | 205 | C3 | PI4 | I/O | FT | - | TIM8_BKIN, SAI2_MCLK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT | - |
| - | - | C4 | 174 | 206 | D3 | D11 | 174 | 206 | D3 | PI5 | I/O | FT | - | TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT | - |
| - | - | C3 | 175 | 207 | D6 | C11 | 175 | 207 | D6 | PI6 | I/O | FT | - | TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT | - |
| - | - | C2 | 176 | 208 | D4 | B12 | 176 | 208 | D4 | PI7 | I/O | FT | - | TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT | - |

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.
4. Guaranteed by test in production.

**Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Single bank mode, ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All peripherals enabled(2)(3) | 216 | 190 | 219 | 255 | - | mA |
| | | | 200 | 177 | 205 | 241 | 268 | |
| | | | 180 | 157 | 173 | 208 | 228 | |
| | | | 168 | 139 | 153 | 185 | 204 | |
| | | | 144 | 107 | 117 | 144 | 161 | |
| | | | 60 | 48 | 54 | 81 | 98 | |
| | | | 25 | 23 | 28 | 54 | 71 | |
| | | All peripherals disabled(3) | 216 | 92 | 104 | 150 | - | |
| | | | 200 | 86 | 97 | 143 | 170 | |
| | | | 180 | 76 | 85 | 119 | 140 | |
| | | | 168 | 67 | 75 | 107 | 126 | |
| | | | 144 | 52 | 58 | 84 | 101 | |
| | | | 60 | 23 | 28 | 54 | 71 | |
| | | | 25 | 11 | 15 | 42 | 56 | |

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

## 5.3.17 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 60*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 60. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 216 MHz, conforms to IEC 61000-4-2 | 2B |
| $V_{FTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ =+25 °C, $f_{HCLK}$ = 168 MHz, conforms to IEC 61000-4-2 | 5A |

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

**Table 62. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to ANSI/ESDA/JEDEC JS-001-2012 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to ANSI/ESD S5.3.1-2009, all the packages | 3 | 250 | |

1. Guaranteed by characterization results.

### Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

**Table 63. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 5.3.19 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 64*.

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.
- The 20mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load Cload supported in Fm+, which is given by these formulas:

  $Tr(SDA/SCL)=0.8473xR_pxC_{load}$

  $R_p(min)= (VDD-V_{OL}(max))/I_{OL}(max)$

Where Rp is the I2C lines pull-up. Refer to Section 5.3.20: I/O port characteristics for the I2C I/Os characteristics.

All $I^2C$ SDA and SCL I/Os embed an analog filter. Refer to *Table 84* for the analog filter characteristics:

**Table 84. I2C analog filter characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50(2) | 70(3) | ns |

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

**Table 85. SPI dynamic characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tsu(MI) | Data input setup time | Master mode | 4<br>9(4) | - | - | ns |
| tsu(SI) | | Slave mode | 4.5 | - | - | |
| th(MI) | Data input hold time | Master mode | 3<br>0(4) | - | - | |
| th(SI) | | Slave mode | 2 | - | - | |
| ta(SO) | Data output access time | Slave mode | 7 | - | 21 | |
| tdis(SO) | Data output disable time | Slave mode | 5 | - | 12 | |
| tv(SO) | Data output valid time | Slave mode 2.7≤VDD≤3.6V | - | 6.5 | 10 | |
| | | Slave mode 1.71≤VDD≤3.6V | - | 6.5 | 13.5 | |
| tv(MO) | | Master mode | - | 2 | 6 | |
| th(SO) | Data output hold time | Slave mode<br>1.71≤VDD≤3.6V | 4.5 | - | - | |
| th(MO) | | Master mode | 0 | - | - | |

1. Guaranteed by characterization results.
2. Excepting SPI1 with SCK IO pin mapped on PA5. In this configuration, Maximum achievable frequency is 40MHz.
3. Maximum Frequency of Slave Transmitter is determined by sum of Tv(SO) and Tsu(MI) intervals which has to fit into SCK level phase preceding the SCK sampling edge.This value can be achieved when it communicates with a Master having Tsu(MI)=0 while signal Duty(SCK)=50%.
4. Only for SPI6.

**Figure 46. SPI timing diagram - slave mode and CPHA = 0**

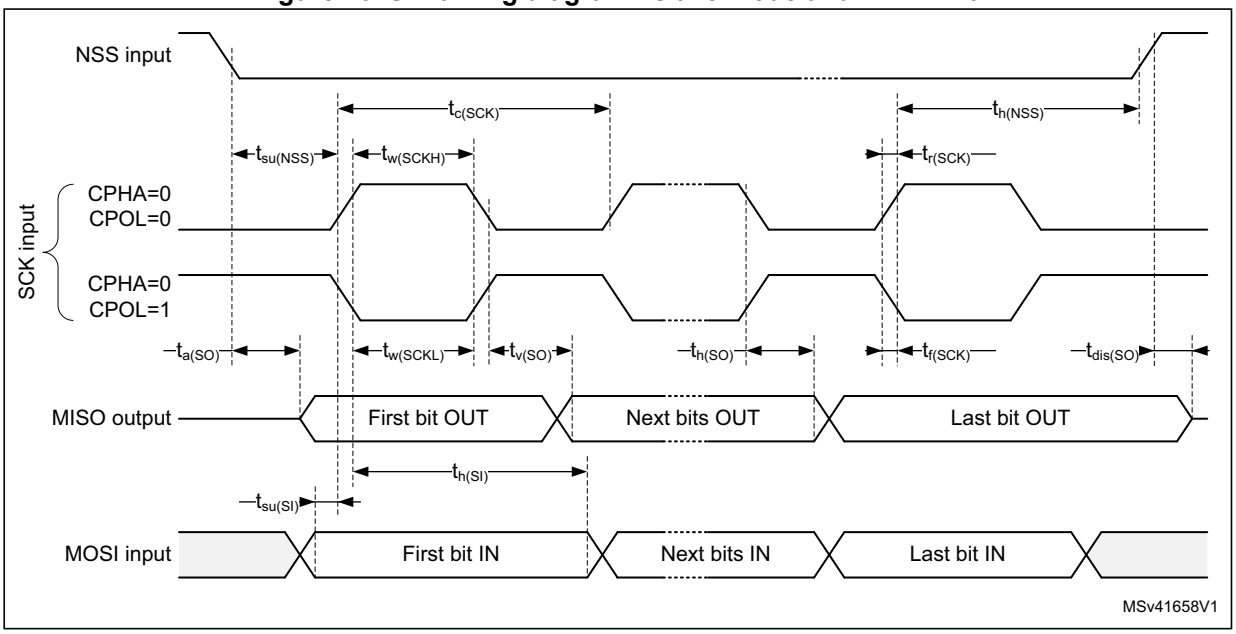
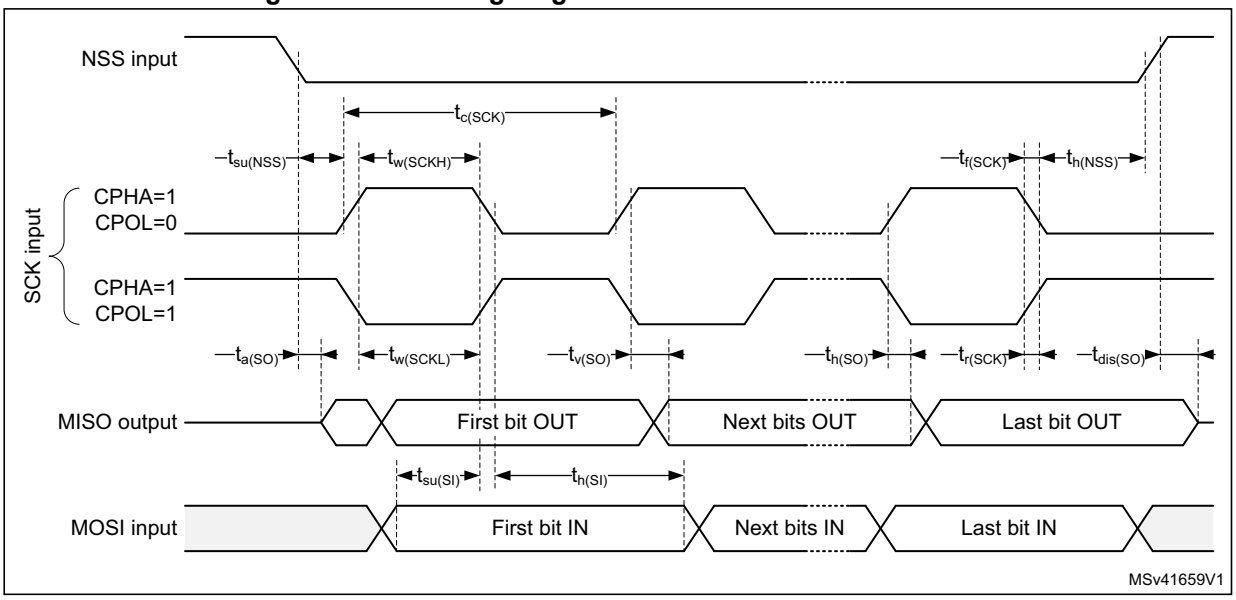
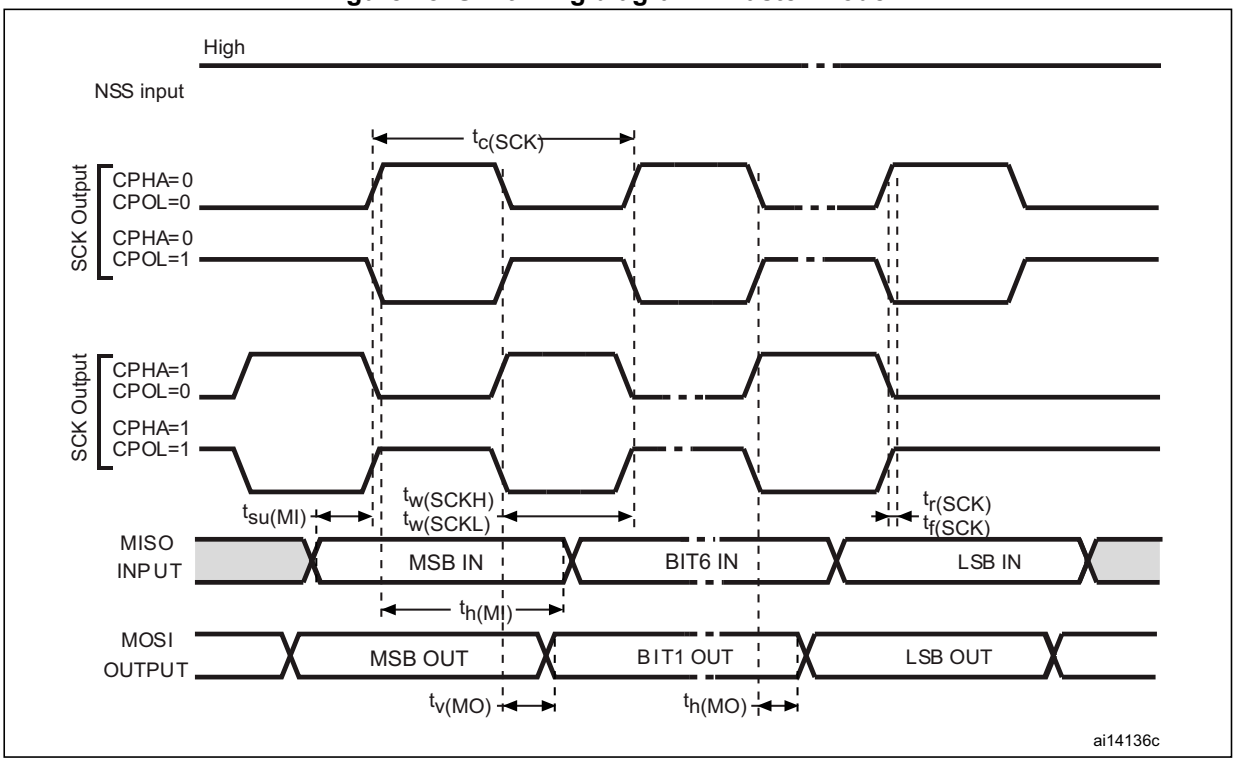


**Figure 47. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at $0.5V_{DD}$ and with external $C_L$ = 30 pF.

**Figure 48. SPI timing diagram - master mode(1)**




1. Measurement points are done at $0.5V_{DD}$ and with external $C_L$ = 30 pF.

1. Guaranteed by characterization results.

**Table 107. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $9T_{HCLK} - 1$ | $9T_{HCLK} + 1$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $7T_{HCLK} - 0.5$ | $7T_{HCLK} + 0.5$ | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $6T_{HCLK} + 2$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK} - 1$ | - | |

1. Guaranteed by characterization results.

## Synchronous waveforms and timings

*Figure 65* through *Figure 68* represent synchronous waveforms and *Table 108* through *Table 111* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all the timing tables, the $T_{HCLK}$ is the HCLK clock period.

– For 2.7 V≤ $V_{DD}$≤ 3.6 V, maximum FMC_CLK = 100 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).

– For 1.71 V≤ $V_{DD}$<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

**Figure 66. Synchronous multiplexed PSRAM write timings**

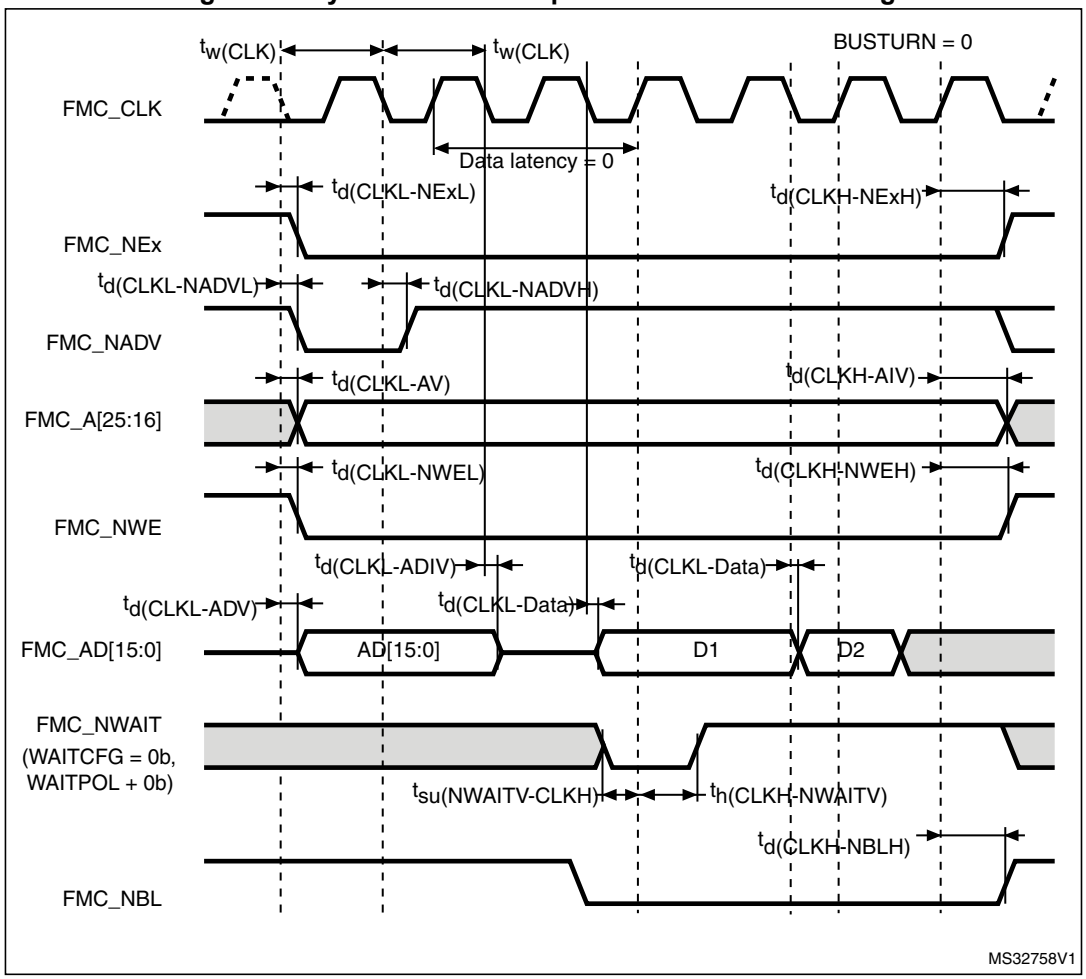


**Figure 71. NAND controller waveforms for common memory read access**

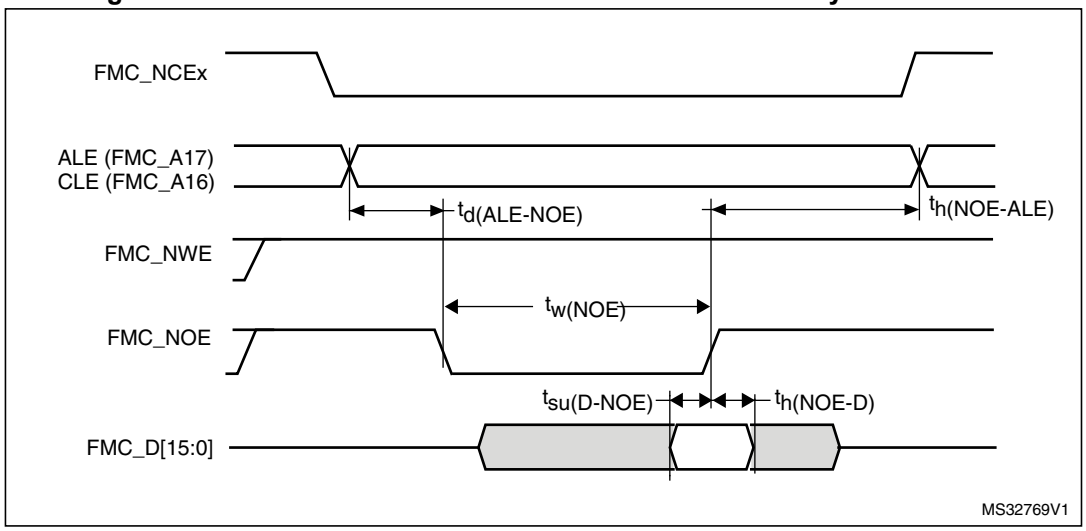



**Figure 72. NAND controller waveforms for common memory write access**

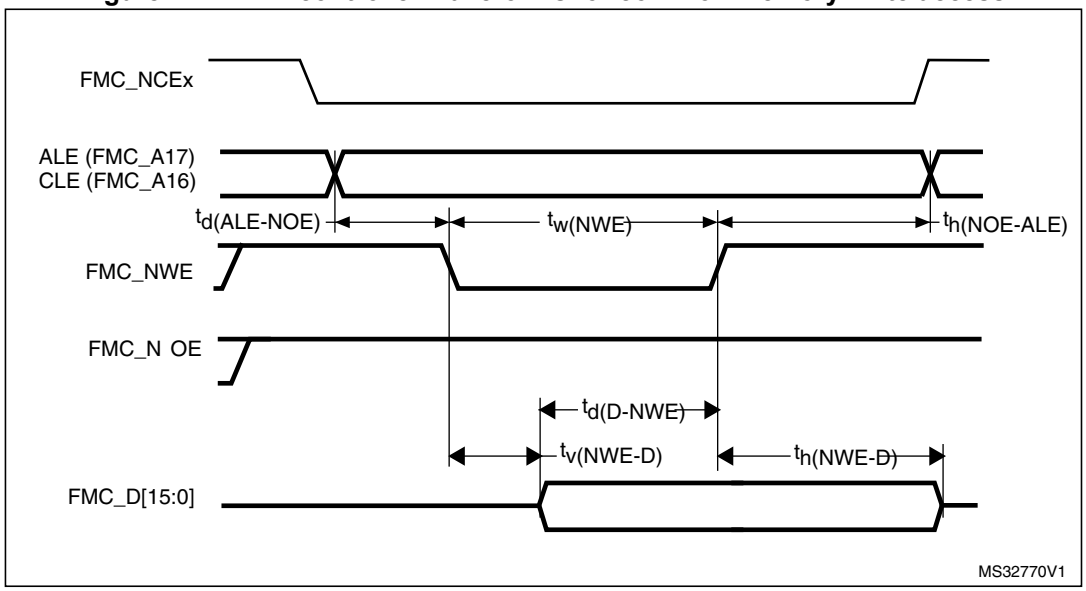



**Table 112. Switching characteristics for NAND Flash read cycles(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(N0E)}$ | FMC_NOE low width | $4T_{HCLK} - 0.5$ | $4T_{HCLK} + 0.5$ | ns |
| $t_{su(D-NOE)}$ | FMC_D[15-0] valid data before FMC_NOE high | 11 | - | |
| $t_{h(NOE-D)}$ | FMC_D[15-0] valid data after FMC_NOE high | 0 | - | |
| $t_{d(ALE-NOE)}$ | FMC_ALE valid before FMC_NOE low | - | $3T_{HCLK} + 1$ | |
| $t_{h(NOE-ALE)}$ | FMC_NWE high to FMC_ALE invalid | $4T_{HCLK} - 2$ | - | |

1. Guaranteed by characterization results.

**Table 117. LPSDR SDRAM write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK} - 0.5$ | $2T_{HCLK} + 0.5$ | ns |
| $t_{d(SDCLKL\_Data)}$ | Data output valid time | - | 2.5 | |
| $t_{h(SDCLKL\_Data)}$ | Data output hold time | 0 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 2.5 | |
| $t_{d(SDCLKL-SDNWE)}$ | SDNWE valid time | - | 2.5 | |
| $t_{h(SDCLKL-SDNWE)}$ | SDNWE hold time | 0 | - | |
| $t_{d(SDCLKL-SDNE)}$ | Chip select valid time | - | 0.5 | |
| $t_{h(SDCLKL-SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL-SDNRAS)}$ | SDNRAS valid time | - | 1.5 | |
| $t_{h(SDCLKL-SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS valid time | - | 1.5 | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

## 5.3.31 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 118* and *Table 119* for Quad-SPI are derived from tests performed under the ambient temperature, $f_{AHB}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17: General operating conditions*, with the following configuration:

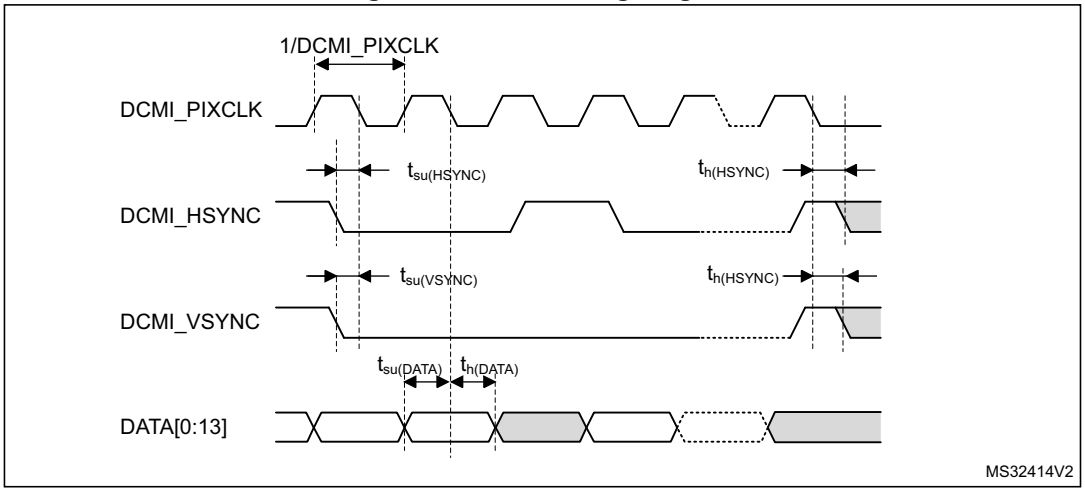
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics.

**Table 118. Quad-SPI characteristics in SDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fck1/t(CK) | Quad-SPI clock frequency | 2.7 V≤ $V_{DD}$<3.6 V CL=20 pF | - | - | 108 | MHz |
| | | 1.71 V<$V_{DD}$<3.6 V CL=15 pF | - | - | 100 | |

**Figure 77. DCMI timing diagram**




## 5.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 121* for LCD-TFT are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage summarized in *Table 17*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits

**Table 121. LTDC characteristics (1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{CLK}$ | LTDC clock output frequency | - | 65 | MHz |
| $D_{CLK}$ | LTDC clock output duty cycle | 45 | 55 | % |
| $t_{w(CLKH)}$, $t_{w(CLKL)}$ | Clock High time, low time | tw(CLK)/2−0.5 | tw(CLK)/2+0.5 | ns |
| $t_{v(DATA)}$ | Data output valid time | - | 6 | |
| $t_{h(DATA)}$ | Data output hold time | 0 | - | |
| $t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$ | HSYNC/VSYNC/DE output valid time | - | 3.5 | |
| $t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$ | HSYNC/VSYNC/DE output hold time | 0.5 | - | |

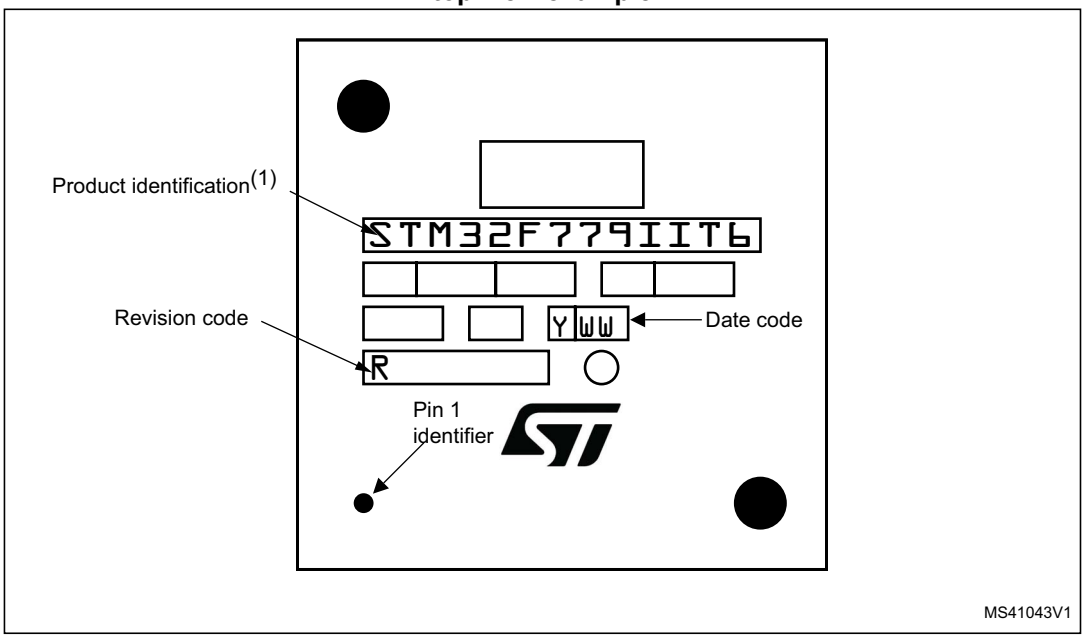
1. Guaranteed by characterization results.

### LQFP176 device marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 91. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Table 129. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.230 |
| A1 | - | 0.175 | - | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3 | - | 0.025 | - | - | 0.0010 | - |
| b[2] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 5.502 | 5.537 | 5.572 | 0.2166 | 0.2180 | 0.2194 |
| E | 6.060 | 6.095 | 6.130 | 0.2386 | 0.2400 | 0.2413 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 4.800 | - | - | 0.1890 | - |
| e2 | - | 5.200 | - | - | 0.2047 | - |
| F | - | 0.368 | - | - | 0.0145 | - |
| G | - | 0.477 | - | - | 0.0188 | - |
| aaa | - | 0.110 | - | - | 0.0043 | - |
| bbb | - | 0.110 | - | - | 0.0043 | - |
| ccc | - | 0.110 | - | - | 0.0043 | - |
| ddd | - | 0.050 | - | - | 0.0020 | - |
| eee | - | 0.050 | - | - | 0.0020 | - |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.