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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex® -M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	159
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f779bit6

2 Functional overview

2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering an outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow an efficient signal processing and a complex algorithm execution.

It supports single and double precision FPU (floating point unit), speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 2 shows the general block diagram of the STM32F77xxx family.

Note: The Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

- LPR is used in the Stop modes:
The LP regulator mode is configured by software when entering Stop mode.
Like the MR mode, the LPR can be configured in two ways during stop mode:
 - LPR operates in normal mode (default mode when LPR is ON)
 - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.
The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to [Table 3](#) for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode⁽¹⁾

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode ⁽²⁾	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.

2. The over-drive mode is not available when $V_{DD} = 1.7$ to 2.1 V.

2.19.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

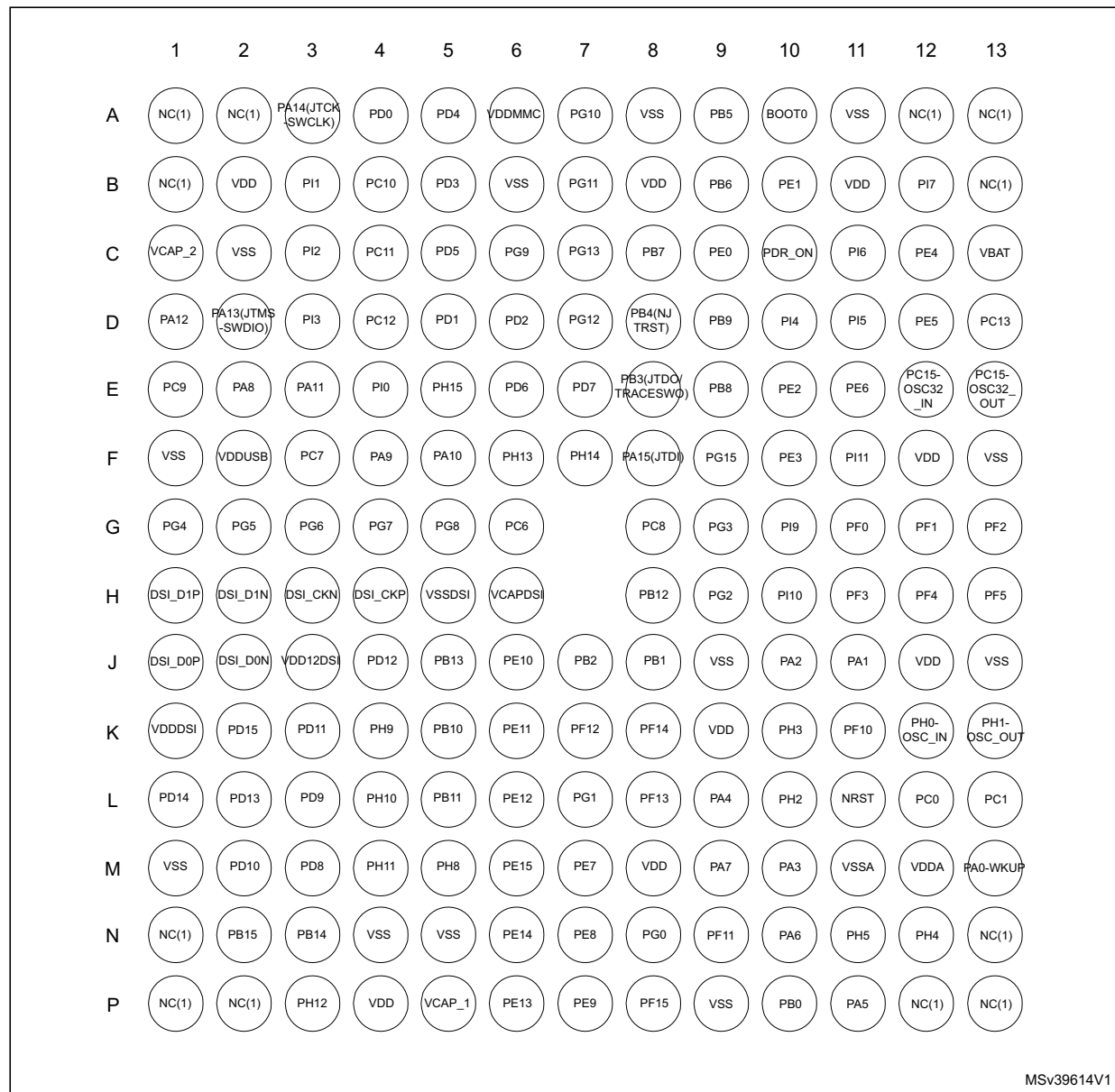
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. The two $2.2\ \mu\text{F}$ ceramic capacitors should be replaced by two $100\ \text{nF}$ decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12} . An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In the regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

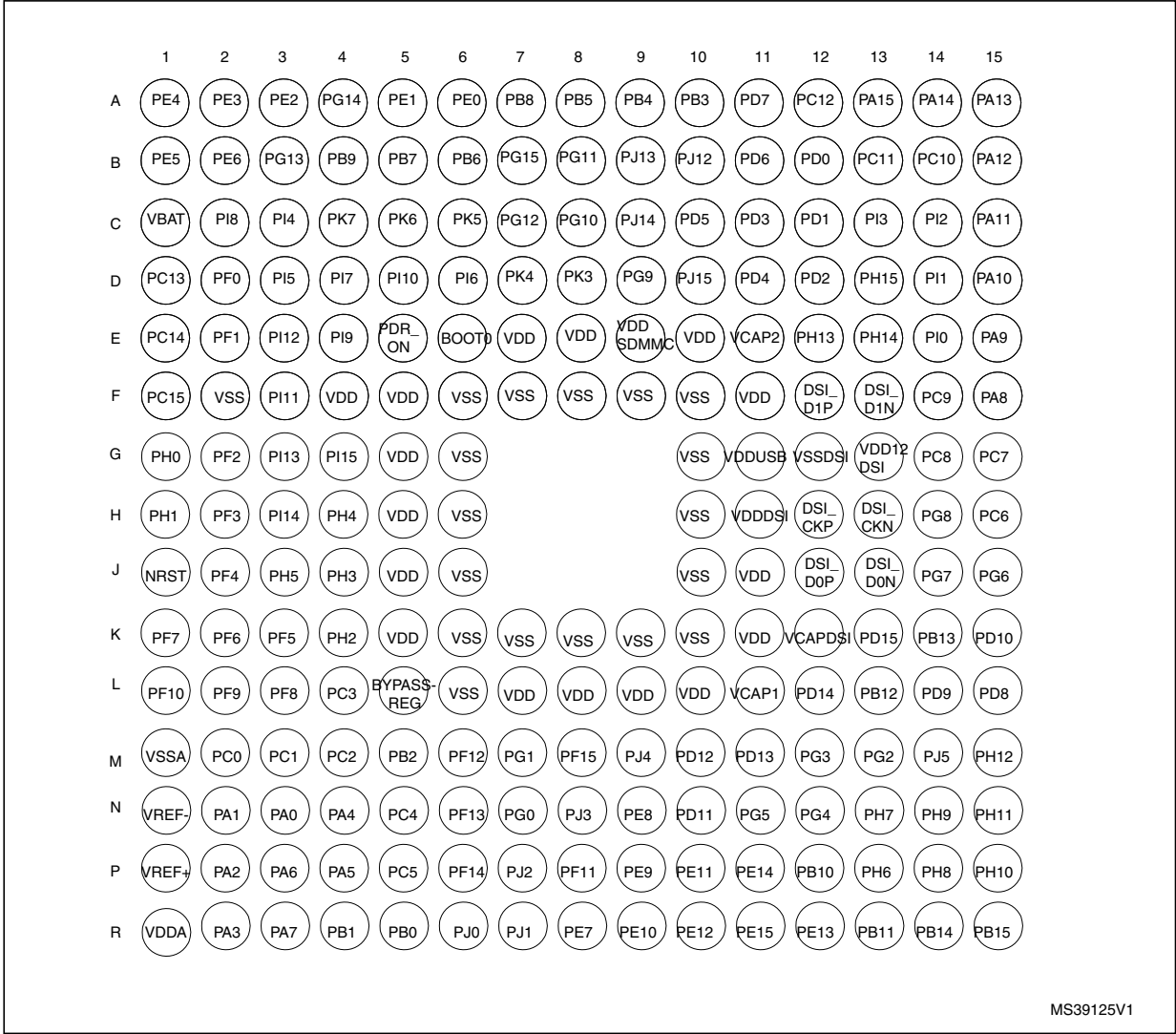
Figure 15. STM32F779Ax/STM32F778Ax WLCSP180 ballout



MSv39614V1

1. NC ball must not be connected to GND nor to VDD.
2. The above figure shows the package top view.

Figure 20. STM32F779xx TFBGA216 ballout



MS39125V1

1. The above figure shows the package top view.

Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F777xx						STM32F778Ax STM32F779xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 ⁽¹⁾	LQFP176	LQFP208	TFBGA216						
28	40	N4	50	53	N4	L9	50	53	N4	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC1_IN4, ADC2_IN4, DAC_OUT1
29	41	P4	51	54	P4	P11	51	54	P4	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC1_IN5, ADC2_IN5, DAC_OUT2
30	42	P3	52	55	P3	N10	52	55	P3	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, SPI6_MISO, TIM13_CH1, MDIOS_MDC, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC1_IN6, ADC2_IN6
31	43	R3	53	56	R3	M9	53	56	R3	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC1_IN7, ADC2_IN7
32	44	N5	54	57	N5	NC	54	57	N5	PC4	I/O	FT	-	DFSDM1_CKIN2, I2S1_MCK, SPDIF_RX2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC1_IN14, ADC2_IN14
33	45	P5	55	58	P5	NC	55	58	P5	PC5	I/O	FT	-	DFSDM1_DATIN2, SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC1_IN15, ADC2_IN15
-	-	-	-	59	L7	-	-	59	L7	VDD	S	-	-	-	-

Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F777xx						STM32F778Ax STM32F779xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 ⁽¹⁾	LQFP176	LQFP208	TFBGA216						
71	104	B15	123	146	B15	D1	127	146	B15	PA12	I/O	FT	-	TIM1_ETR, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	105	A15	124	147	A15	D2	128	147	A15	PA13(JT MS- SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	106	F13	125	148	E11	C1	129	148	E11	VCAP_2	S	-	-	-	-
74	107	F12	126	149	F10	C2	130	149	F10	VSS	S	-	-	-	-
75	108	G13	127	150	F11	B2	131	150	F11	VDD	S	-	-	-	-
-	-	E12	128	151	E12	F6	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	E13	129	152	E13	F7	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	D13	130	153	D13	E5	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	E14	131	154	E14	E4	132	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	D14	132	155	D14	B3	133	155	D14	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	C14	133	156	C14	C3	-	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

5.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in [Table 23](#). They are subject to general operating conditions for T_A .

Table 23. Over-drive switching characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	μs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 26: Current consumption measurement scheme](#).

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 34. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ		Max ⁽¹⁾						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
			IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD		
IDD12/ IDD	Supply current in RUN mode from V12 and V _{DD} supply	All Peripherals Enabled ⁽²⁾	180	102	1	114	2	148	2	168	2	mA
			168	91	1	101	2	132	2	152	2	
			144	71	1	78	2	105	2	122	2	
			60	32	1	37	2	64	2	81	2	
			25	16	1	20	2	46	2	64	2	
		All Peripherals Disabled	180	13	1	18	2	53	2	73	2	
			168	12	1	16	2	47	2	67	2	
			144	9	1	13	2	39	2	56	2	
			60	5	1	9	2	35	2	52	2	
			25	3	1	7	2	33	2	50	2	

1. Guaranteed by characterization results, unless otherwise specified.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

Table 35. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾				Unit
				V _{DD} = 3.6 V				
			T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C		
I _{DD_STOP_NM} (normal mode)	Supply current in Stop mode, main regulator in Run mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.55	3	18	27	mA	
		Flash memory in Deep power down mode, all oscillators OFF	0.5	3	18	27		
	Supply current in Stop mode, main regulator in Low-power mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.42	2.5	15	24		
		Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.37	2.5	15	24		
I _{DD_STOP_UDM} (under-drive mode)	Supply current in Stop mode, main regulator in Low voltage and under-drive modes	Regulator in Run mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.18	1.2	6	10		
		Regulator in Low-power mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.13	1.1	6	10		

1. Data based on characterization, tested in production.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 39: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

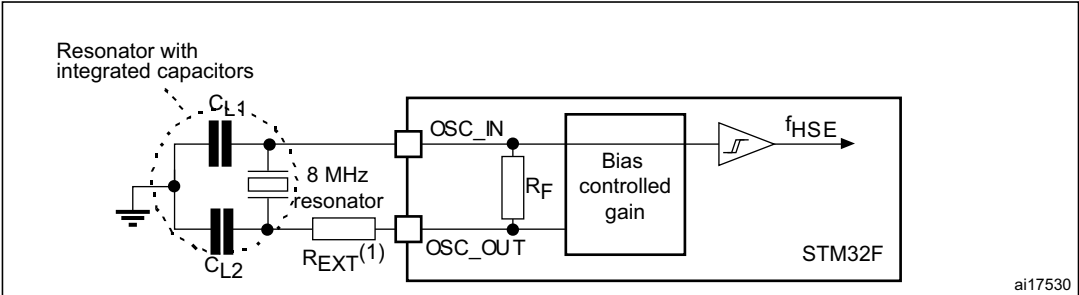
Table 38. Switching output I/O current consumption⁽¹⁾

Symbol	Parameter	Conditions	I/O toggling frequency (f _{sw}) MHz	Typ V _{DD} = 3.3 V	Typ V _{DD} = 1.8 V	Unit
I _{DDIO}	I/O switching Current	C _{EXT} = 0 pF C = C _{INT} + C _S + C _{EXT}	2	0.1	0.1	mA
			8	0.4	0.2	
			25	1.1	0.7	
			50	2.4	1.3	
			60	3.1	1.6	
			84	4.3	2.4	
			90	4.9	2.6	
			100	5.4	2.8	
		C _{EXT} = 10 pF C = C _{INT} + C _S + C _{EXT}	2	0.2	0.1	
			8	0.6	0.3	
			25	1.8	1.1	
			50	3.1	2.3	
			60	4.6	3.4	
			84	9.7	3.6	
			90	10.12	5.2	
			100	14.92	5.4	

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 30](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . The PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 30. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 44](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 44. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz) ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 Low drive capability	-	250	-	nA
		LSEDRV[1:0]=10 Medium low drive capability	-	300	-	
		LSEDRV[1:0]=01 Medium high drive capability	-	370	-	
		LSEDRV[1:0]=11 High drive capability	-	480	-	

5.3.21 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 65: I/O static characteristics](#)).

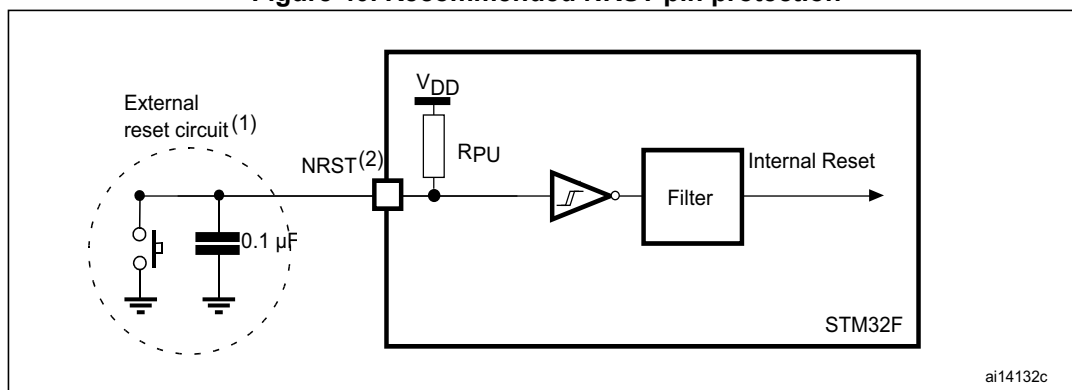
Unless otherwise specified, the parameters given in [Table 68](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 68. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
$V_{F(NRST)}^{(2)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(2)}$	NRST Input not filtered pulse	$V_{DD} > 2.7\text{ V}$	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	μs

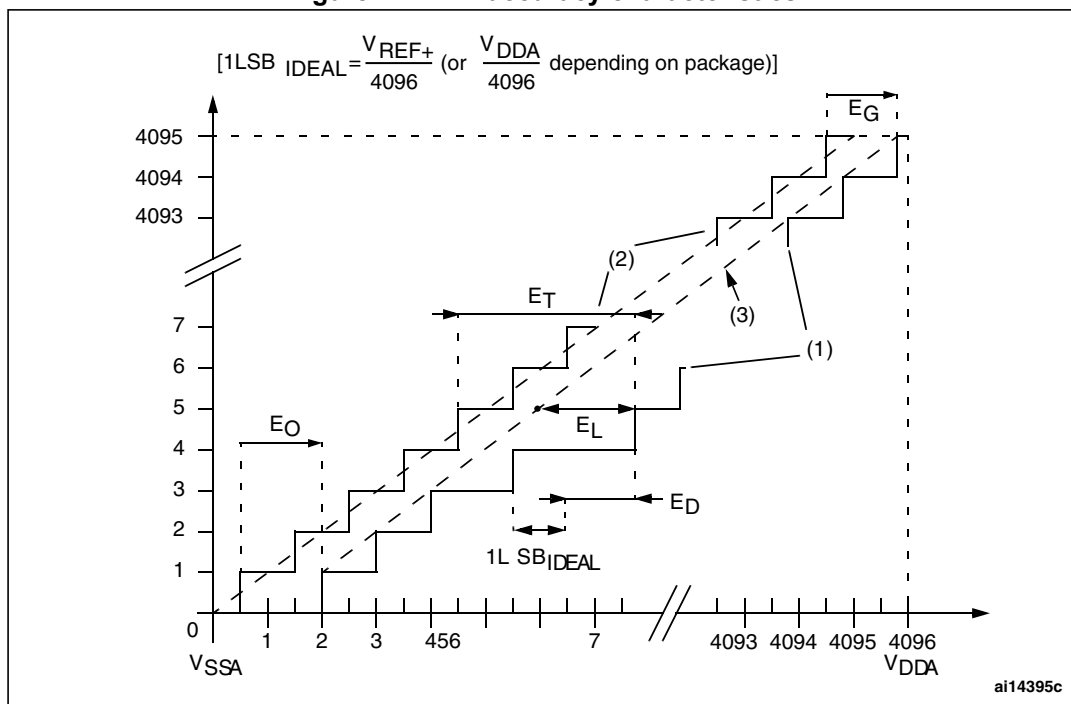
1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 40. Recommended NRST pin protection



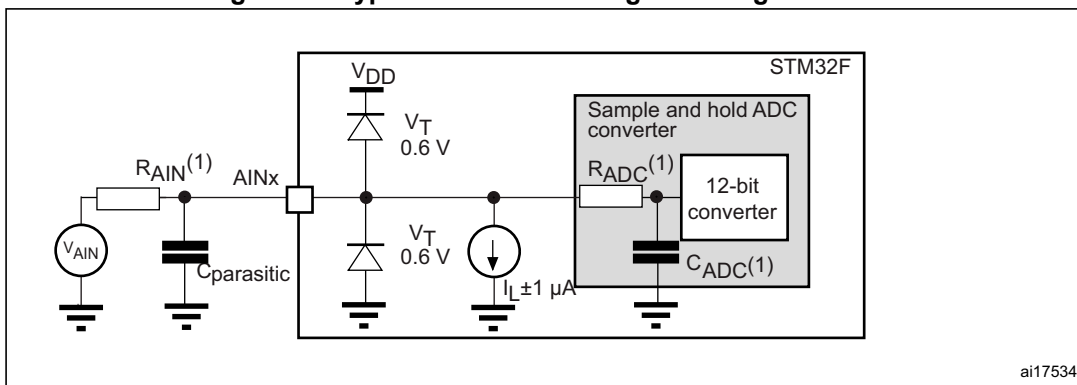
1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 68](#). Otherwise the reset is not taken into account by the device.

Figure 41. ADC accuracy characteristics



1. See also [Table 73](#).
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
 E_O = Offset Error: deviation between the first actual transition and the first ideal one.
 E_G = Gain Error: deviation between the last ideal transition and the last actual one.
 E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
 E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical connection diagram using the ADC



1. Refer to [Table 71](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

5.3.25 Temperature sensor characteristics

Table 77. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	-	2.5	-	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	-	0.76	-	V
$t_{START}^{(2)}$	Startup time	-	6	10	μs
$T_{S_temp}^{(2)}$	ADC sampling time when reading the temperature (1 $^{\circ}\text{C}$ accuracy)	10	-	-	μs

1. Guaranteed by characterization results.

2. Guaranteed by design.

Table 78. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 $^{\circ}\text{C}$, $V_{DDA} = 3.3\text{ V}$	0x1FF0 F44C - 0x1FF0 F44D
TS_CAL2	TS ADC raw data acquired at temperature of 110 $^{\circ}\text{C}$, $V_{DDA} = 3.3\text{ V}$	0x1FF0 F44E - 0x1FF0 F44F

5.3.26 V_{BAT} monitoring characteristics

Table 79. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	K Ω
Q	Ratio on V_{BAT} measurement	-	4	-	
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$T_{S_vbat}^{(2)(2)}$	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	μs

1. Guaranteed by design.

2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.27 Reference voltage

The parameters given in [Table 80](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 80. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.18	1.21	1.24	V
$T_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	10	-	-	μs
$V_{RERINT_s}^{(2)}$	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V} \pm 10\text{ mV}$	-	3	5	mV

I²S interface characteristics

Unless otherwise specified, the parameters given in [Table 86](#) for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5V_{DD}

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 86. I²S dynamic characteristics⁽¹⁾

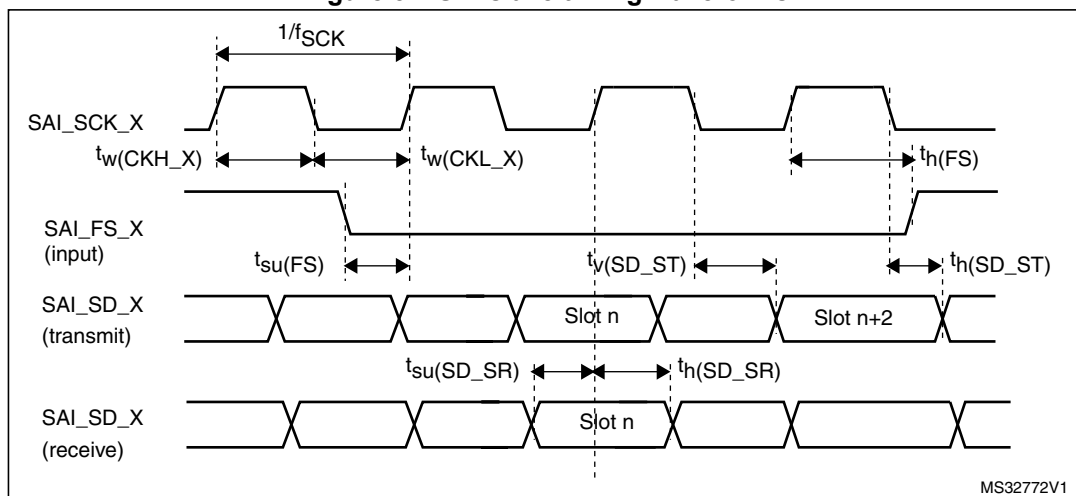
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256x F_S ⁽²⁾	MHz
f_{CK}	I2S clock frequency	Master data	-	64x F_S	MHz
		Slave data	-	64x F_S	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	5	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD_SR)}$		Slave receiver	2.5	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD_SR)}$		Slave receiver	2	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	12	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.

2. The maximum value of 256x F_S is 49.152 MHz (APB1 maximum frequency).

Note: Refer to RM0410 reference manual I2S section for more details about the sampling frequency (F_S). f_{MCK} , f_{CK} , and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of $(I2SDIV/(2*I2SDIV+ODD))$ and a maximum value of $(I2SDIV+ODD)/(2*I2SDIV+ODD)$. F_S maximum value is supported for each mode/condition.

Figure 54. SAI slave timing waveforms



USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 90. USB OTG full speed startup time

Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB OTG full speed transceiver startup time	1	μs

1. Guaranteed by design.

Table 91. USB OTG full speed DC electrical characteristics

Symbol	Parameter	Conditions	Min. (1)	Typ.	Max. (1)	Unit
Input levels	V_{DDUSB}	USB OTG full speed transceiver operating voltage	3.0 ⁽²⁾	-	3.6	V
	$V_{\text{DI}}^{(3)}$	Differential input sensitivity	0.2	-	-	V
	$V_{\text{CM}}^{(3)}$	Differential common mode range	0.8	-	2.5	
	$V_{\text{SE}}^{(3)}$	Single ended receiver threshold	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 k Ω to 3.6 V ⁽⁴⁾		0.3	V
	V_{OH}	Static output level high	R_L of 15 k Ω to V_{SS} ⁽⁴⁾		3.6	

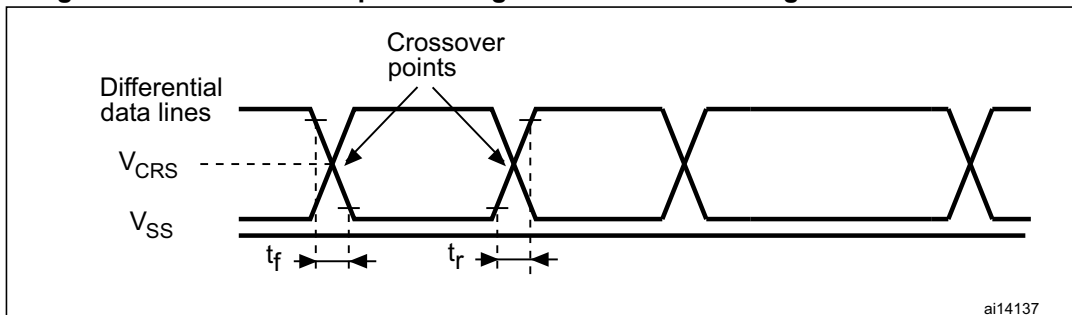
Table 91. USB OTG full speed DC electrical characteristics (continued)

Symbol	Parameter	Conditions	Min. (1)	Typ.	Max. (1)	Unit
R_{PD}	PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	k Ω
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		2.4	5.2	8	
R_{PU}	PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.55	0.95	1.35	

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DDUSB} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

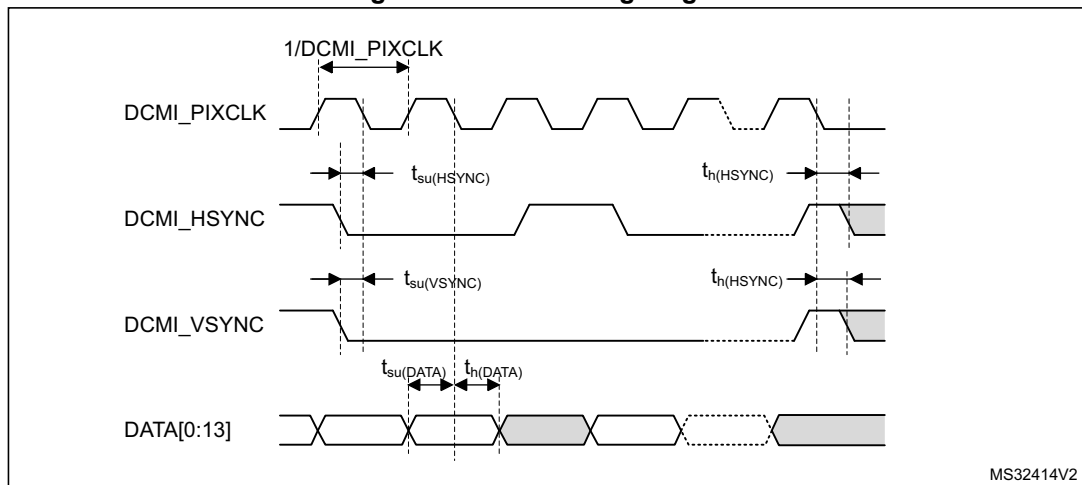
Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 μ A current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.

Figure 55. USB OTG full speed timings: definition of data signal rise and fall time

Table 92. USB OTG full speed electrical characteristics⁽¹⁾

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_f	Fall time ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V
Z_{DRV}	Output driver impedance ⁽³⁾	Driving high or low	28	44	Ω

Figure 77. DCMI timing diagram



5.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in [Table 121](#) for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 17](#), with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits

Table 121. LTDC characteristics ⁽¹⁾

Symbol	Parameter	Min	Max	Unit
f_{CLK}	LTDC clock output frequency	-	65	MHz
D_{CLK}	LTDC clock output duty cycle	45	55	%
$t_{w(\text{CLKH})}$, $t_{w(\text{CLKL})}$	Clock High time, low time	$t_w(\text{CLK})/2-0.5$	$t_w(\text{CLK})/2+0.5$	ns
$t_{v(\text{DATA})}$	Data output valid time	-	6	
$t_{h(\text{DATA})}$	Data output hold time	0	-	
$t_{v(\text{HSYNC})}$, $t_{v(\text{VSYNC})}$, $t_{v(\text{DE})}$	HSYNC/VSYNC/DE output valid time	-	3.5	
$t_{h(\text{HSYNC})}$, $t_{h(\text{VSYNC})}$, $t_{h(\text{DE})}$	HSYNC/VSYNC/DE output hold time	0.5	-	

1. Guaranteed by characterization results.

5.3.34 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in [Table 122](#) for DFSDM are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage summarized in [Table 17](#), with the following configuration:

- Output speed is set to $OSPEEDR[1:0] = 10$
- Capacitive load $C = 30\text{pF}$
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics (DFSDM1_CKINx, DFSDM1_DATINx, DFSDM1_CKOUT for DFSDM1).

Table 122. DFSDM measured timing 1.71-3.6V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	$1.71 < V_{DD} < 3.6 \text{ V}$	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.71 < V_{DD} < 3.6 \text{ V}$	-	-	20 ($f_{DFSDMCLK}/4$)	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $2.7 < V_{DD} < 3.6 \text{ V}$	-	-	20 ($f_{DFSDMCLK}/4$)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), $1.71 < V_{DD} < 3.6 \text{ V}$	-	-	20 ($f_{DFSDMCLK}/4$)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), $2.7 < V_{DD} < 3.6 \text{ V}$	-	-	20 ($f_{DFSDMCLK}/4$)	
f_{CKOUT}	Output clock frequency	$1.71 < V_{DD} < 3.6 \text{ V}$	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	$1.71 < V_{DD} < 3.6 \text{ V}$	45	50	55	%

Table 126. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 129. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b ⁽²⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	5.502	5.537	5.572	0.2166	0.2180	0.2194
E	6.060	6.095	6.130	0.2386	0.2400	0.2413
e	-	0.400	-	-	0.0157	-
e1	-	4.800	-	-	0.1890	-
e2	-	5.200	-	-	0.2047	-
F	-	0.368	-	-	0.0145	-
G	-	0.477	-	-	0.0188	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.