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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	132
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f779iit6

Table 2. STM32F777xx, STM32F778Ax and STM32F779xx features and peripheral counts

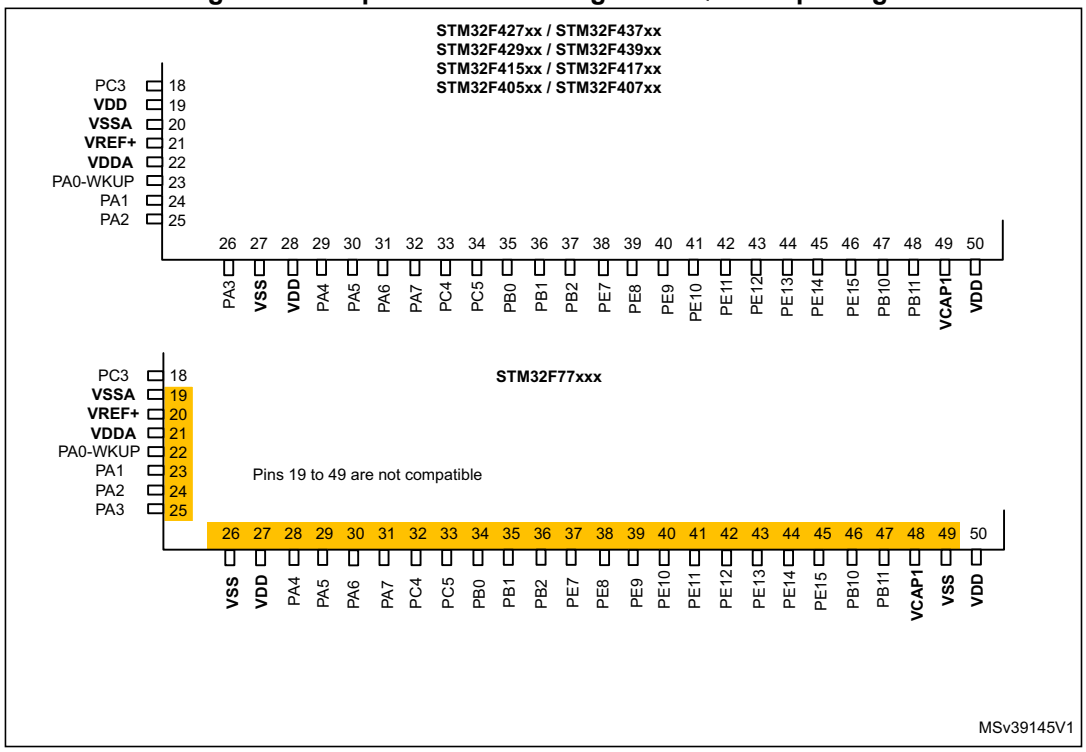
Peripherals		STM32F77xVx		STM32F77xZx		STM32F779Ax		STM32F778Ax	STM32F77xIx		STM32F77xBx		STM32F77xNx	
Flash memory in Kbytes		1024	2048	1024	2048	1024	2048	2048	1024	2048	1024	2048	1024	2048
SRAM in Kbytes	System	512(368+16+128)												
	Instruction	16												
	Backup	4												
FMC memory controller		Yes(1)												
Quad-SPI		Yes												
Ethernet		Yes				No			Yes					
Timers	General-purpose	10												
	Advanced-control	2												
	Basic	2												
	Low-power	1												
Random number generator		Yes												
Communication interfaces	SPI / I^2S	4/3 (simplex)(2)		6/3 (simplex)(2)										
	I^2C	4												
	USART/UART	4/4												
	USB OTG FS	Yes												
	USB OTG HS	Yes												
	CAN	3												
	SAI	2												
	SPDIFRX	4 inputs												
	SDMMC1	Yes												
	SDMMC2	Yes(3)												
Camera interface		Yes												
MIPI-DSI Host(4)		No				Yes								
LCD-TFT		Yes												
Chrom-ART Accelerator™ (DMA2D)		Yes												
JPEG codec		Yes												
Cryptography		Yes												

1.1 Full compatibility throughout the family

The STM32F777xx, STM32F778Ax and STM32F779xx devices are fully pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

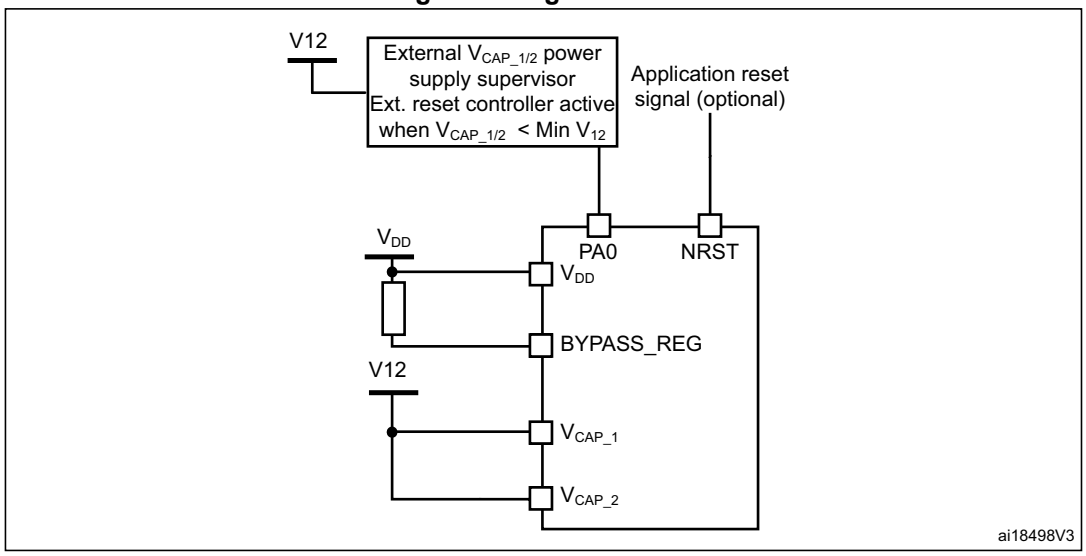
Figure 1 gives compatible board designs between the STM32F7xx and STM32F4xx families.

Figure 1. Compatible board design for LQFP100 package



The STM32F77x LQFP144, LQFP176, LQFP208, TFBGA216, UFBGA176 packages are fully pin to pin compatible with STM32F4xx devices.

Figure 8. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	108	216
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	108	216
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	108	216
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	54	108/216
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	54	108/216
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	54	108/216

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2.48 DSI Host (DSIHOST)

The DSI Host is a dedicated peripheral for interfacing with MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

These interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI).
  - Through a customized for mode, this interface can be used to transmit information in full bandwidth in the Adapted Command mode (DBI).
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface.
  - Can operate concurrently with either LTDC interface in either Video mode or Adapted Command mode.
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli.

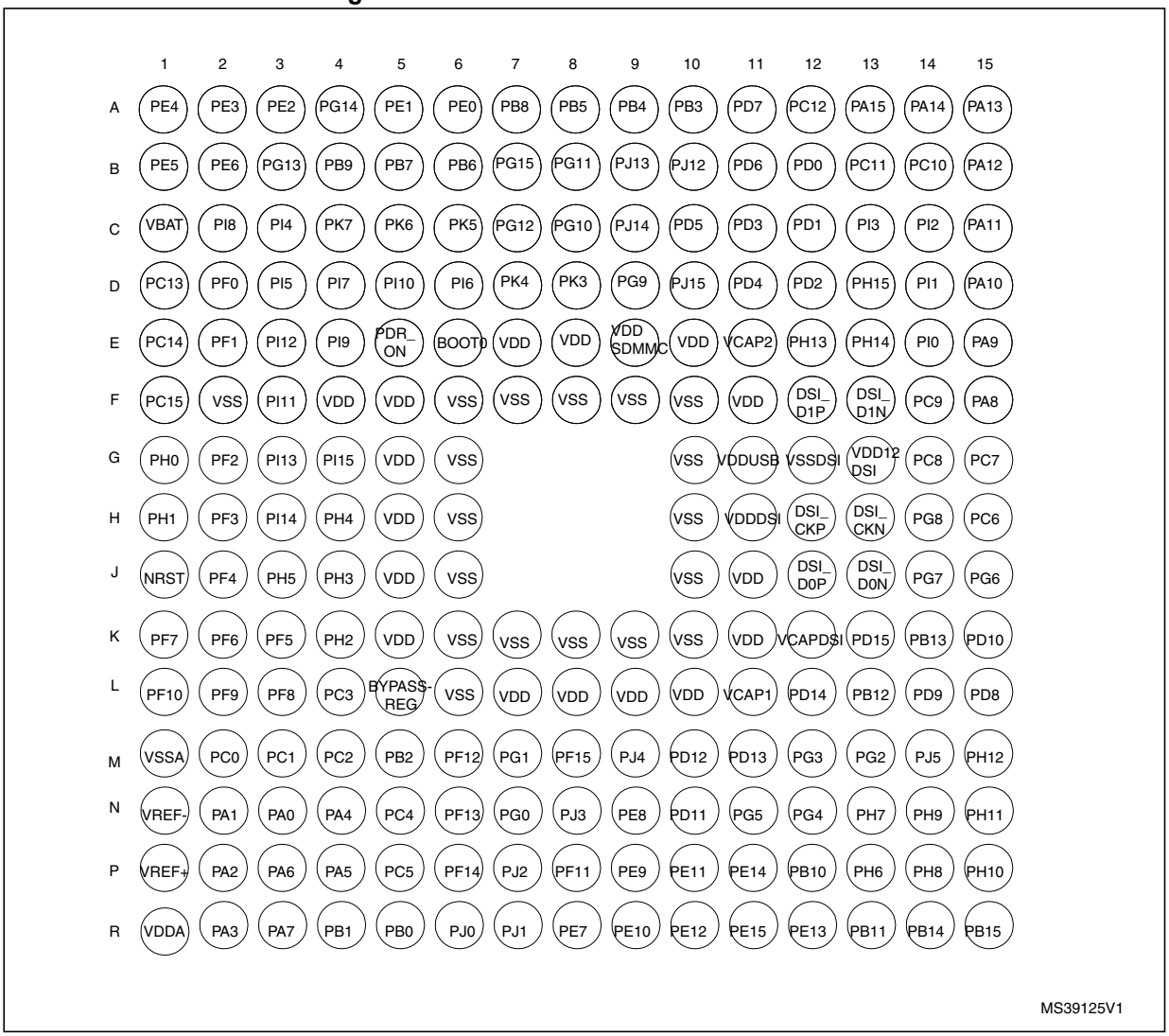
The DSI Host main features:

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS:
  - Transmission of all Command mode packets through the APB interface
  - Transmission of commands in low-power and high-speed during Video mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-power mode with PLL disabled
- ECC and Checksum capabilities
- Support for End of Transmission Packet (EoTp)
- Fault recovery schemes
- 3D transmission support
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for Generic and DCS commands
  - Video Mode interface through LTDC
  - Adapted Command mode interface through LTDC
- Independently programmable Virtual Channel ID in
  - Video mode
  - Adapted Command mode
  - APB Slave

Video Mode interfaces features:

- LTDC interface color coding mappings into 24-bit interface:

Figure 20. STM32F779xx TFBGA216 ballout



1. The above figure shows the package top view.

Table 10. STM32F777xx, STM32F778Ax and STM32F779xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F777xx						STM32F778Ax STM32F779xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
40	63	R9	73	84	R9	J6	73	84	R9	PE10	I/O	FT	-	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-
41	64	P10	74	85	P10	K6	74	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, DFSDM1_CKIN4, SAI2_SD_B, FMC_D8, LCD_G3, EVENTOUT	-
42	65	R10	75	86	R10	L6	75	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, DFSDM1_DATIN5, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT	-
43	66	N11	76	87	R12	P6	76	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, DFSDM1_CKIN5, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT	-
44	67	P11	77	88	P11	N6	77	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11, LCD_CLK, EVENTOUT	-
45	68	R11	78	89	R11	M6	78	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
46	69	R12	79	90	P12	K5	79	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-

1. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid an extra current consumption in low-power modes. list of pins: PI8, PI12, PI13, PI14, PF6, PF7, PF8, PF9, PC2, PC3, PC4, PC5, PI15, PJ0, PJ1, PJ2, PJ3, PJ4, PJ5, PH6, PH7, PJ12, PJ13, PJ14, PJ15, PG14, PK3, PK4, PK5, PK6 and PK7.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: - The speed should not exceed 2 MHz with a maximum load of 30 pF. - These I/Os must not be used as a current source (e.g. to drive an LED).
3. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
4. If the device is in regulator OFF/internal reset ON mode (BYPASS_REG pin is set to VDD), then PA0 is used as an internal reset (active low).
5. Internally connected to VDD or VSS depending on part number.

Table 12. STM32F777xx, STM32F778Ax and STM32F779xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	SAI2_SD_B	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	SAI2_SCK_B	-	-	ETH_MDIO	MDIOS_MDIO	-	LCD_R1	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	SPI6_MISO	TIM13_CH1	-	-	MDIOS_MDC	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SD	-	-	SPI6_MOSI	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	CAN3_RX	UART7_RX	LCD_B3	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	DCMI_D0	LCD_R5	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	LCD_B4	OTG_FS_ID	-	MDIOS_MDIO	DCMI_D1	LCD_B1	EVENTOUT

Table 12. STM32F777xx, STM32F778Ax and STM32F779xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port E	PE4	TRACED1	-	-	-	-	SPI4_NSS	SAI1_FS_A	-	-	-	DFSDM1_DATAIN3	-	FMC_A20	DCMI_D4	LCD_B0	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SAI1_SCK_A	-	-	-	DFSDM1_CKIN3	-	FMC_A21	DCMI_D6	LCD_G0	EVENTOUT
	PE6	TRACED3	TIM1_BKIN2	-	TIM9_CH2	-	SPI4_MOSI	SAI1_SD_A	-	-	-	SAI2_MCK_B	-	FMC_A22	DCMI_D7	LCD_G1	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_DATAIN2	-	UART7_Rx	-	QUADSPI_BK2_IO0	-	FMC_D4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-	UART7_Tx	-	QUADSPI_BK2_IO1	-	FMC_D5	-	-	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_CKOUT	-	UART7_RTS	-	QUADSPI_BK2_IO2	-	FMC_D6	-	-	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM1_DATAIN4	-	UART7_CTS	-	QUADSPI_BK2_IO3	-	FMC_D7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	DFSDM1_CKIN4	-	-	-	SAI2_SD_B	-	FMC_D8	-	LCD_G3	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	DFSDM1_DATAIN5	-	-	-	SAI2_SCK_B	-	FMC_D9	-	LCD_B4	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	DFSDM1_CKIN5	-	-	-	SAI2_FS_B	-	FMC_D10	-	LCD_DE	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCK_B	-	FMC_D11	-	LCD_CLK	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FMC_D12	-	LCD_R7	EVENTOUT

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 18: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq$ 144 MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq$ 168 MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq$ 216 MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 17: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V $\leq V_{DD} \leq$ 3.6 V voltage range and for T_A= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V $\leq V_{DD} \leq$ 3.6 V voltage range and a maximum ambient temperature (T_A) unless otherwise specified.
- For the voltage range 1.7 V $\leq V_{DD} \leq$ 3.6 V, the maximum frequency is 180 MHz.

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	193	221(4)	258(4)	-	mA
			200	179	207	244	279	
			180	159	176(4)	210(4)	238(4)	
			168	142	156	187	211	
			144	122	135	167	190	
			60	49	55	81	103	
			25	23	28	54	76	
		All peripherals disabled(3)	216	95	107(4)	153(4)	-	
			200	88	100	146	180	
			180	78	88(4)	122(4)	147(4)	
			168	70	78	109	133	
			144	60	68	99	123	
			60	24	29	55	76	
			25	12	16	42	63	

1. Guaranteed by characterization results, unless otherwise specified.

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 108 MHz)	TIM1	24.1	23.8	19.6	µA/MHz
	TIM8	24.5	24.2	20.0	
	USART1	17.7	17.4	14.3	
	USART6	11.9	11.8	9.4	
	ADC1(5)	4.5	4.7	3.5	
	ADC2(5)	4.5	4.7	3.3	
	ADC3(5)	4.5	4.6	3.3	
	SDMMC1	8.4	8.3	6.9	
	SDMMC2	8.2	8.2	6.4	
	SPI1/I2S1(3)	3.9	3.6	3.1	
	SPI4	3.9	3.6	3.1	
	SYSCFG	2.5	2.2	1.9	
	TIM9	8.0	8.0	6.2	
	TIM10	5.0	5.1	3.7	
	TIM11	6.9	6.9	5.3	
	SPI5	2.7	2.8	1.8	
	SPI6	3.1	3.2	2.2	
	SAI1	3.2	3.3	2.2	
	DFSDM1	10.9	10.7	9.0	
	SAI2	3.9	3.9	2.8	
	MDIO	7.1	7.0	5.8	
	LTDC	51.2	50.3	41.8	
	DSI	8.5	8.4	8.1	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.75 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 48. PLLI2S characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-		0.95(2)	1	2.10	MHz
$f_{PLLI2SP\_OUT}$	PLLI2S multiplier output clock for SPDIFRX	-		-	-	216	
$f_{PLLI2SQ\_OUT}$	PLLI2S multiplier output clock for SAI	-		-	-	216	
$f_{PLLI2SR\_OUT}$	PLLI2S multiplier output clock for I2S	-		-	-	216	
f_{VCO_OUT}	PLLI2S VCO output	-		100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 192 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 49. PLLISAI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock(1)	-	0.95(2)	1	2.10	MHz
$f_{PLLSAIP\_OUT}$	PLLSAI multiplier output clock for 48 MHz	-	-	48	75	
$f_{PLLSAIQ\_OUT}$	PLLSAI multiplier output clock for SAI	-	-	-	216	
$f_{PLLSAIR\_OUT}$	PLLSAI multiplier output clock for LCD-TFT	-	-	-	216	
f_{VCO_OUT}	PLLSAI VCO output	-	100	-	432	

Table 66. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	CMOS port(2) I_{IO} = -8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	
V_{OH}(3)	Output high level voltage for PC14	CMOS port(2) I_{IO} = -2 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4		
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+8mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin except PC14	TTL port(2) I_{IO} =-8mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}−1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤ V_{DD} ≤ 3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -6 mA 1.8 V ≤ V_{DD} ≤ 3.6 V	V_{DD}−0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤ V_{DD} ≤ 3.6V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -4 mA 1.7 V ≤ V_{DD} ≤ 3.6V	V_{DD}−0.4(5)	-	
V_{OH}(3)	Output high level voltage for PC14	I_{IO} = -1 mA 1.7 V ≤ V_{DD} ≤ 3.6V	V_{DD}−0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 67*, respectively.

Table 80. internal reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 81. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FF0 F44A - 0x1FF0 F44B

5.3.28 DAC electrical characteristics

Table 82. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.7(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.7(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs

Figure 69. NAND controller waveforms for read access

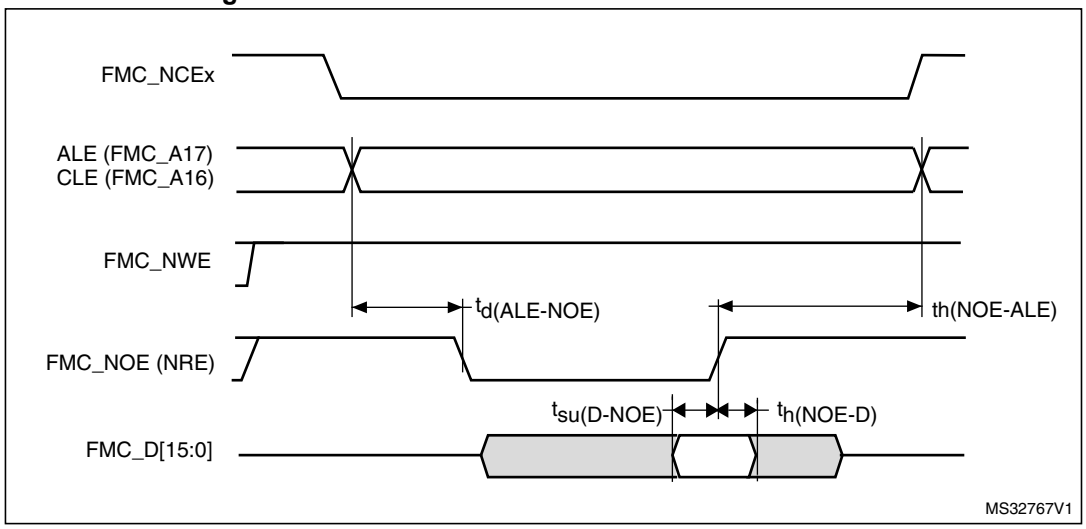


Figure 70. NAND controller waveforms for write access

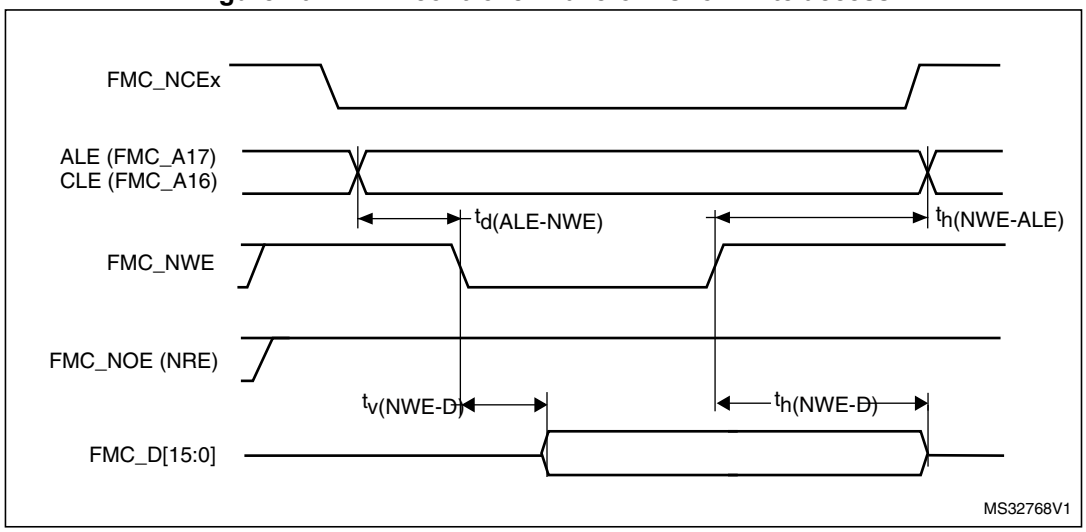


Figure 75. Quad-SPI timing diagram - SDR mode

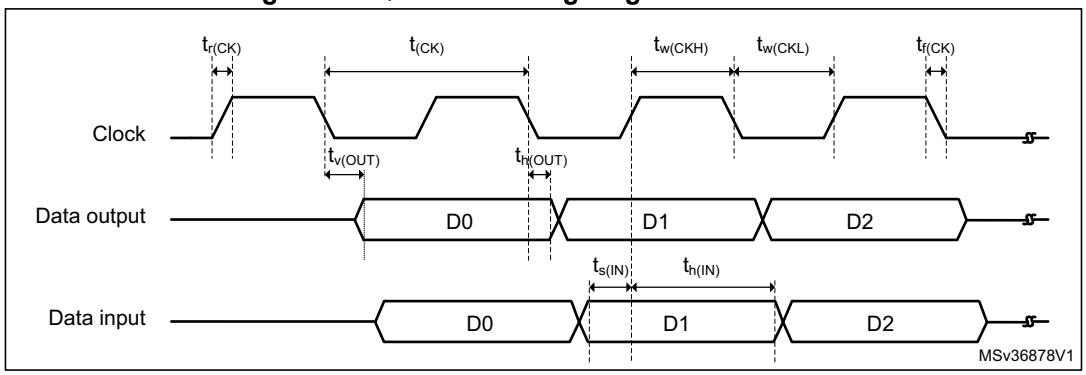
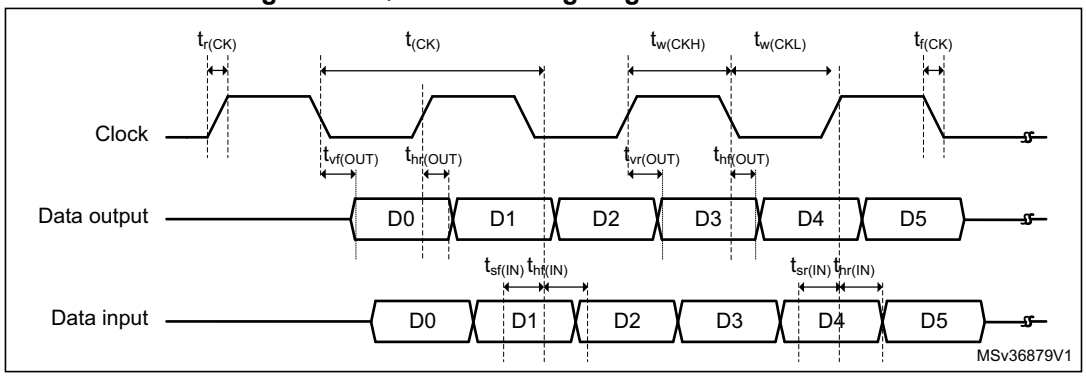


Figure 76. Quad-SPI timing diagram - DDR mode



5.3.32 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 120* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 120. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2	-	ns
$t_{h(DATA)}$	Data input hold time	0.5	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	2.5	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	3	-	

1. Guaranteed by characterization results.

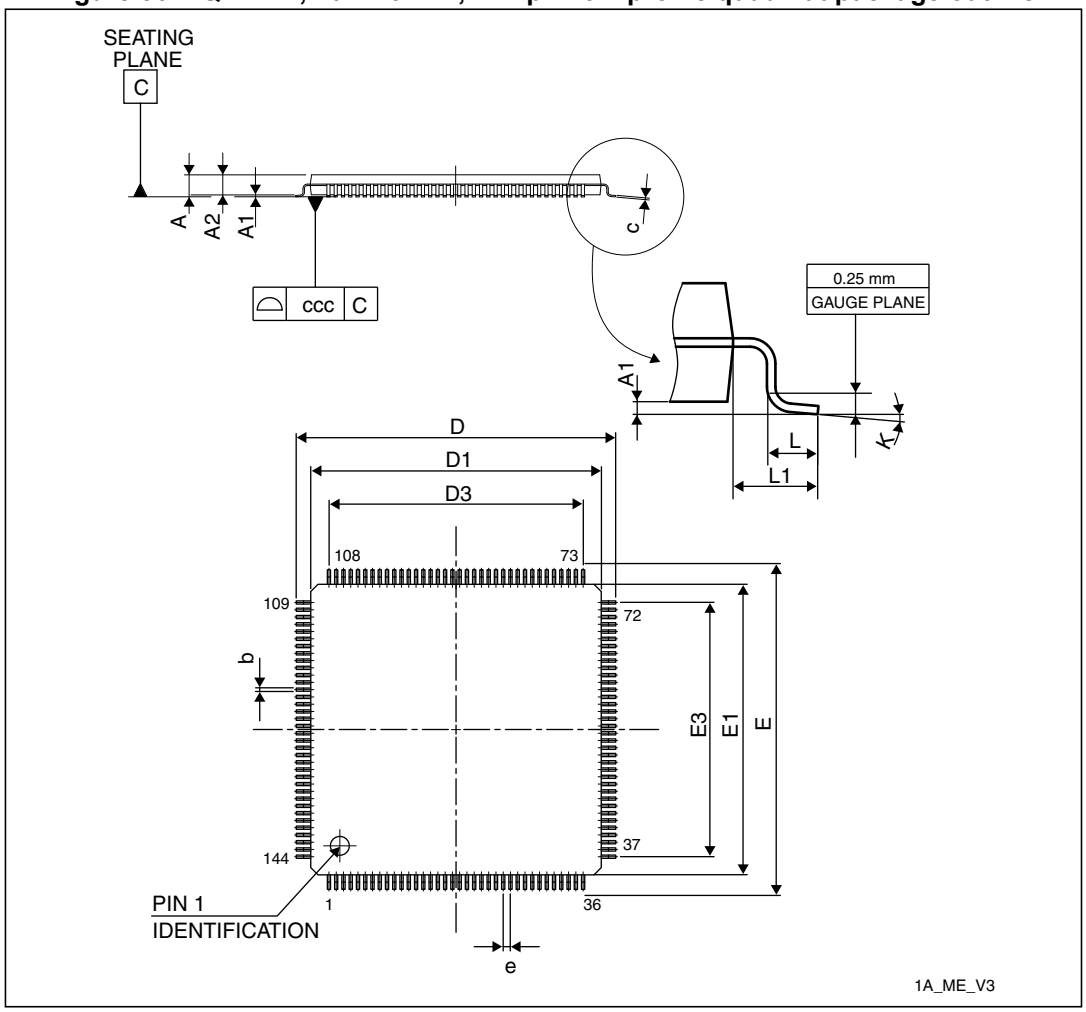
Table 125. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

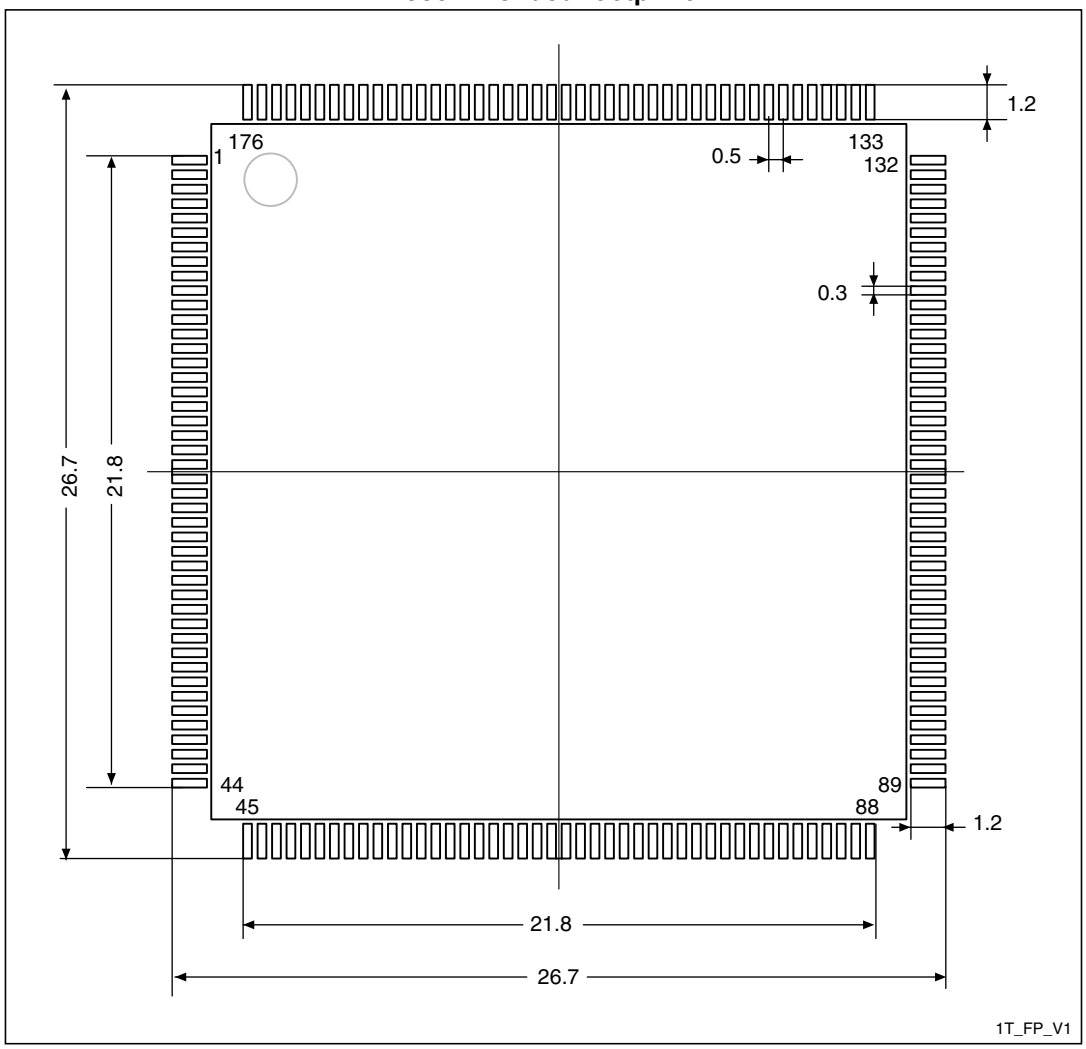
6.2 LQFP144 20 x 20 mm, low-profile quad flat package information

Figure 86. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

Figure 90. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.