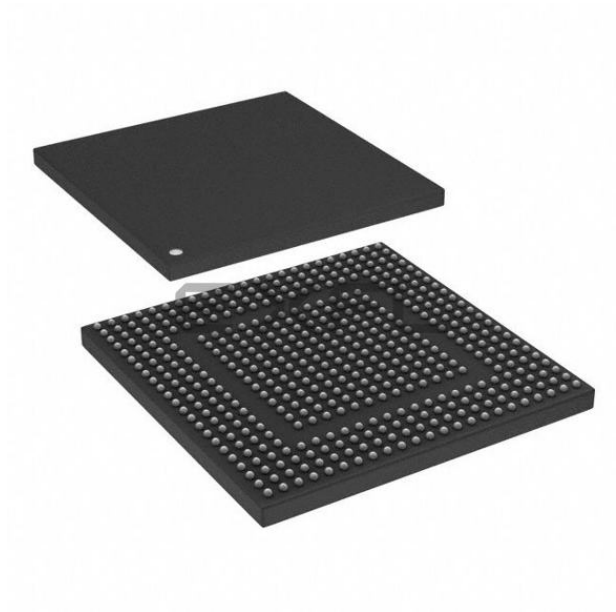

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8308cvmadd

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit
SerDes internal digital power	$XCOREV_{DD}$	1.0 V ± 50 mV	V
SerDes internal digital power	$XCOREV_{SS}$	0.0	V
SerDes I/O digital power	$XPADV_{DD}$	1.0 V ± 50 mV	V
SerDes analog power for PLL	$SDAV_{DD}$	1.0 V ± 50 mV	V
SerDes analog power for PLL	$SDAV_{SS}$	0	V
SerDes I/O digital power	$XPADV_{SS}$	0	V
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V
Analog supply for e300 core APLL[2]	AV_{DD1}	1.0 V ± 50 mV	V
Analog supply for system APLL[2]	AV_{DD2}	1.0 V ± 50 mV	V
DDR2 DRAM I/O voltage	GV_{DD}	1.8 V ± 100 mV	V
Differential reference voltage for DDR controller	MV_{REF}	GVDD/2 ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$)	V
Standard I/O voltage (Local bus, DUART, system control and power management, eSDHC, USB, I^2C, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage)[3]	NV_{DD}	3.3 V ± 300 mV	V
eTSEC IO supply[4,5]	LV_{DD1}, LV_{DD2}	2.5 V ± 125 mV 3.3 V ± 300 mV	V
Analog and digital ground	V_{SS}	0.0	V
Operating temperature range[6]	T_A/T_J	Standard = 0 to 105 Extended = -40 to 105	°C

Notes:

1. GV_{DD}, NV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. This voltage is the input to the filter discussed in Section 23.2, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. NV_{DD} here refers to NV_{DDA}, NV_{DDB},NV_{DDG}, NV_{DDH}, NV_{DDJ} and NV_{DDP_K} from the ball map.
4. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
5. LV_{DD1} here refers to NV_{DDC} and LV_{DD2} refers to NV_{DDF} from the ball map.
6. Minimum temperature is specified with T_A; Maximum temperature is specified with T_J.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8308 Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	NV_{DD} (3.3 V)	LV_{DD}/ (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR2 R_S = 22 Ω R_t = 75 Ω	250 MHz 32 bits+ECC 266 MHz 32 bits+ECC	0.302 0.309	—	—	—	W	—
Local bus I/O load = 20 pF	62.5 MHz 66 MHZ	—	0.038 0.040	—	—	W	—
TSEC I/O load = 20 pF	MII, 25 MHz	—	—	0.008	—	W	2 controllers
	RGMII, 125 MHz	—	—	0.078	0.044	W	
eSDHC IO Load = 40 pF	50 MHz	—	—	0.008	—	W	—
USB IO Load = 20 pF	60 MHz	—	—	0.012		W	—
Other I/O	—	—	0.017	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN) DC electrical specifications for the device.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V $\le V_{IN} \le NV_{DD}$	I_{IN}	—	±10	μA

This table provides the RTC clock input (RTC_PIT_CLOCK) DC electrical specifications for the device.

Table 7. RTC_PIT_CLOCK DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	3.3 V – 400 mV		V
Input low voltage	—	V_{IL}	0	0.4	V

4.2 AC Electrical Characteristics

The primary clock source for the device is SYS_CLK_IN. This table provides the system clock input (SYS_CLK_IN) AC timing specifications for the device.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.45	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.45	—	V	—

This table provides input AC timing specifications for the DDR2 SDRAM interface.

Table 17. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 1.8± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC 266 MHz	t_{CISKEW}	–875	875	ps	1, 2,3

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ or MECC signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = +/–(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Memory controller ODT value of 150 Ω is recommended

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ//MDM/MECC output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}		—	ps	5
266 MHz		900			
MDQ//MDM/MECC output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}		—	ps	5
266 MHz		1100			
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Table 22. RGMII DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD}= Min	VSS – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DD}		—	15	μA
Input low current	I_{IL}	V_{IN} [1] = VSS		–15	—	μA

Note:
1. V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 MII and RGMII AC Timing Specifications

The AC timing specifications for MII and RGMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 28. GPIO DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NVDD$	—	± 5	μA

8.4.2 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

Table 29. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	—
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Note:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9 USB

9.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

9.1.1 USB DC Electrical Characteristics

This table lists the DC electrical characteristics for the USB interface.

Table 30. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LVDD + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	LVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

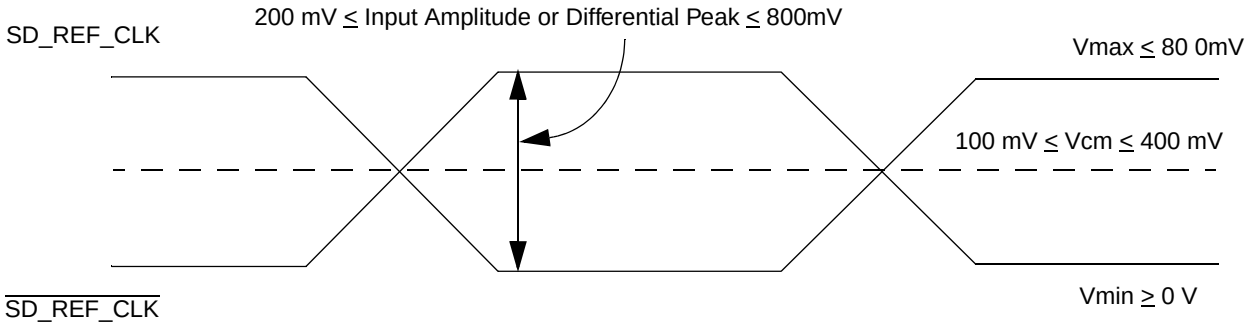

Figure 17. Differential Reference Clock Input DC Requirements (External DC-Coupled)

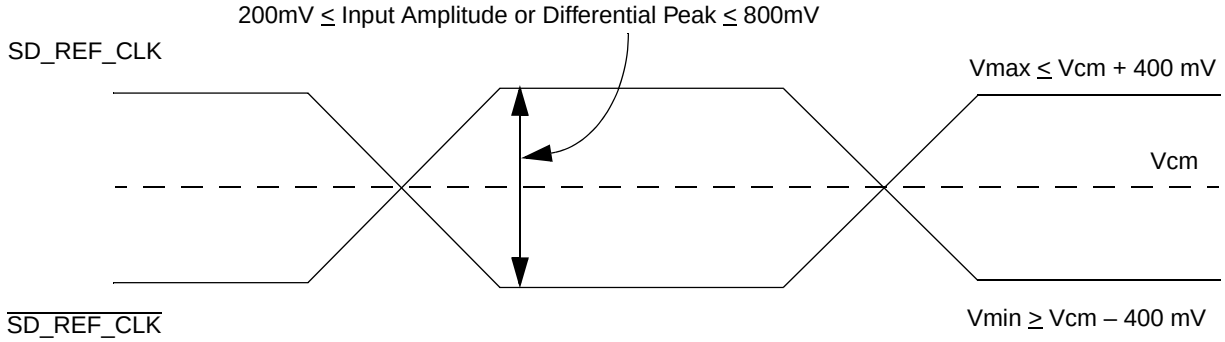

Figure 18. Differential Reference Clock Input DC Requirements (External AC-Coupled)

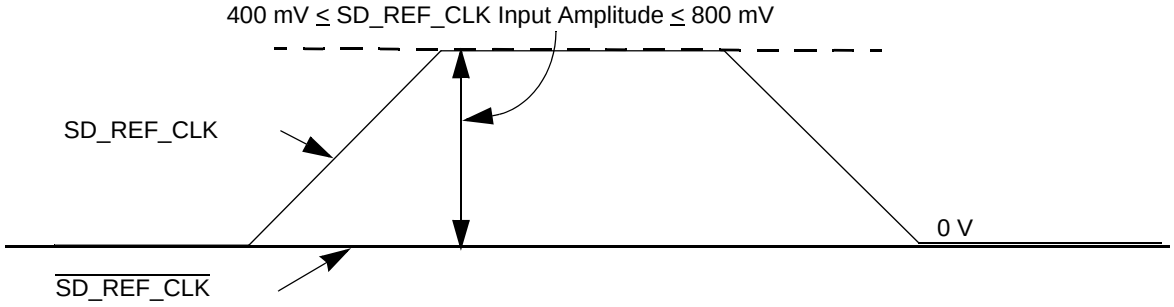

Figure 19. Single-Ended Reference Clock Input DC Requirements

10.2.3 Interfacing with Other Differential Signaling Levels

With on-chip termination to XCOREVSS, the differential reference clocks inputs are high-speed current steering logic (HCSL) compatible and DC coupled.

Many other low voltage differential type outputs like low-voltage differential signaling (LVDS) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100–400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

Table 32. SerDes Reference Clock AC Parameters (continued)

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
Rising edge rate (SD_REF_CLK) to falling edge rate ($\overline{\text{SD\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing (Figure 24).
4. Matching applies to rising edge rate for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate (See Figure 25).

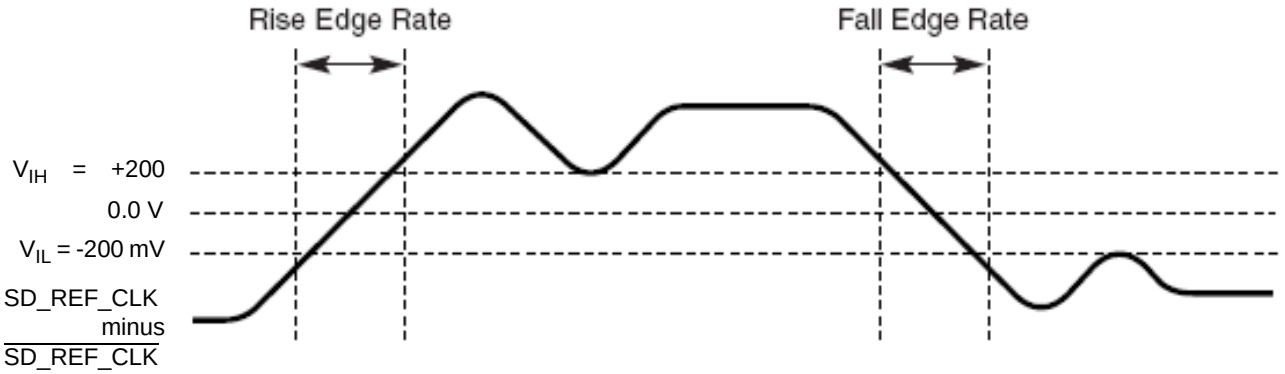

Figure 24. Differential Measurement Points for Rise and Fall Time

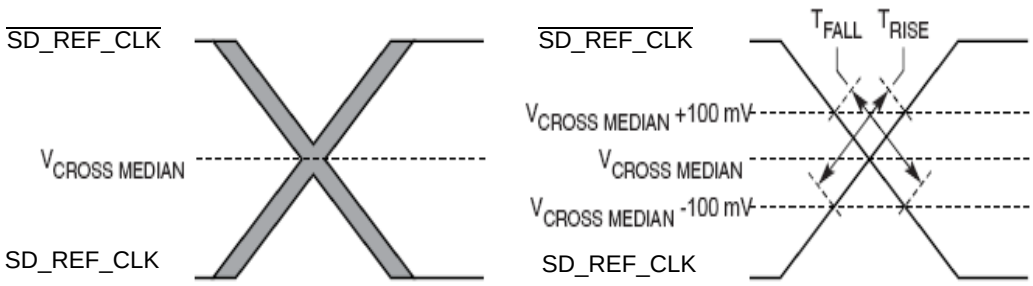

Figure 25. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. For detailed information, see the following sections:

- Section 11.2, “AC Requirements for PCI Express SerDes Clocks”

15 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

15.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 43. I²C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times NV_{DD}$	$NV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times NV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times NV_{DD}$	V	1
High level output voltage	V_{OH}	$0.8 \times NV_{DD}$	$NV_{DD} + 0.3$	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current, ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	μA	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. For information on the digital filter used, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

15.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface.

Table 44. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	μs
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns

16 Timers

This section describes the DC and AC electrical specifications for the timers.

16.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8308 timers pins, including TIN, $\overline{\text{TOUT}}$, and $\overline{\text{TGATE}}$.

Table 45. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

16.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 46. Timers Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the Timers.

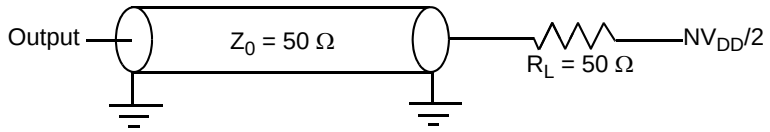

Figure 47. Timers AC Test Load

2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

20.3 Pinout Listings

This table provides the pin-out listing for the MPC8308, MAPBGA package.

Table 53. MPC8308 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	V6	I/O	GV_{DDA}	—
MEMC_MDQ[1]	Y4	I/O	GV_{DDA}	—
MEMC_MDQ[2]	AB3	I/O	GV_{DDA}	—
MEMC_MDQ[3]	AA3	I/O	GV_{DDA}	—
MEMC_MDQ[4]	AA2	I/O	GV_{DDA}	—
MEMC_MDQ[5]	AA1	I/O	GV_{DDA}	—
MEMC_MDQ[6]	W4	I/O	GV_{DDA}	—
MEMC_MDQ[7]	Y2	I/O	GV_{DDA}	—
MEMC_MDQ[8]	W3	I/O	GV_{DDA}	—
MEMC_MDQ[9]	W1	I/O	GV_{DDA}	—
MEMC_MDQ[10]	Y1	I/O	GV_{DDA}	—
MEMC_MDQ[11]	W2	I/O	GV_{DDA}	—
MEMC_MDQ[12]	U4	I/O	GV_{DDA}	—
MEMC_MDQ[13]	U3	I/O	GV_{DDA}	—
MEMC_MDQ[14]	V4	I/O	GV_{DDA}	—
MEMC_MDQ[15]	U6	I/O	GV_{DDA}	—
MEMC_MDQ[16]	T3	I/O	GV_{DDB}	—
MEMC_MDQ[17]	T2	I/O	GV_{DDB}	—
MEMC_MDQ[18]	R4	I/O	GV_{DDB}	—
MEMC_MDQ[19]	R3	I/O	GV_{DDB}	—
MEMC_MDQ[20]	P4	I/O	GV_{DDB}	—
MEMC_MDQ[21]	N6	I/O	GV_{DDB}	—
MEMC_MDQ[22]	P2	I/O	GV_{DDB}	—
MEMC_MDQ[23]	P1	I/O	GV_{DDB}	—
MEMC_MDQ[24]	N4	I/O	GV_{DDB}	—
MEMC_MDQ[25]	N3	I/O	GV_{DDB}	—
MEMC_MDQ[26]	N2	I/O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDQ[27]	M6	I/O	GV_{DDB}	—
MEMC_MDQ[28]	M2	I/O	GV_{DDB}	—
MEMC_MDQ[29]	M3	I/O	GV_{DDB}	—
MEMC_MDQ[30]	L2	I/O	GV_{DDB}	—
MEMC_MDQ[31]	L3	I/O	GV_{DDB}	—
MEMC_MDM[0]	AB2	O	GV_{DDA}	—
MEMC_MDM[1]	V3	O	GV_{DDA}	—
MEMC_MDM[2]	P3	O	GV_{DDB}	—
MEMC_MDM[3]	M7	O	GV_{DDB}	—
MEMC_MDM[8]	K2	O	GV_{DDB}	—
MEMC_MDQS[0]	AC3	I/O	GV_{DDA}	—
MEMC_MDQS[1]	V1	I/O	GV_{DDA}	—
MEMC_MDQS[2]	R1	I/O	GV_{DDB}	—
MEMC_MDQS[3]	M1	I/O	GV_{DDB}	—
MEMC_MDQS[8]	K1	I/O	GV_{DDB}	—
MEMC_MBA[0]	C3	O	GV_{DDB}	—
MEMC_MBA[1]	B2	O	GV_{DDB}	—
MEMC_MBA[2]	H4	O	GV_{DDB}	—
MEMC_MA0	C2	O	GV_{DDB}	—
MEMC_MA1	D2	O	GV_{DDB}	—
MEMC_MA2	D3	O	GV_{DDB}	—
MEMC_MA3	D4	O	GV_{DDB}	—
MEMC_MA4	E4	O	GV_{DDB}	—
MEMC_MA5	F4	O	GV_{DDB}	—
MEMC_MA6	E2	O	GV_{DDB}	—
MEMC_MA7	E1	O	GV_{DDB}	—
MEMC_MA8	F2	O	GV_{DDB}	—
MEMC_MA9	F3	O	GV_{DDB}	—
MEMC_MA10	C1	O	GV_{DDB}	—
MEMC_MA11	F7	O	GV_{DDB}	—
MEMC_MA12	G2	O	GV_{DDB}	—
MEMC_MA13	G3	O	GV_{DDB}	—
$\overline{\text{MEMC\_MWE}}$	D5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MRAS}}$	B4	O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MEMC\_MCAS}}$	C5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCS}}$[0]	B6	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCS}}$[1]	C6	O	GV_{DDB}	—
MEMC_MCKE	H3	O	GV_{DDB}	3
MEMC_MCK [0]	A3	O	GV_{DDB}	—
MEMC_MCK [1]	U2	O	GV_{DDB}	—
MEMC_MCK [2]	G1	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [0]	A4	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [1]	U1	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [2]	H1	O	GV_{DDB}	—
MEMC_MODT[0]	A5	O	GV_{DDB}	—
MEMC_MODT[1]	B5	O	GV_{DDB}	—
MEMC_MECC[0]	L4	I/O	GV_{DDB}	—
MEMC_MECC[1]	L6	I/O	GV_{DDB}	—
MEMC_MECC[2]	K4	I/O	GV_{DDB}	—
MEMC_MECC[3]	K3	I/O	GV_{DDB}	—
MEMC_MECC[4]	J2	I/O	GV_{DDB}	—
MEMC_MECC[5]	K6	I/O	GV_{DDB}	—
MEMC_MECC[6]	J3	I/O	GV_{DDB}	—
MEMC_MECC[7]	J6	I/O	GV_{DDB}	—
MV_{REF}	G6	I	GV_{DDB}	—
Local Bus Controller Interface				
LD0	U18	I/O	NV_{DDP_K}	8
LD1	V18	I/O	NV_{DDP_K}	8
LD2	U16	I/O	NV_{DDP_K}	8
LD3	Y20	I/O	NV_{DDP_K}	8
LD4	AA21	I/O	NV_{DDP_K}	8
LD5	AC22	I/O	NV_{DDP_K}	8
LD6	V17	I/O	NV_{DDP_K}	8
LD7	AB21	I/O	NV_{DDP_K}	8
LD8	Y19	I/O	NV_{DDP_K}	8
LD9	AA20	I/O	NV_{DDP_K}	8
LD10	Y17	I/O	NV_{DDP_K}	8

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
IIC_SCL1	A9	I/O	NV_{DDA}	2
IIC_SDA2/$\overline{\text{CKSTOP\_OUT}}$	D10	I/O	NV_{DDA}	2
IIC_SCL2/$\overline{\text{CKSTOP\_IN}}$	C10	I/O	NV_{DDA}	2
Interrupts				
IRQ[0]/$\overline{\text{MCP\_IN}}$	A17	I	NV_{DDB}	—
IRQ[1]/$\overline{\text{MCP\_OUT}}$	F16	I/O	NV_{DDB}	—
IRQ[2] /$\overline{\text{CKSTOP\_OUT}}$	B17	I/O	NV_{DDB}	—
IRQ[3] /$\overline{\text{CKSTOP\_IN}}$	A18	I	NV_{DDB}	—
JTAG				
TCK	Y7	I	NV_{DDP_K}	—
TDI	U9	I	NV_{DDP_K}	4
TDO	AC5	O	NV_{DDP_K}	3
TMS	AA6	I	NV_{DDP_K}	4
$\overline{\text{TRST}}$	V8	I	NV_{DDP_K}	4
TEST				
TEST_MODE	AC6	I	NV_{DDP_K}	5
System Control				
$\overline{\text{HRESET}}$	AA9	I/O	NV_{DDP_K}	1
$\overline{\text{PORESET}}$	AA8	I	NV_{DDP_K}	—
$\overline{\text{SRESET}}$	AB7	I/O	NV_{DDP_K}	—
Clocks				
SYS_CLK_IN	AC8	I	NV_{DDP_K}	—
RTC_PIT_CLOCK	AA23	I	NV_{DDJ}	—
MISC				
QUIESCE	AA7	O	NV_{DDP_K}	—
THERM0	AC7	I	NV_{DDP_K}	6
ETSEC1				
TSEC1_COL	B20	I	NV_{DDC}	—
TSEC1_CRS	B21	I	NV_{DDC}	—
TSEC1_GTX_CLK	F18	O	NV_{DDC}	3
TSEC1_RX_CLK	A22	I	NV_{DDC}	—
TSEC1_RX_DV	D21	I	NV_{DDC}	—
TSEC1_RXD[3]	C22	I	NV_{DDC}	—
TSEC1_RXD[2]	C21	I	NV_{DDC}	—

This table provides the operating frequencies for the device under recommended operating conditions (Table 2).

Table 55. Operating Frequencies for MPC8308

Characteristic[1]	Maximum Operating Frequency	Unit
e300 core frequency (*core_clk*)	400	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
DDR2 memory bus frequency (MCK)[2]	133	MHz
Local bus frequency (LCLK*0*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK0, and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCCR[CLKDIV]) which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

21.2 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

Table 56. System PLL Ratio

RCWL[SPMF]	csb_clk: SYS_CLK_IN
0000	Reserved
0001	Reserved
0010	2 : 1
0011	3 : 1
0100	4 : 1
0101	5 : 1
0110–1111	Reserved

As described in Section 21, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (SYS_CLK_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN ratios.

Table 57. CSB Frequency Options

SPMF *csb_clk* :Input Clock Ratio		Input Clock Frequency (MHz)		
		25	33.33	66.67
0010	2:1			133
0100	4:1		133	
0101	5:1	125	167	

23.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8308 system, and the MPC8308 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, NV_{DD}, GV_{DD} and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, and V_{SS} power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, NV_{DD}, GV_{DD}, LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

23.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, LV_{DD} as required. Unused active high inputs should be connected to VSS. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, AV_{DD1}, AV_{DD2}, GV_{DD}, LV_{DD} and V_{SS} pins of the device.

23.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C, MDIO and HRESET)

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS}. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (Figure 55). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

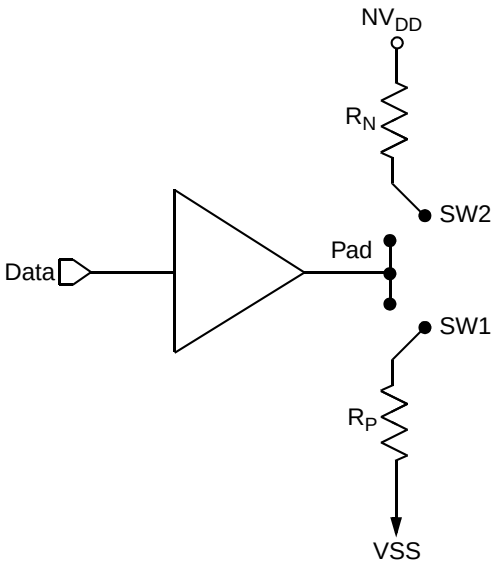

Figure 55. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal NV_{DD}, 105°C.

Table 60. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	Ω
R_P	42 Target	20 Target	Z_0	Ω

Note: Nominal supply voltages. See Table 2, T_j = 105°C.

23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 KΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{PORESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{PORESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

23.7 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C, Ethernet management MDIO, $\overline{\text{HRESET}}$ and IPIC (integrated programmable interrupt controller).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 56. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions because most have asynchronous behavior and spurious assertion, which give unpredictable results.

24 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 24.1, "Part Numbers Fully Addressed by This Document."

24.1 Part Numbers Fully Addressed by This Document

This table provides the Freescale part numbering nomenclature for the MPC8308 family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed. Each part number also contains a revision code which refers to the die mask revision number.

Table 61. Part Numbering Nomenclature

MPC	*nnnn*	*C*	*VM*	*AD*	*D*	*A*
Product Code	**Part Identifier**	**Temperature Range[1,4]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR Frequency**	**Revision Level**
MPC	8308	Blank = 0 to 105°C C = –40 to 105°C	VM = Pb-free 473 MAPBGA	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz	Contact local Freescale sales office

Notes:

1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 20, "Package and Pin Listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies
4. Minimum temperature is specified with T_A; Maximum temperature is specified with T_J

25 Document Revision History

This table summarizes a revision history for this document.

Table 63. Document Revision History

Rev. Number	Date	Substantive Change(s)
3	10/2011	• In Section 2.1.4, "Power Sequencing," changed description. • In Table 53, updated GPIOs pins as I/O. • In Table 54, removed PCI Express = csb_clk/2 and csb_clk/3 options. • In Table 61, added note 4.
2	02/2011	• Added NV_{DDJ} to Note-7 in Table 1. • In Table 2, Added Note-2 Added NV_{DDJ} to Note-3 Added "Extended Temperature range from -40 to 105 °C, in the last row of the table Changed "characteristic name Junction temperature" to "Operating temperature range" • In Table 4, Note-3, changed ambient temperature to junction temperature, T_J = 105° C • In Table 18, t_{DDKHCS} changed from 3.15ns to 2.5ns t_{DDKHMP} and t_{DDKHME} values updated • In Figure 6, corrected t_{DDKHMP} & t_{DDKHME} waveform • In Table 53, Y23 Package Pin Number changed from NC to V_{DD} signal group TSEC2_CRS is muxed with GPIO[0], shown as TSEC2_CRS/ GPIO[0] • In Table 58, note-1, core_clk maximum operating frequency 333 MHz replaced with 400 MHz
1	06/2010	• In Table 4, T_A = 105 replaced with T_J = 105 • In Table 8, $f_{SYS\_CLK\_IN}$ (Max) = 66 replaced with 66.67 and $t_{SYS\_CLK\_IN}$ (Min) = 15.15 replaced with 15 • In Table 53, TSEC1_TMR_RX_ESFD replaced with TSEC2_TMR_RX_ESFD TSEC1_TMR_TX_ESFD replaced with TSEC2_TMR_TX_ESFD TSEC0_TMR_RX_ESFD replaced with TSEC1_TMR_RX_ESFD TSEC0_TMR_TX_ESFD replaced with TSEC1_TMR_TX_ESFD • In Table 56, rows from 1000 to 1111 removed • In Table 57, SPMF 5:1 Option 167 MHz added.
0	05/2010	Initial release