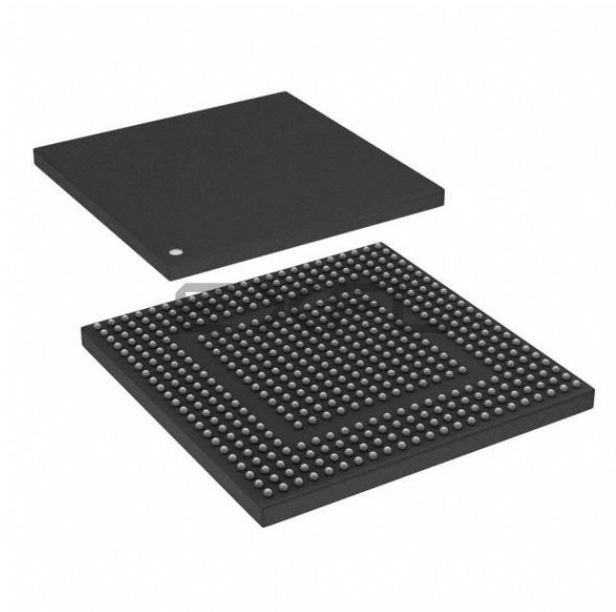


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

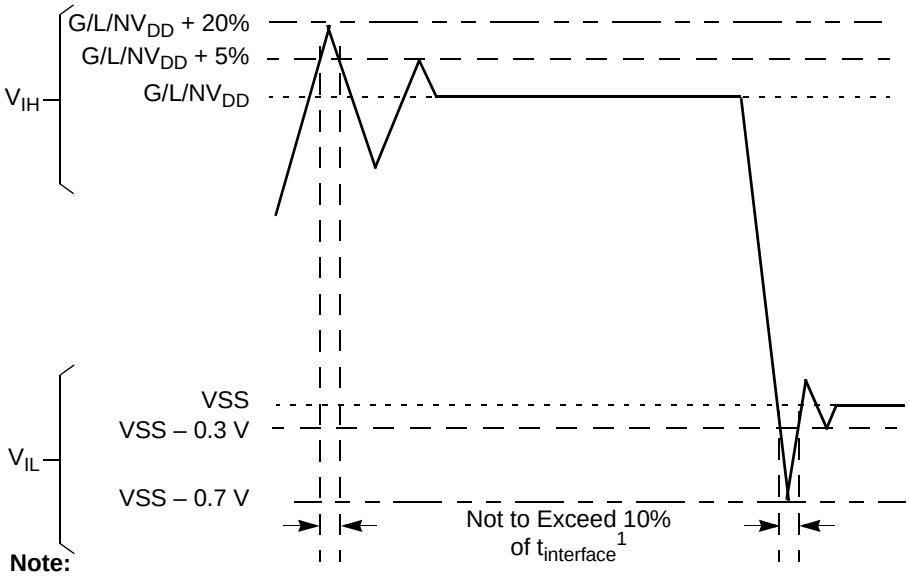
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8308cvmadda

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GVDD/NVDD/LVDD

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NV_{DD} = 3.3 V
DDR2 signals[1]	18	GV_{DD} = 1.8 V
DUART, system control, I^2C, JTAG, eSDHC, GPIO,SPI, USB	42	NV_{DD} = 3.3 V
eTSEC signals	42	LV_{DD} = 2.5/3.3 V

[1] Output Impedance can also be adjusted through configurable options in DDR Control Driver Register (DDRCDR). For more information, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

2.1.4 Power Sequencing

It is required to apply the core supply voltage (V_{DD}) before the I/O supply voltages (GV_{DD}, LV_{DD}, and NV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. The core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3.

If this recommendation is not observed and I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. To overcome side effects of this condition, the application environment may require tuning of external pull-up or pull-down resistors on particular signals to lesser values.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ//MDM/MECC output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}		—	ps	5
266 MHz		900			
MDQ//MDM/MECC output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}		—	ps	5
266 MHz		1100			
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure shows the MII transmit AC timing diagram.

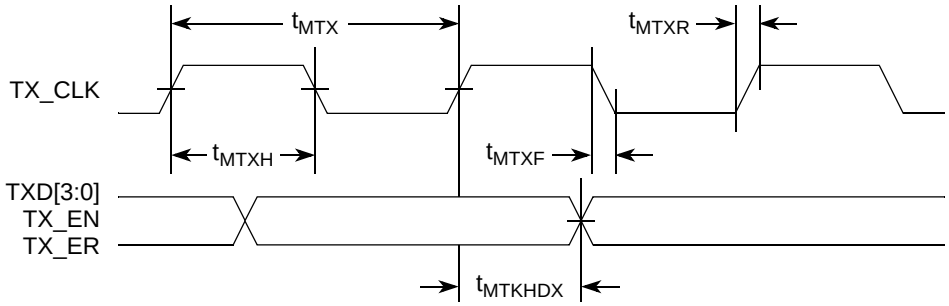


Figure 8. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

10 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

10.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 15 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX*n* and $\overline{\text{TX}n}$) or a receiver input (RX*n* and $\overline{\text{RX}n}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- **Single-Ended Swing**

  The transmitter output signals and the receiver input signals TX*n*, $\overline{\text{TX}n}$, RX*n*, and $\overline{\text{RX}n}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's single-ended swing.
- **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**)

  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.
- **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**)

  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.
- **Differential Peak Voltage, V_{DIFFp}**

  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, V_{DIFFp} = |A – B| Volts.
- **Differential Peak-to-Peak, $V_{DIFFp-p}$**

  Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.
- **Differential Waveform**

  The differential waveform is constructed by subtracting the inverting signal (for example, $\overline{\text{TX}n}$) from the non-inverting signal (for example, TX*n*) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 24 as an example for differential waveform.

- **Common Mode Voltage, V_{cm}**

  The common mode voltage is equal to one-half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{TXn} + V_{\overline{TXn}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

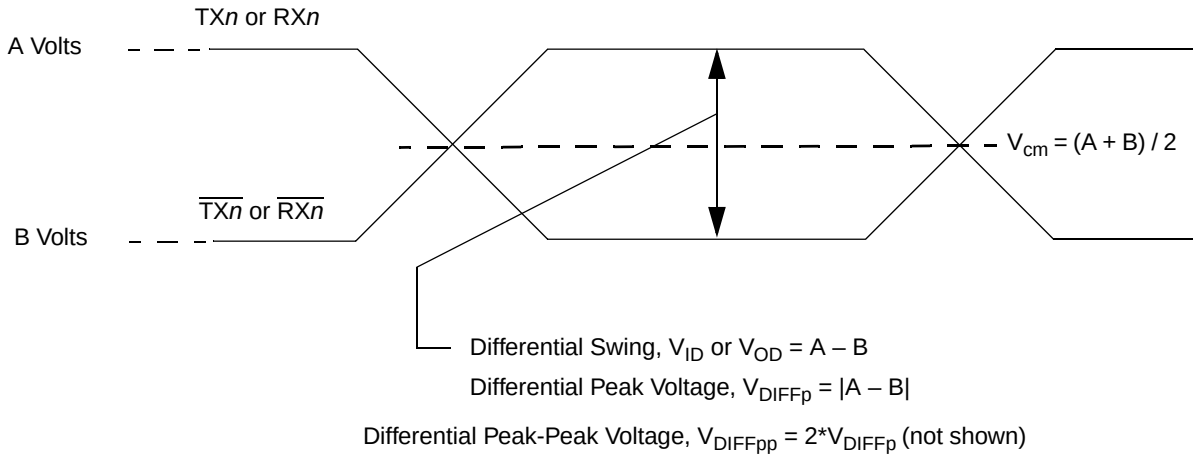


Figure 15. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

10.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for PCI Express.

The following sections describe the SerDes reference clock requirements and some application information.

10.2.1 SerDes Reference Clock Receiver Characteristics

Figure 16 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XCOREVDD are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 16. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above XCOREVSS. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to XCOREVSS DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

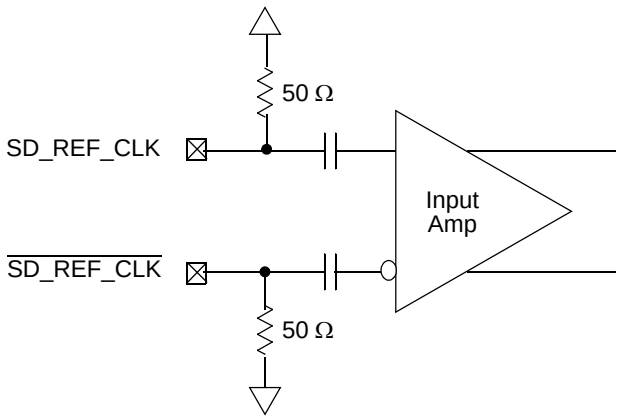


Figure 16. Receiver of SerDes Reference Clocks

Table 32. SerDes Reference Clock AC Parameters (continued)

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
Rising edge rate (SD_REF_CLK) to falling edge rate ($\overline{\text{SD\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing (Figure 24).
4. Matching applies to rising edge rate for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate (See Figure 25).

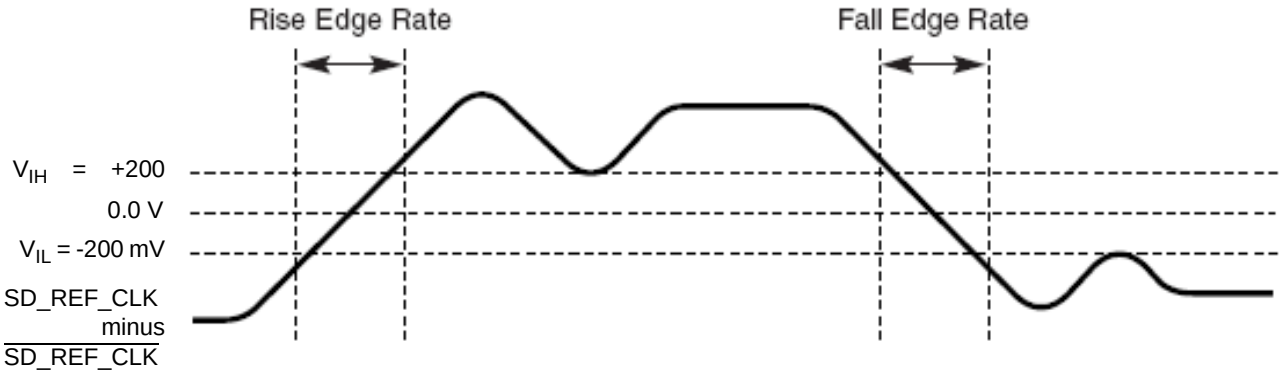


Figure 24. Differential Measurement Points for Rise and Fall Time

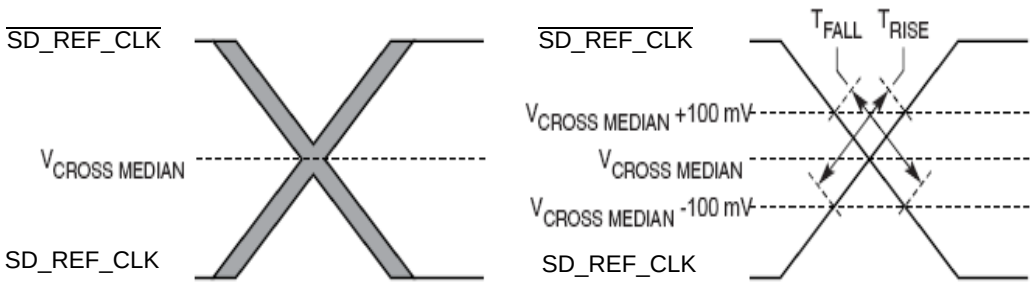


Figure 25. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. For detailed information, see the following sections:

- Section 11.2, “AC Requirements for PCI Express SerDes Clocks”

Table 35. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
AC peak common mode input voltage	$V_{RX-CM-ACp}$	$V_{PEACPCMRX} = \lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$	—	—	150	mV	2
Differential return loss	$RL_{RX-DIFF}$	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively.	15	—	—	dB	4
Common mode return loss	RL_{RX-CM}	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V.	6	—	—	dB	4
DC differential input impedance	$Z_{RX-DIFF-DC}$	RX DC differential mode impedance.	80	100	120	Ω	5
DC Input Impedance	Z_{RX-DC}	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance).	40	50	60	Ω	2, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	$V_{PEEIDT} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

Table 35. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 29 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 28). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 29). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

11.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 28 is specified using the passive compliance/test measurement load (Figure 29) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (Figure 29) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 28) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

Figure 31 through Figure 33 show the local bus signals. In what follows, T1, T2, T3, and T4 are internal clock reference phase signals corresponding to LCCR[CLKDIV].

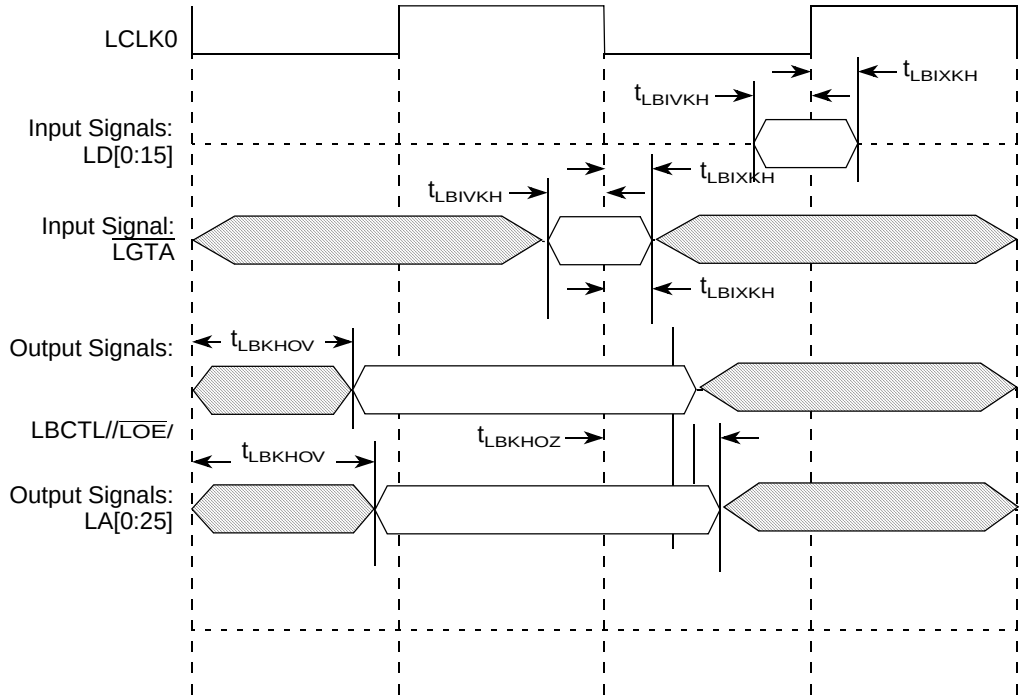


Figure 31. Local Bus Signals, Non-Special Signals Only

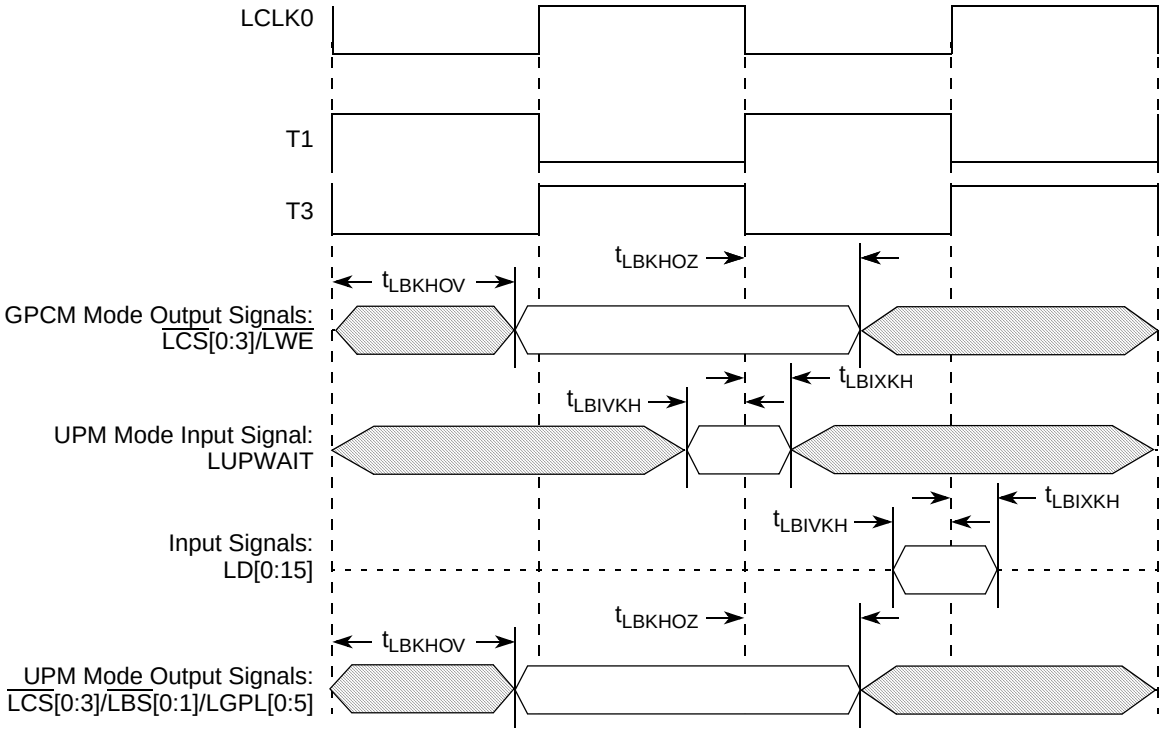


Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2

Table 38. eSDHC interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V

13.2 eSDHC AC Timing Specifications (Full Speed Mode)

This section describes the AC electrical specifications for the eSDHC (SD/MMC) interface of the device. This table provides the eSDHC AC timing specifications for full speed mode as defined in Figure 35 and Figure 36.

Table 39. eSDHC AC Timing Specifications for Full Speed Mode

At recommended operating conditions NV_{DD} = 3.3 V ± 300 mV.

Parameter	Symbol [1]	Min	Max	Unit	Notes
SD_CLK clock frequency—full speed mode	f_{SFSCK}	0	25	MHz	—
SD_CLK clock cycle	t_{SFSCK}	40	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	kHz	—
SD_CLK clock low time	t_{SFSCKL}	15	—	ns	2
SD_CLK clock high time	t_{SFSCKH}	15	—	ns	2
SD_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	5	ns	2
Input setup times: SD_CMD, SD_DATx to SD_CLK	$t_{SFSIVKH}$	3	—	ns	2
Input hold times: SD_CMD, SD_DATx to SD_CLK	$t_{SFSIXKH}$	2	—	ns	2
Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOV}$	—	3	ns	2
Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOX}$	–3	—	—	—
SD card input setup	t_{ISU}	5	—	ns	3
SD card input hold	t_{IH}	5	—	ns	3
SD card output valid	t_{ODLY}	—	14	ns	3
SD card output hold	t_{OH}	0	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

14 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

14.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 41. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—		±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

14.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

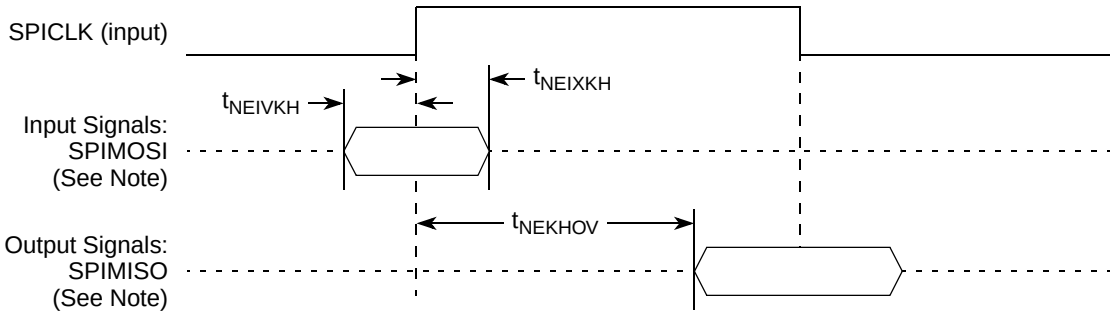
This table provides the JTAG AC timing specifications as defined in Figure 41 through Figure 44.

Table 42. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5

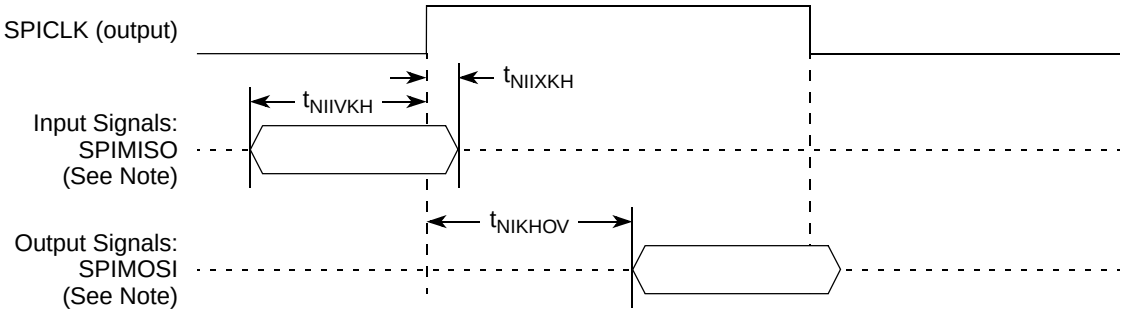
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 51. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8308 is available in a moulded array process ball grid array (MAPBGA). For information on the MAPBGA, see Section 20.1, "Package Parameters for the MPC8308 MAPBGA," and Section 20.2, "Mechanical Dimensions of the MPC8308 MAPBGA."

20.1 Package Parameters for the MPC8308 MAPBGA

The package parameters are as provided in the following list. The package type is 19 mm × 19 mm, 473 MAPBGA.

Package outline	19 mm × 19 mm
Interconnects	473
Pitch	0.80 mm
Module height (typical)	1.39 mm
Solder Balls	96.5 Sn/ 3.5Ag
Ball diameter (typical)	0.40 mm

2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

20.3 Pinout Listings

This table provides the pin-out listing for the MPC8308, MAPBGA package.

Table 53. MPC8308 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	V6	I/O	GV_{DDA}	—
MEMC_MDQ[1]	Y4	I/O	GV_{DDA}	—
MEMC_MDQ[2]	AB3	I/O	GV_{DDA}	—
MEMC_MDQ[3]	AA3	I/O	GV_{DDA}	—
MEMC_MDQ[4]	AA2	I/O	GV_{DDA}	—
MEMC_MDQ[5]	AA1	I/O	GV_{DDA}	—
MEMC_MDQ[6]	W4	I/O	GV_{DDA}	—
MEMC_MDQ[7]	Y2	I/O	GV_{DDA}	—
MEMC_MDQ[8]	W3	I/O	GV_{DDA}	—
MEMC_MDQ[9]	W1	I/O	GV_{DDA}	—
MEMC_MDQ[10]	Y1	I/O	GV_{DDA}	—
MEMC_MDQ[11]	W2	I/O	GV_{DDA}	—
MEMC_MDQ[12]	U4	I/O	GV_{DDA}	—
MEMC_MDQ[13]	U3	I/O	GV_{DDA}	—
MEMC_MDQ[14]	V4	I/O	GV_{DDA}	—
MEMC_MDQ[15]	U6	I/O	GV_{DDA}	—
MEMC_MDQ[16]	T3	I/O	GV_{DDB}	—
MEMC_MDQ[17]	T2	I/O	GV_{DDB}	—
MEMC_MDQ[18]	R4	I/O	GV_{DDB}	—
MEMC_MDQ[19]	R3	I/O	GV_{DDB}	—
MEMC_MDQ[20]	P4	I/O	GV_{DDB}	—
MEMC_MDQ[21]	N6	I/O	GV_{DDB}	—
MEMC_MDQ[22]	P2	I/O	GV_{DDB}	—
MEMC_MDQ[23]	P1	I/O	GV_{DDB}	—
MEMC_MDQ[24]	N4	I/O	GV_{DDB}	—
MEMC_MDQ[25]	N3	I/O	GV_{DDB}	—
MEMC_MDQ[26]	N2	I/O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

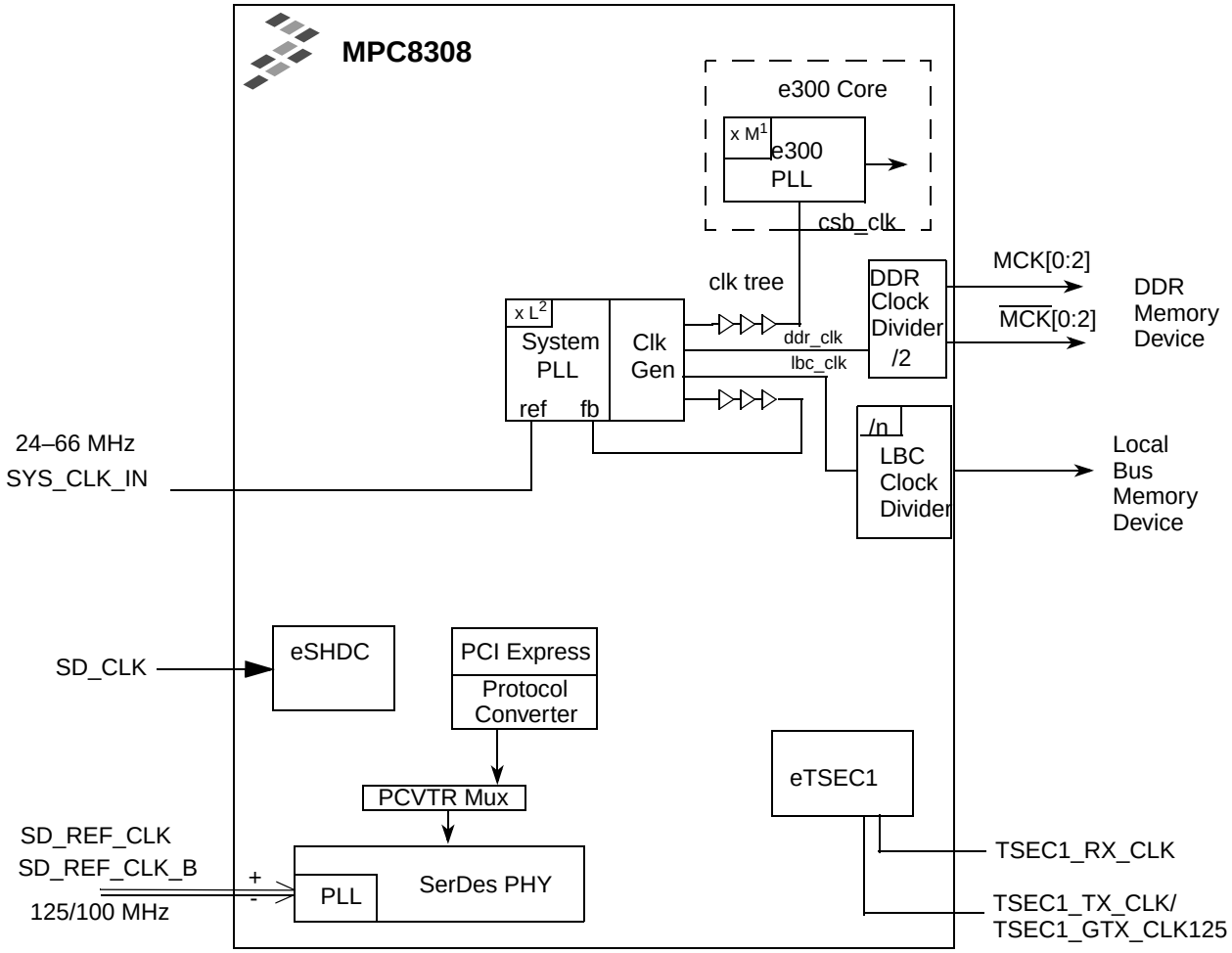
Signal	Package Pin Number	Pin Type	Power Supply	Note
LD11	AC21	I/O	NV_{DDP_K}	8
LD12	AB20	I/O	NV_{DDP_K}	8
LD13	V16	I/O	NV_{DDP_K}	8
LD14	AA19	I/O	NV_{DDP_K}	8
LD15	AC17	I/O	NV_{DDP_K}	8
LA0	AC20	O	NV_{DDP_K}	—
LA1	Y16	O	NV_{DDP_K}	—
LA2	U15	O	NV_{DDP_K}	—
LA3	V15	O	NV_{DDP_K}	—
LA4	AA18	O	NV_{DDP_K}	—
LA5	AA17	O	NV_{DDP_K}	—
LA6	AC19	O	NV_{DDP_K}	—
LA7	AA16	O	NV_{DDP_K}	—
LA8	AB18	O	NV_{DDP_K}	—
LA9	AC18	O	NV_{DDP_K}	—
LA10	V14	O	NV_{DDP_K}	—
LA11	AB17	O	NV_{DDP_K}	—
LA12	AA15	O	NV_{DDP_K}	—
LA13	AC16	O	NV_{DDP_K}	—
LA14	Y14	O	NV_{DDP_K}	—
LA15	AC15	O	NV_{DDP_K}	—
LA16	U13	O	NV_{DDP_K}	—
LA17	V13	O	NV_{DDP_K}	—
LA18	Y13	O	NV_{DDP_K}	—
LA19	AB15	O	NV_{DDP_K}	—
LA20	AA14	O	NV_{DDP_K}	—
LA21	AB14	O	NV_{DDP_K}	—
LA22	U12	O	NV_{DDP_K}	—
LA23	V12	O	NV_{DDP_K}	—
LA24	Y12	O	NV_{DDP_K}	—
LA25	AC14	O	NV_{DDP_K}	—
$\overline{\text{LCS}}$[0]	AA13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[1]	AB13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[2]	AA12	O	NV_{DDP_K}	4

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC1_RXD[1]	C20	I	NV_{DDC}	—
TSEC1_RXD[0]	D20	I	NV_{DDC}	—
TSEC1_RX_ER	C23	I	NV_{DDC}	—
TSEC1_TX_CLK/ TSEC1_GTX_CLK125	E23	I	NV_{DDC}	—
TSEC1_TXD[3]/ CFG_RESET_SOURCE[0]	F22	I/O	NV_{DDC}	—
TSEC1_TXD[2]/ CFG_RESET_SOURCE[1]	F21	I/O	NV_{DDC}	—
TSEC1_TXD[1]/ CFG_RESET_SOURCE[2]	E21	I/O	NV_{DDC}	—
TSEC1_TXD[0]/ CFG_RESET_SOURCE[3]	D22	I/O	NV_{DDC}	—
TSEC1_TX_EN/ LBC_PM_REF_10	F20	O	NV_{DDC}	—
TSEC1_TX_ER/ LB_POR_CFG_BOOT_ECC	E22	I/O	NV_{DDC}	7
Ethernet Mgmt				
TSEC1_MDC	A20	O	NV_{DDB}	—
TSEC1_MDIO	C19	I/O	NV_{DDB}	2
eSDHC/GTM				
SD_CLK/GPIO[16]	D7	O	NV_{DDA}	—
SD_CMD/GPIO[17]	G9	I/O	NV_{DDA}	—
$\overline{\text{SD\_CD}}$/GTM1_TIN1/ GPIO[18]	A7	I	NV_{DDA}	—
SD_WP/$\overline{\text{GTM1\_TGATE1}}$/ GPIO[19]	D8	I	NV_{DDA}	—
SD_DAT[0]/$\overline{\text{GTM1\_TOUT1}}$/ GPIO[20]	C8	I/O	NV_{DDA}	—
SD_DAT[1]/$\overline{\text{GTM1\_TOUT2}}$/ GPIO[21]	B8	I/O	NV_{DDA}	—
SD_DAT[2]/GTM1_TIN2/ GPIO[22]	A8	I/O	NV_{DDA}	—
SD_DAT[3]/$\overline{\text{GTM1\_TGATE2}}$/ GPIO[23]	B9	I/O	NV_{DDA}	—
SPI				
SPIMOSI/MSRCID4/ LSRCID4	AB5	I/O	NV_{DDP_K}	—
SPIMISO/MDVAL/LDVAL	Y6	I/O	NV_{DDP_K}	—

21 Clocking

This figure shows the internal distribution of clocks within the device.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4, 5 and 6. Value is decided by RCWLR[SPMF].

Figure 53. MPC8308 Clock Subsystem

The following external clock sources are utilized on the MPC8308:

- System clock (SYS_CLK_IN)
- Ethernet Clock (TSEC1_RX_CLK/TSEC1_TX_CLK/TSEC1_GTX_CLK125 for eTSEC)
- SerDes PHY clock
- eSHDC clock (SD_CLK)

  For more information, see the SerDes chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

All clock inputs can be supplied using an external canned oscillator, a clock generation chip, or some other source that provides a standard CMOS square wave input.

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the device

23.1 System Clocking

The device includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 21.2, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.3, “Core PLL Configuration.”

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} for core PLL and AV_{DD2} for the platform PLL). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low pass filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 54, one to each of the two AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs’ resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

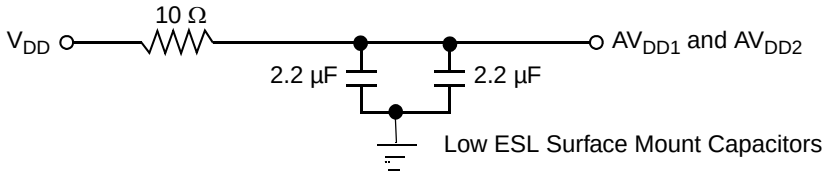


Figure 54. PLL Power Supply Filter Circuit

25 Document Revision History

This table summarizes a revision history for this document.

Table 63. Document Revision History

Rev. Number	Date	Substantive Change(s)
3	10/2011	• In Section 2.1.4, "Power Sequencing," changed description. • In Table 53, updated GPIOs pins as I/O. • In Table 54, removed PCI Express = csb_clk/2 and csb_clk/3 options. • In Table 61, added note 4.
2	02/2011	• Added NV_{DDJ} to Note-7 in Table 1. • In Table 2, Added Note-2 Added NV_{DDJ} to Note-3 Added "Extended Temperature range from -40 to 105 °C, in the last row of the table Changed "characteristic name Junction temperature" to "Operating temperature range" • In Table 4, Note-3, changed ambient temperature to junction temperature, T_J = 105° C • In Table 18, t_{DDKHCS} changed from 3.15ns to 2.5ns t_{DDKHMP} and t_{DDKHME} values updated • In Figure 6, corrected t_{DDKHMP} & t_{DDKHME} waveform • In Table 53, Y23 Package Pin Number changed from NC to V_{DD} signal group TSEC2_CRS is muxed with GPIO[0], shown as TSEC2_CRS/ GPIO[0] • In Table 58, note-1, core_clk maximum operating frequency 333 MHz replaced with 400 MHz
1	06/2010	• In Table 4, T_A = 105 replaced with T_J = 105 • In Table 8, $f_{SYS\_CLK\_IN}$ (Max) = 66 replaced with 66.67 and $t_{SYS\_CLK\_IN}$ (Min) = 15.15 replaced with 15 • In Table 53, TSEC1_TMR_RX_ESFD replaced with TSEC2_TMR_RX_ESFD TSEC1_TMR_TX_ESFD replaced with TSEC2_TMR_TX_ESFD TSEC0_TMR_RX_ESFD replaced with TSEC1_TMR_RX_ESFD TSEC0_TMR_TX_ESFD replaced with TSEC1_TMR_TX_ESFD • In Table 56, rows from 1000 to 1111 removed • In Table 57, SPMF 5:1 Option 167 MHz added.
0	05/2010	Initial release