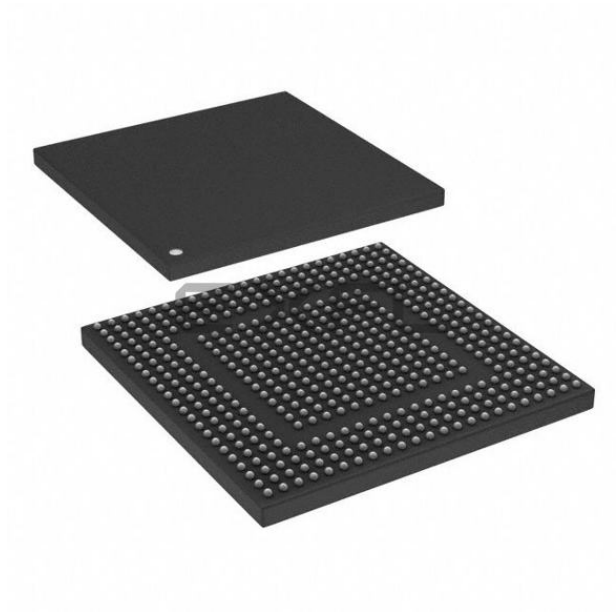

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8308cvmafd

1 Overview

This figure shows the major functional units within the MPC8308. The e300 core in the MPC8308, with its 16 Kbytes of instruction and 16 Kbytes of data cache, implements the Power Architecture user instruction set architecture and provides hardware and software debugging support. In addition, the MPC8308 offers a PCI Express controller, two three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSEC), a DDR2 SDRAM memory controller, a SerDes block, an enhanced local bus controller (eLBC), an integrated programmable interrupt controller (IPIC), a general purpose DMA controller, two I^2C controllers, dual UART (DUART), GPIOs, USB, general purpose timers, and an SPI controller. The high level of integration in the MPC8308 helps simplify board design and offers significant bandwidth and performance.

This figure shows a block diagram of the device.

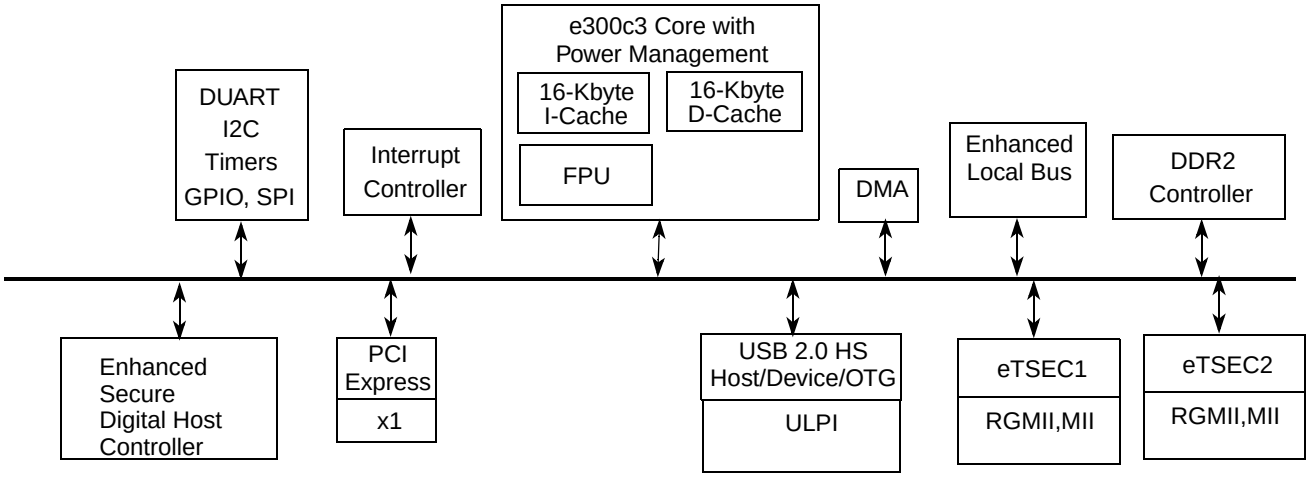

Figure 1. MPC8308 Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8308. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8308 Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	NV_{DD} (3.3 V)	LV_{DD}/ (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR2 R_S = 22 Ω R_t = 75 Ω	250 MHz 32 bits+ECC 266 MHz 32 bits+ECC	0.302 0.309	—	—	—	W	—
Local bus I/O load = 20 pF	62.5 MHz 66 MHZ	—	0.038 0.040	—	—	W	—
TSEC I/O load = 20 pF	MII, 25 MHz	—	—	0.008	—	W	2 controllers
	RGMII, 125 MHz	—	—	0.078	0.044	W	
eSDHC IO Load = 40 pF	50 MHz	—	—	0.008	—	W	—
USB IO Load = 20 pF	60 MHz	—	—	0.012		W	—
Other I/O	—	—	0.017	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN) DC electrical specifications for the device.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V $\le V_{IN} \le NV_{DD}$	I_{IN}	—	±10	μA

This table provides the RTC clock input (RTC_PIT_CLOCK) DC electrical specifications for the device.

Table 7. RTC_PIT_CLOCK DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	3.3 V – 400 mV		V
Input low voltage	—	V_{IL}	0	0.4	V

4.2 AC Electrical Characteristics

The primary clock source for the device is SYS_CLK_IN. This table provides the system clock input (SYS_CLK_IN) AC timing specifications for the device.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/	Symbol	Min	Typ	Max	Unit	Notes
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1, 6
SYS_CLK_IN period	$t_{SYS\_CLK\_IN}$	15	—	41.67	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6		1.2	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system and core must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33 kHz (max rate).

Table 9. RTC_PIT_CLOCK AC Timing Specifications

Parameter/	Symbol	Min	Typ	Max	Unit	Notes
RTC_PIT_CLOCK frequency	$f_{RTC\_PIT\_CLOCK}$	1	32768	—	Hz	—
RTC_PIT_CLOCK rise and fall time	t_{RTCH}, t_{RTCL}	1.5	—	3	μs	—
RTC_PIT_CLOCK duty cycle	$t_{RTCHK}/t_{RTC\_PIT\_CLOCK}$	45	—	55	%	—

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the device.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

Table 10. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$		±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ (input) to activate reset flow	32	—	$t_{SYS\_CLK\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable power and clock applied to SYS_CLK_IN	32	—	$t_{SYS\_CLK\_IN}$	—
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS\_CLK\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of PORESET	4	—	$t_{SYS\_CLK\_IN}$	—
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	2
Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$	1	—	ns	1, 2

Notes:
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN.
2. POR configuration signals consists of CFG_RESET_SOURCE[0:3].

This table provides the PLL lock times.

Table 12. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
System PLL lock time	—	100	μs	—
e300 core PLL lock time	—	100	μs	—

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.45	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.45	—	V	—

This table provides input AC timing specifications for the DDR2 SDRAM interface.

Table 17. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 1.8± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC 266 MHz	t_{CISKEW}	–875	875	ps	1, 2,3

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ or MECC signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = +/–(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Memory controller ODT value of 150 Ω is recommended

This figure illustrates the DDR2 input timing diagram showing the t_{DISKEW} timing parameter.

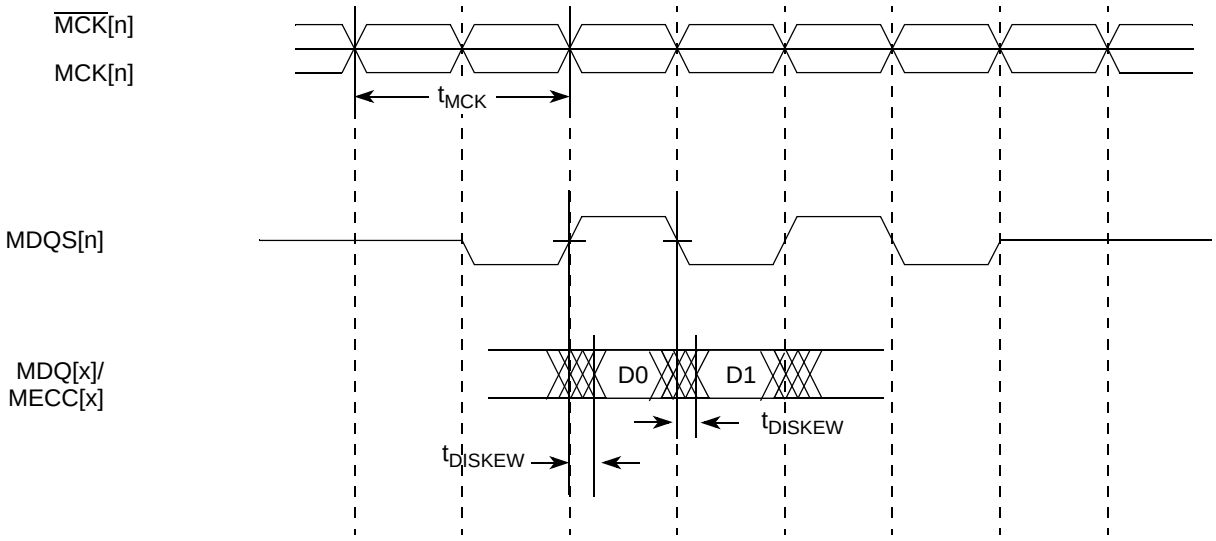

Figure 4. Timing Diagram for t_{DISKEW}

6.2.2 DDR2 SDRAM Output AC Timing Specifications

Table 18. DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}		—	ns	3
266 MHz		2.9			
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}		—	ns	3
266 MHz		2.33			
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}		—	ns	3
266 MHz		2.5			
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}		—	ns	3
266 MHz		3.15			
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ//MDM/MECC output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}		—	ps	5
266 MHz		900			
MDQ//MDM/MECC output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}		—	ps	5
266 MHz		1100			
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

10.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8308 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 10.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 17 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 18 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 19 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

Table 35. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 29 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 28). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 29). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

11.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 28 is specified using the passive compliance/test measurement load (Figure 29) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (Figure 29) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 28) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

14 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

14.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 41. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—		±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

14.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

This table provides the JTAG AC timing specifications as defined in Figure 41 through Figure 44.

Table 42. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5

Table 42. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 40). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

This figure provides the AC test load for TDO and the boundary-scan outputs.

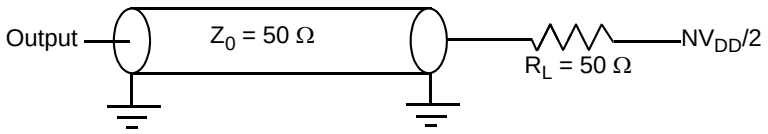

Figure 40. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

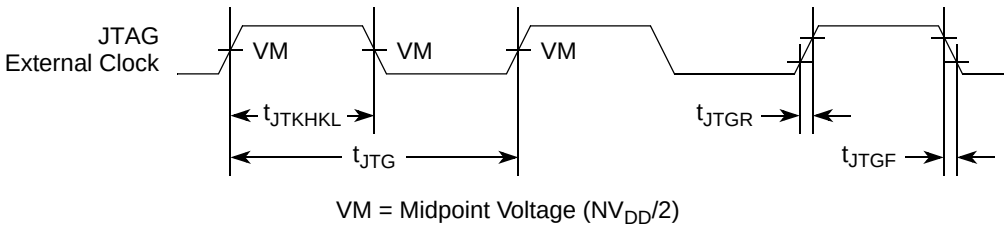

Figure 41. JTAG Clock Input Timing Diagram

Table 44. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The device does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

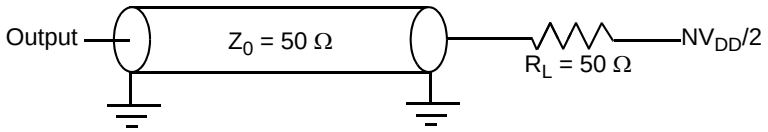

Figure 45. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

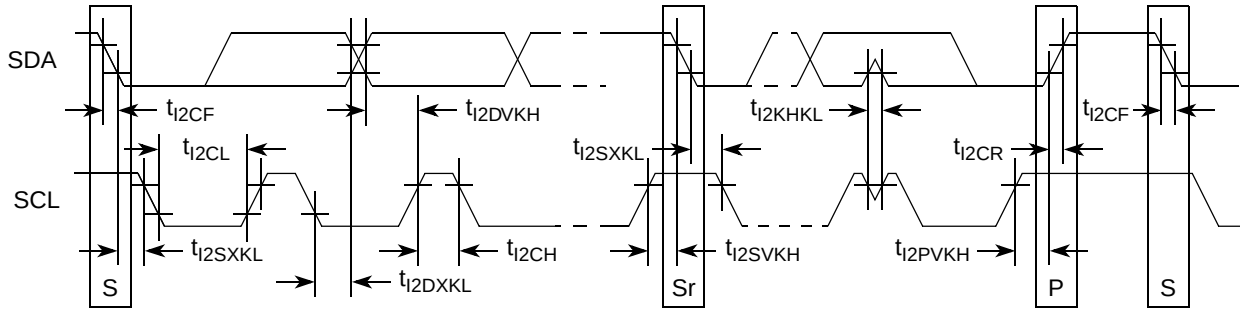

Figure 46. I²C Bus AC Timing Diagram

16 Timers

This section describes the DC and AC electrical specifications for the timers.

16.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8308 timers pins, including TIN, $\overline{\text{TOUT}}$, and $\overline{\text{TGATE}}$.

Table 45. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

16.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 46. Timers Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the Timers.

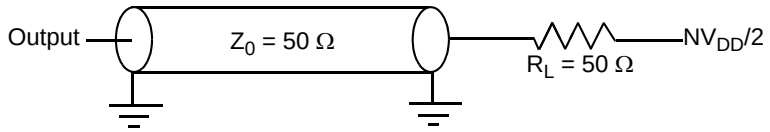

Figure 47. Timers AC Test Load

18 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

18.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 49. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

18.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 50. IPIC Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

19 SPI

This section describes the DC and AC electrical specifications for the SPI of the device.

19.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8308 SPI.

Table 51. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

20.3 Pinout Listings

This table provides the pin-out listing for the MPC8308, MAPBGA package.

Table 53. MPC8308 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	V6	I/O	GV_{DDA}	—
MEMC_MDQ[1]	Y4	I/O	GV_{DDA}	—
MEMC_MDQ[2]	AB3	I/O	GV_{DDA}	—
MEMC_MDQ[3]	AA3	I/O	GV_{DDA}	—
MEMC_MDQ[4]	AA2	I/O	GV_{DDA}	—
MEMC_MDQ[5]	AA1	I/O	GV_{DDA}	—
MEMC_MDQ[6]	W4	I/O	GV_{DDA}	—
MEMC_MDQ[7]	Y2	I/O	GV_{DDA}	—
MEMC_MDQ[8]	W3	I/O	GV_{DDA}	—
MEMC_MDQ[9]	W1	I/O	GV_{DDA}	—
MEMC_MDQ[10]	Y1	I/O	GV_{DDA}	—
MEMC_MDQ[11]	W2	I/O	GV_{DDA}	—
MEMC_MDQ[12]	U4	I/O	GV_{DDA}	—
MEMC_MDQ[13]	U3	I/O	GV_{DDA}	—
MEMC_MDQ[14]	V4	I/O	GV_{DDA}	—
MEMC_MDQ[15]	U6	I/O	GV_{DDA}	—
MEMC_MDQ[16]	T3	I/O	GV_{DDB}	—
MEMC_MDQ[17]	T2	I/O	GV_{DDB}	—
MEMC_MDQ[18]	R4	I/O	GV_{DDB}	—
MEMC_MDQ[19]	R3	I/O	GV_{DDB}	—
MEMC_MDQ[20]	P4	I/O	GV_{DDB}	—
MEMC_MDQ[21]	N6	I/O	GV_{DDB}	—
MEMC_MDQ[22]	P2	I/O	GV_{DDB}	—
MEMC_MDQ[23]	P1	I/O	GV_{DDB}	—
MEMC_MDQ[24]	N4	I/O	GV_{DDB}	—
MEMC_MDQ[25]	N3	I/O	GV_{DDB}	—
MEMC_MDQ[26]	N2	I/O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
IIC_SCL1	A9	I/O	NV_{DDA}	2
IIC_SDA2/$\overline{\text{CKSTOP\_OUT}}$	D10	I/O	NV_{DDA}	2
IIC_SCL2/$\overline{\text{CKSTOP\_IN}}$	C10	I/O	NV_{DDA}	2
Interrupts				
IRQ[0]/$\overline{\text{MCP\_IN}}$	A17	I	NV_{DDB}	—
IRQ[1]/$\overline{\text{MCP\_OUT}}$	F16	I/O	NV_{DDB}	—
IRQ[2] /$\overline{\text{CKSTOP\_OUT}}$	B17	I/O	NV_{DDB}	—
IRQ[3] /$\overline{\text{CKSTOP\_IN}}$	A18	I	NV_{DDB}	—
JTAG				
TCK	Y7	I	NV_{DDP_K}	—
TDI	U9	I	NV_{DDP_K}	4
TDO	AC5	O	NV_{DDP_K}	3
TMS	AA6	I	NV_{DDP_K}	4
$\overline{\text{TRST}}$	V8	I	NV_{DDP_K}	4
TEST				
TEST_MODE	AC6	I	NV_{DDP_K}	5
System Control				
$\overline{\text{HRESET}}$	AA9	I/O	NV_{DDP_K}	1
$\overline{\text{PORESET}}$	AA8	I	NV_{DDP_K}	—
$\overline{\text{SRESET}}$	AB7	I/O	NV_{DDP_K}	—
Clocks				
SYS_CLK_IN	AC8	I	NV_{DDP_K}	—
RTC_PIT_CLOCK	AA23	I	NV_{DDJ}	—
MISC				
QUIESCE	AA7	O	NV_{DDP_K}	—
THERM0	AC7	I	NV_{DDP_K}	6
ETSEC1				
TSEC1_COL	B20	I	NV_{DDC}	—
TSEC1_CRS	B21	I	NV_{DDC}	—
TSEC1_GTX_CLK	F18	O	NV_{DDC}	3
TSEC1_RX_CLK	A22	I	NV_{DDC}	—
TSEC1_RX_DV	D21	I	NV_{DDC}	—
TSEC1_RXD[3]	C22	I	NV_{DDC}	—
TSEC1_RXD[2]	C21	I	NV_{DDC}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC1_RXD[1]	C20	I	NV_{DDC}	—
TSEC1_RXD[0]	D20	I	NV_{DDC}	—
TSEC1_RX_ER	C23	I	NV_{DDC}	—
TSEC1_TX_CLK/ TSEC1_GTX_CLK125	E23	I	NV_{DDC}	—
TSEC1_TXD[3]/ CFG_RESET_SOURCE[0]	F22	I/O	NV_{DDC}	—
TSEC1_TXD[2]/ CFG_RESET_SOURCE[1]	F21	I/O	NV_{DDC}	—
TSEC1_TXD[1]/ CFG_RESET_SOURCE[2]	E21	I/O	NV_{DDC}	—
TSEC1_TXD[0]/ CFG_RESET_SOURCE[3]	D22	I/O	NV_{DDC}	—
TSEC1_TX_EN/ LBC_PM_REF_10	F20	O	NV_{DDC}	—
TSEC1_TX_ER/ LB_POR_CFG_BOOT_ECC	E22	I/O	NV_{DDC}	7
Ethernet Mgmt				
TSEC1_MDC	A20	O	NV_{DDB}	—
TSEC1_MDIO	C19	I/O	NV_{DDB}	2
eSDHC/GTM				
SD_CLK/GPIO[16]	D7	O	NV_{DDA}	—
SD_CMD/GPIO[17]	G9	I/O	NV_{DDA}	—
$\overline{\text{SD\_CD}}$/GTM1_TIN1/ GPIO[18]	A7	I	NV_{DDA}	—
SD_WP/$\overline{\text{GTM1\_TGATE1}}$/ GPIO[19]	D8	I	NV_{DDA}	—
SD_DAT[0]/$\overline{\text{GTM1\_TOUT1}}$/ GPIO[20]	C8	I/O	NV_{DDA}	—
SD_DAT[1]/$\overline{\text{GTM1\_TOUT2}}$/ GPIO[21]	B8	I/O	NV_{DDA}	—
SD_DAT[2]/GTM1_TIN2/ GPIO[22]	A8	I/O	NV_{DDA}	—
SD_DAT[3]/$\overline{\text{GTM1\_TGATE2}}$/ GPIO[23]	B9	I/O	NV_{DDA}	—
SPI				
SPIMOSI/MSRCID4/ LSRCID4	AB5	I/O	NV_{DDP_K}	—
SPIMISO/MDVAL/LDVAL	Y6	I/O	NV_{DDP_K}	—

[illegible]

This table provides the package thermal characteristics for the 473, 19 19 mm MAPBGA.

[illegible]

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	42	°C/W	1, 2
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	27	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	35	°C/W	1, 3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W	1, 3
Junction to Board	—	$R_{\theta JB}$	17	°C/W	4
Junction to Case	—	$R_{\theta JC}$	9	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

[illegible]

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

[illegible]

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

[illegible]

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is