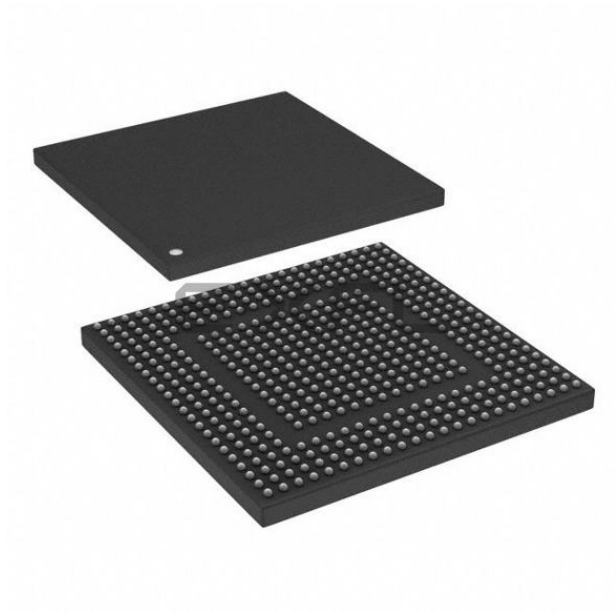

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Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8308czqafda

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ (input) to activate reset flow	32	—	$t_{SYS\_CLK\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable power and clock applied to SYS_CLK_IN	32	—	$t_{SYS\_CLK\_IN}$	—
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS\_CLK\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of PORESET	4	—	$t_{SYS\_CLK\_IN}$	—
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	2
Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$	1	—	ns	1, 2

Notes:
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN.
2. POR configuration signals consists of CFG_RESET_SOURCE[0:3].

This table provides the PLL lock times.

Table 12. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
System PLL lock time	—	100	μs	—
e300 core PLL lock time	—	100	μs	—

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ//MDM/MECC output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}		—	ps	5
266 MHz		900			
MDQ//MDM/MECC output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}		—	ps	5
266 MHz		1100			
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure shows the DDR2 SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

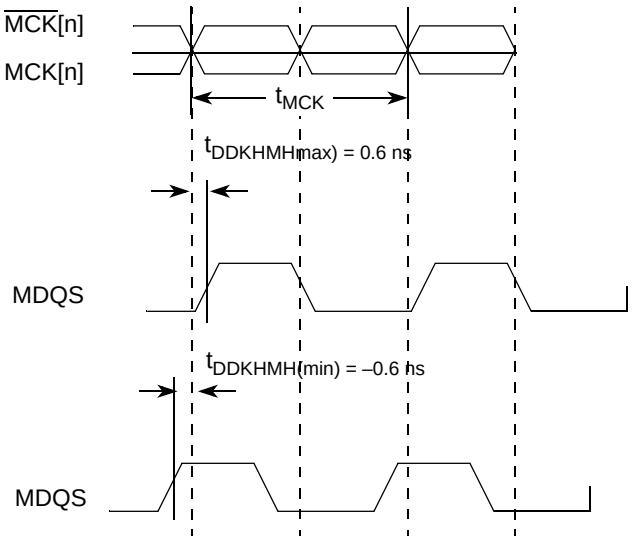


Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR2 SDRAM output timing diagram.

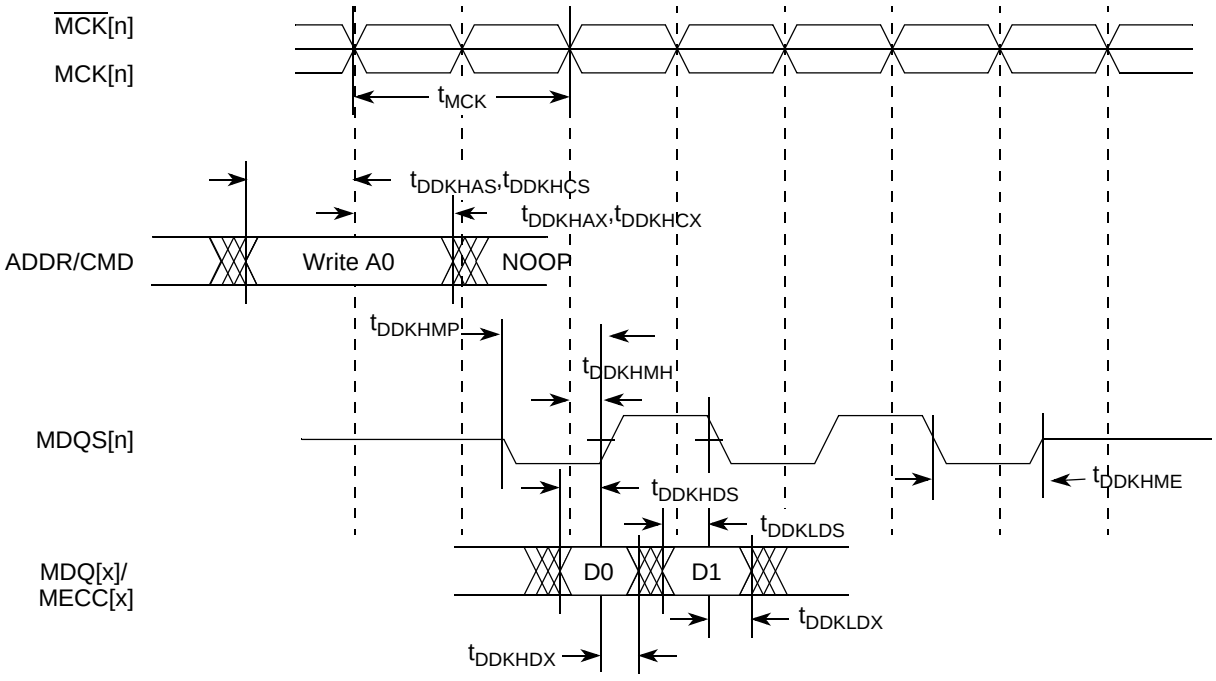


Figure 6. DDR2 SDRAM Output Timing Diagram

This figure provides the AC test load for the DDR2 bus.

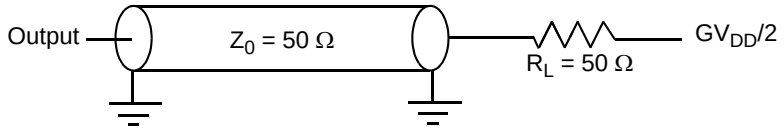


Figure 7. DDR2 AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.1	NV_{DD} + 0.3	V
Low-level input voltage NVDD	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	NV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NV_{DD})	I_{IN}	—	± 5	μA

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management. MPC8308 supports dual Ethernet controllers.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII) and reduced gigabit media independent interface (RGMII), signals except management data input/output (MDIO) and management data clock (MDC). The RGMII interface is defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RGMII interface follows the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 eTSEC DC Electrical Characteristics

All MII and RGMII drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The RGMII signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 21. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}	—		3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD}= Min	VSS	0.50	V
Input high voltage	V_{IH}	—	—	2.1	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DD}		—	40	μA
Input low current	I_{IL}	V_{IN} [1] = VSS		–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 22. RGMII DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD}= Min	VSS – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DD}		—	15	μA
Input low current	I_{IL}	V_{IN} [1] = VSS		–15	—	μA

Note:
1. V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 MII and RGMII AC Timing Specifications

The AC timing specifications for MII and RGMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 25. RGMII AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of t_{RGT} represents the RGMII receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $0.5*LV_{DD}$
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

This figure shows the RGMII AC timing and multiplexing diagrams.

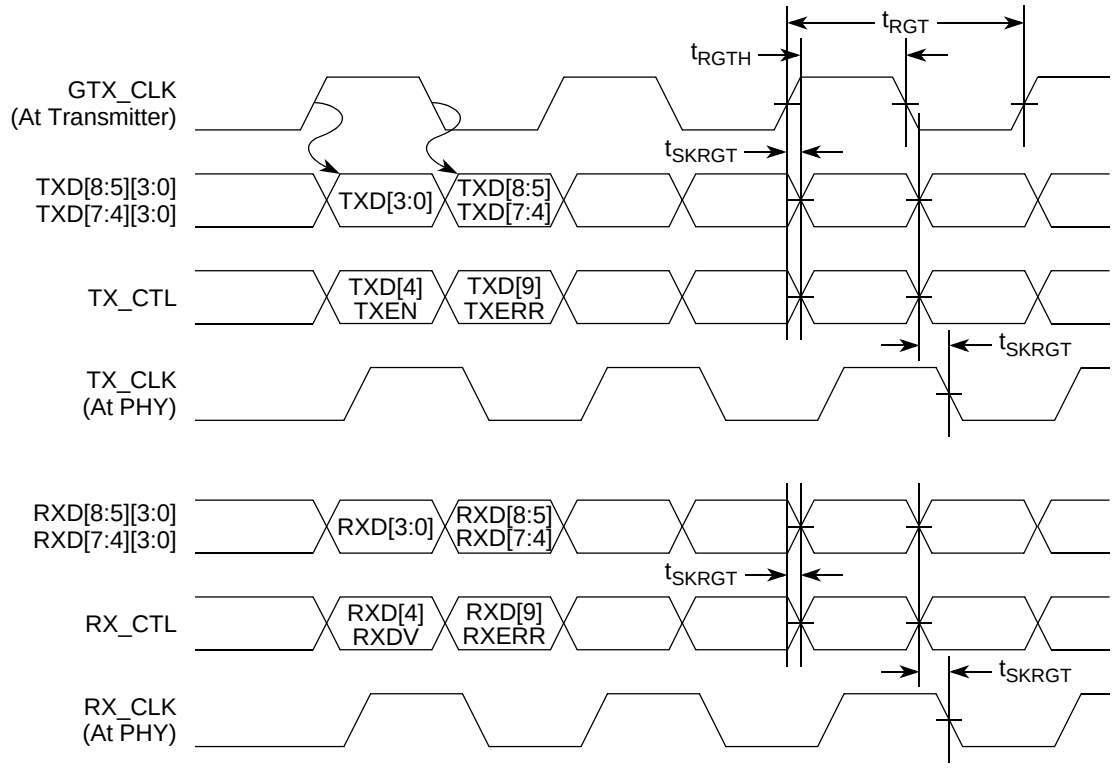


Figure 11. RGMII AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII

10.2.1 SerDes Reference Clock Receiver Characteristics

Figure 16 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XCOREVDD are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 16. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above XCOREVSS. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to XCOREVSS DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

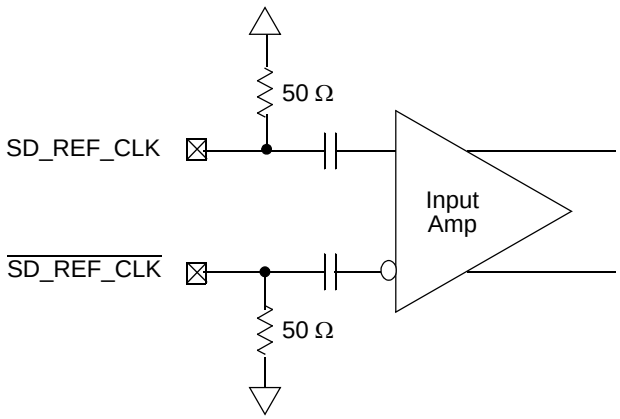


Figure 16. Receiver of SerDes Reference Clocks

10.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8308 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 10.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 17 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 18 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 19 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

Table 35. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
AC peak common mode input voltage	$V_{RX-CM-ACp}$	$V_{PEACPCMRX} = \lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$	—	—	150	mV	2
Differential return loss	$RL_{RX-DIFF}$	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively.	15	—	—	dB	4
Common mode return loss	RL_{RX-CM}	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V.	6	—	—	dB	4
DC differential input impedance	$Z_{RX-DIFF-DC}$	RX DC differential mode impedance.	80	100	120	Ω	5
DC Input Impedance	Z_{RX-DC}	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance).	40	50	60	Ω	2, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	$V_{PEEIDT} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

Figure 31 through Figure 33 show the local bus signals. In what follows, T1, T2, T3, and T4 are internal clock reference phase signals corresponding to LCCR[CLKDIV].

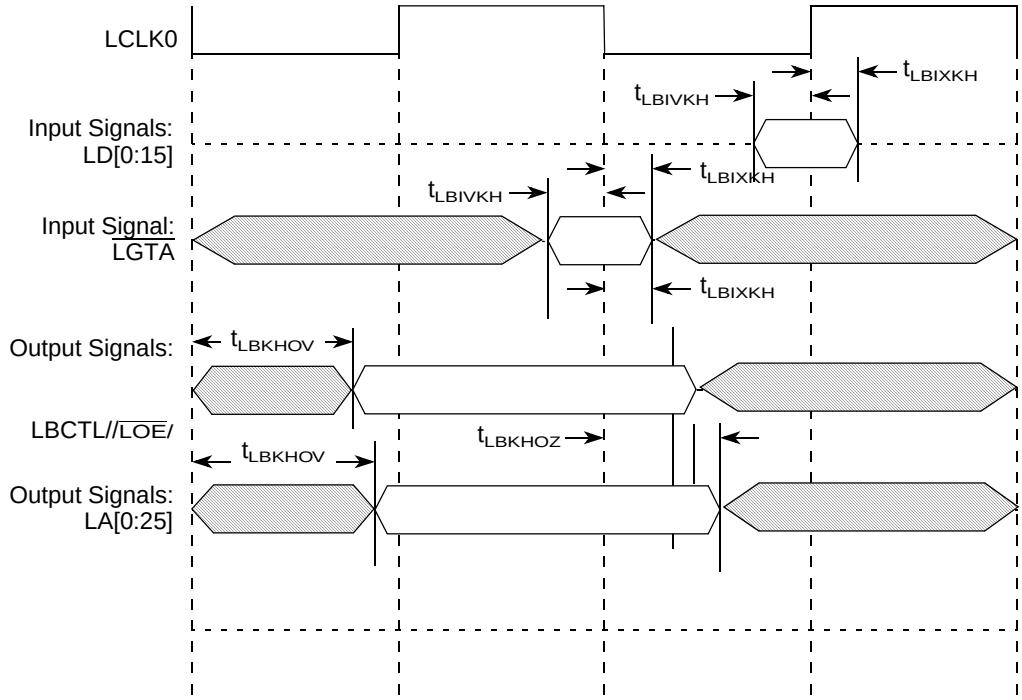


Figure 31. Local Bus Signals, Non-Special Signals Only

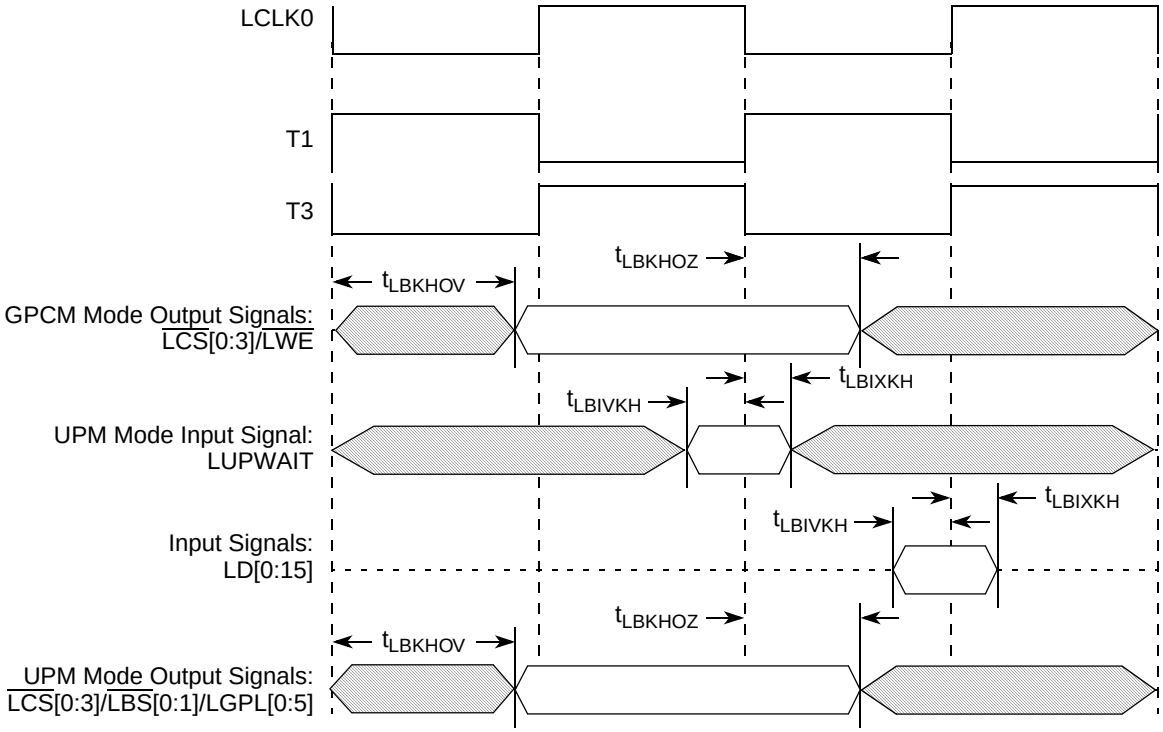


Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2

13.3.1 High Speed Output Path (Write)

This figure provides the data and command output timing diagram.

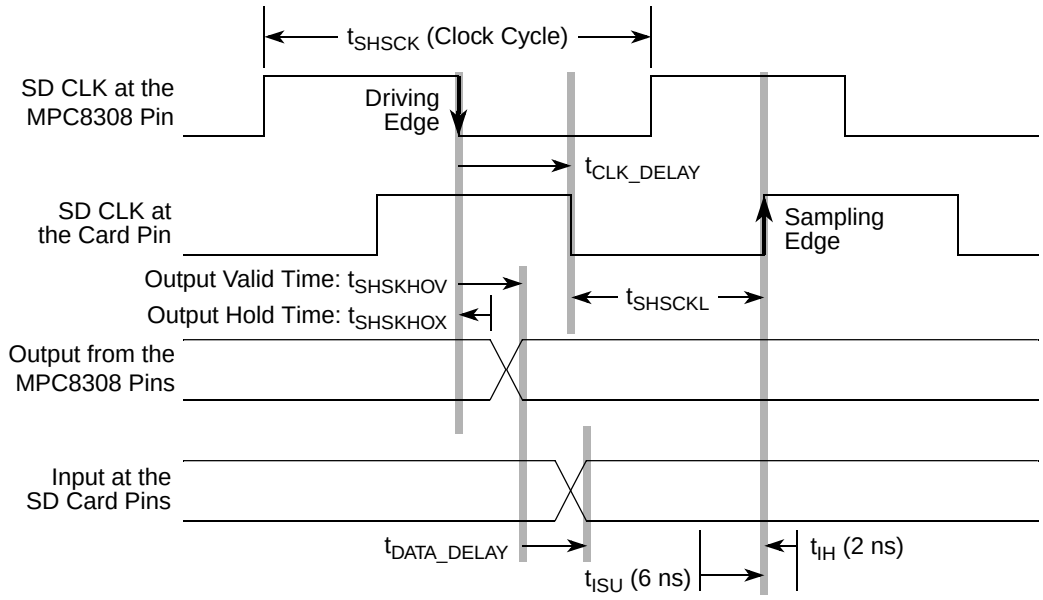


Figure 38. High Speed Output Path

13.3.2 High Speed Input Path (Read)

This figure provides the data and command input timing diagram.

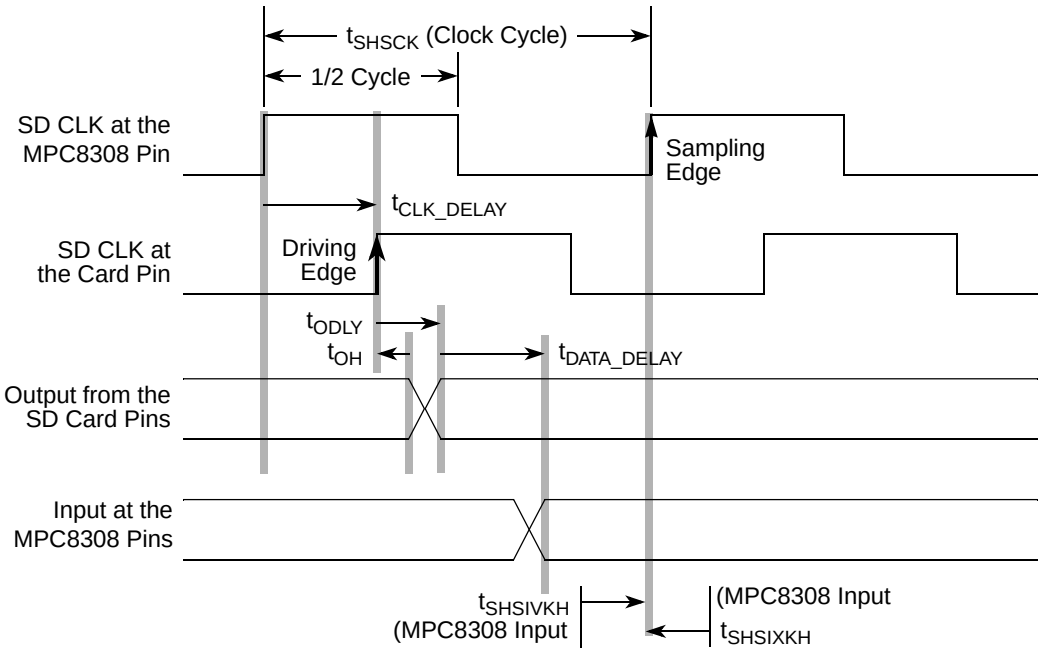
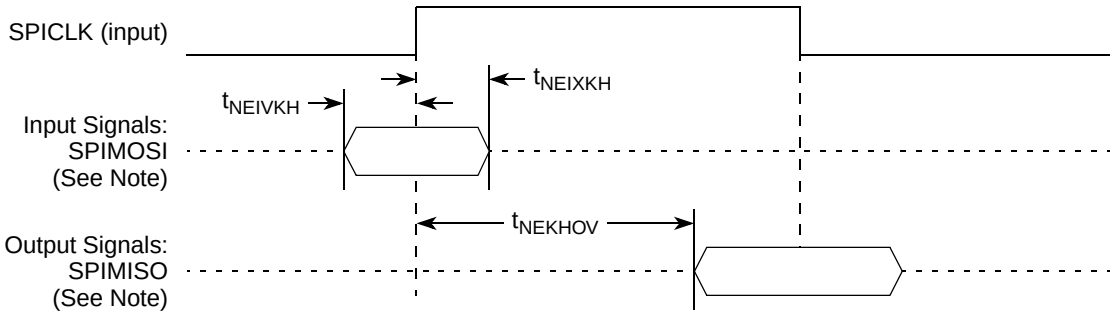


Figure 39. High Speed Input Path

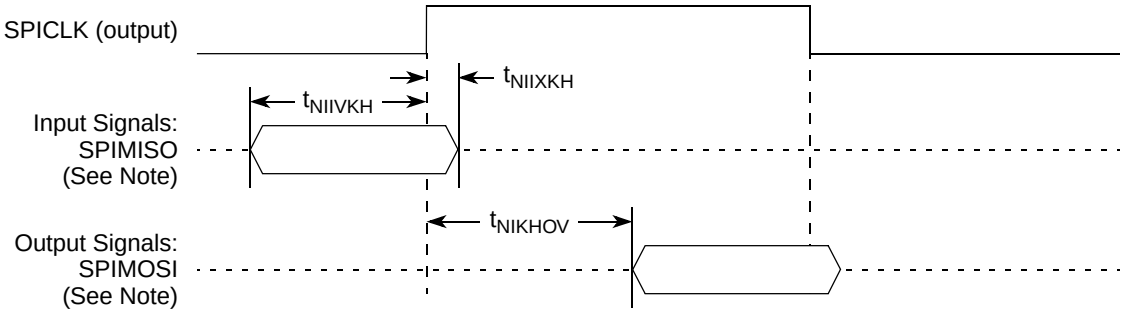
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 51. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8308 is available in a moulded array process ball grid array (MAPBGA). For information on the MAPBGA, see Section 20.1, "Package Parameters for the MPC8308 MAPBGA," and Section 20.2, "Mechanical Dimensions of the MPC8308 MAPBGA."

20.1 Package Parameters for the MPC8308 MAPBGA

The package parameters are as provided in the following list. The package type is 19 mm × 19 mm, 473 MAPBGA.

Package outline	19 mm × 19 mm
Interconnects	473
Pitch	0.80 mm
Module height (typical)	1.39 mm
Solder Balls	96.5 Sn/ 3.5Ag
Ball diameter (typical)	0.40 mm

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDQ[27]	M6	I/O	GV_{DDB}	—
MEMC_MDQ[28]	M2	I/O	GV_{DDB}	—
MEMC_MDQ[29]	M3	I/O	GV_{DDB}	—
MEMC_MDQ[30]	L2	I/O	GV_{DDB}	—
MEMC_MDQ[31]	L3	I/O	GV_{DDB}	—
MEMC_MDM[0]	AB2	O	GV_{DDA}	—
MEMC_MDM[1]	V3	O	GV_{DDA}	—
MEMC_MDM[2]	P3	O	GV_{DDB}	—
MEMC_MDM[3]	M7	O	GV_{DDB}	—
MEMC_MDM[8]	K2	O	GV_{DDB}	—
MEMC_MDQS[0]	AC3	I/O	GV_{DDA}	—
MEMC_MDQS[1]	V1	I/O	GV_{DDA}	—
MEMC_MDQS[2]	R1	I/O	GV_{DDB}	—
MEMC_MDQS[3]	M1	I/O	GV_{DDB}	—
MEMC_MDQS[8]	K1	I/O	GV_{DDB}	—
MEMC_MBA[0]	C3	O	GV_{DDB}	—
MEMC_MBA[1]	B2	O	GV_{DDB}	—
MEMC_MBA[2]	H4	O	GV_{DDB}	—
MEMC_MA0	C2	O	GV_{DDB}	—
MEMC_MA1	D2	O	GV_{DDB}	—
MEMC_MA2	D3	O	GV_{DDB}	—
MEMC_MA3	D4	O	GV_{DDB}	—
MEMC_MA4	E4	O	GV_{DDB}	—
MEMC_MA5	F4	O	GV_{DDB}	—
MEMC_MA6	E2	O	GV_{DDB}	—
MEMC_MA7	E1	O	GV_{DDB}	—
MEMC_MA8	F2	O	GV_{DDB}	—
MEMC_MA9	F3	O	GV_{DDB}	—
MEMC_MA10	C1	O	GV_{DDB}	—
MEMC_MA11	F7	O	GV_{DDB}	—
MEMC_MA12	G2	O	GV_{DDB}	—
MEMC_MA13	G3	O	GV_{DDB}	—
$\overline{\text{MEMC\_MWE}}$	D5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MRAS}}$	B4	O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MEMC\_MCAS}}$	C5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCS}}$[0]	B6	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCS}}$[1]	C6	O	GV_{DDB}	—
MEMC_MCKE	H3	O	GV_{DDB}	3
MEMC_MCK [0]	A3	O	GV_{DDB}	—
MEMC_MCK [1]	U2	O	GV_{DDB}	—
MEMC_MCK [2]	G1	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [0]	A4	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [1]	U1	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [2]	H1	O	GV_{DDB}	—
MEMC_MODT[0]	A5	O	GV_{DDB}	—
MEMC_MODT[1]	B5	O	GV_{DDB}	—
MEMC_MECC[0]	L4	I/O	GV_{DDB}	—
MEMC_MECC[1]	L6	I/O	GV_{DDB}	—
MEMC_MECC[2]	K4	I/O	GV_{DDB}	—
MEMC_MECC[3]	K3	I/O	GV_{DDB}	—
MEMC_MECC[4]	J2	I/O	GV_{DDB}	—
MEMC_MECC[5]	K6	I/O	GV_{DDB}	—
MEMC_MECC[6]	J3	I/O	GV_{DDB}	—
MEMC_MECC[7]	J6	I/O	GV_{DDB}	—
MV_{REF}	G6	I	GV_{DDB}	—
Local Bus Controller Interface				
LD0	U18	I/O	NV_{DDP_K}	8
LD1	V18	I/O	NV_{DDP_K}	8
LD2	U16	I/O	NV_{DDP_K}	8
LD3	Y20	I/O	NV_{DDP_K}	8
LD4	AA21	I/O	NV_{DDP_K}	8
LD5	AC22	I/O	NV_{DDP_K}	8
LD6	V17	I/O	NV_{DDP_K}	8
LD7	AB21	I/O	NV_{DDP_K}	8
LD8	Y19	I/O	NV_{DDP_K}	8
LD9	AA20	I/O	NV_{DDP_K}	8
LD10	Y17	I/O	NV_{DDP_K}	8

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LD11	AC21	I/O	NV_{DDP_K}	8
LD12	AB20	I/O	NV_{DDP_K}	8
LD13	V16	I/O	NV_{DDP_K}	8
LD14	AA19	I/O	NV_{DDP_K}	8
LD15	AC17	I/O	NV_{DDP_K}	8
LA0	AC20	O	NV_{DDP_K}	—
LA1	Y16	O	NV_{DDP_K}	—
LA2	U15	O	NV_{DDP_K}	—
LA3	V15	O	NV_{DDP_K}	—
LA4	AA18	O	NV_{DDP_K}	—
LA5	AA17	O	NV_{DDP_K}	—
LA6	AC19	O	NV_{DDP_K}	—
LA7	AA16	O	NV_{DDP_K}	—
LA8	AB18	O	NV_{DDP_K}	—
LA9	AC18	O	NV_{DDP_K}	—
LA10	V14	O	NV_{DDP_K}	—
LA11	AB17	O	NV_{DDP_K}	—
LA12	AA15	O	NV_{DDP_K}	—
LA13	AC16	O	NV_{DDP_K}	—
LA14	Y14	O	NV_{DDP_K}	—
LA15	AC15	O	NV_{DDP_K}	—
LA16	U13	O	NV_{DDP_K}	—
LA17	V13	O	NV_{DDP_K}	—
LA18	Y13	O	NV_{DDP_K}	—
LA19	AB15	O	NV_{DDP_K}	—
LA20	AA14	O	NV_{DDP_K}	—
LA21	AB14	O	NV_{DDP_K}	—
LA22	U12	O	NV_{DDP_K}	—
LA23	V12	O	NV_{DDP_K}	—
LA24	Y12	O	NV_{DDP_K}	—
LA25	AC14	O	NV_{DDP_K}	—
$\overline{\text{LCS}}$[0]	AA13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[1]	AB13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[2]	AA12	O	NV_{DDP_K}	4

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{LCS}}$[3]	Y11	O	NV_{DDP_K}	4
$\overline{\text{LWE}}$[0] /$\overline{\text{LFWE}}$0/$\overline{\text{LBS}}$0	AB11	O	NV_{DDP_K}	—
$\overline{\text{LWE}}$[1]/$\overline{\text{LBS}}$1	AC11	O	NV_{DDP_K}	—
LBCTL	U11	O	NV_{DDP_K}	—
LGPL0/LFCLE	Y10	O	NV_{DDP_K}	—
LGPL1/LFALE	AA10	O	NV_{DDP_K}	—
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AB10	O	NV_{DDP_K}	4
LGPL3/$\overline{\text{LFWP}}$	AC10	O	NV_{DDP_K}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LFRB	AB9	I/O	NV_{DDP_K}	4
LGPL5	Y9	O	NV_{DDP_K}	—
LCLK0	AC12	O	NV_{DDP_K}	—
DUART				
UART_SOUT1/MSRCID0/ LSRCID0	C17	O	NV_{DDB}	—
UART_SIN1/MSRCID1/ LSRCID1	B18	I/O	NV_{DDB}	—
UART_SOUT2/MSRCID2/ LSRCID2	D17	O	NV_{DDB}	—
UART_SIN2/MSRCID3/ LSRCID3	D18	I/O	NV_{DDB}	—
PEX PHY				
TXA	C14	O	XPADVDD	—
$\overline{\text{TXA}}$	C15	O	XPADVDD	—
RXA	A13	I	XCOREVDD	—
$\overline{\text{RXA}}$	B13	I	XCOREVDD	—
SD_IMP_CAL_RX	A15	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	C12	I	XCOREVDD	—
SD_REF_CLK	D12	I	XCOREVDD	—
SD_PLL_TPD	F13	O	—	—
SD_IMP_CAL_TX	A11	I	XPADVDD	—
SD_PLL_TPA_ANA	F11	O	—	—
SDAVDD_0	G12	I	—	—
SDAVSS_0	F12	I	—	—
I^2C interface				
IIC_SDA1	C9	I/O	NV_{DDA}	2

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPICLK	AA5	I/O	NV_{DDP_K}	—
SPISEL	AB4	I	NV_{DDP_K}	—
GPIO/ETSEC2				
GPIO[0]/TSEC2_COL	G21	I/O	NV_{DDF}	—
GPIO[1]/TSEC2_TX_ER	K23	I/O	NV_{DDF}	—
GPIO[2]/TSEC2_GTX_CLK	H18	I/O	NV_{DDF}	—
GPIO[3]/TSEC2_RX_CLK	G23	I/O	NV_{DDF}	—
GPIO[4]/TSEC2_RX_DV	J18	I/O	NV_{DDF}	—
GPIO[5]/TSEC2_RXD3	J20	I/O	NV_{DDF}	—
GPIO[6]/TSEC2_RXD2	H22	I/O	NV_{DDF}	—
GPIO[7]/TSEC2_RXD1	H21	I/O	NV_{DDF}	—
GPIO[8]/TSEC2_RXD0	H20	I/O	NV_{DDF}	—
GPIO[9]/TSEC2_RX_ER	J21	I/O	NV_{DDF}	—
GPIO[10]/TSEC2_TX_CLK/ TSEC2_GTX_CLK125	J23	I/O	NV_{DDF}	—
GPIO[11]/TSEC2_TXD3	K22	I/O	NV_{DDF}	—
GPIO[12]/TSEC2_TXD2	K20	I/O	NV_{DDF}	—
GPIO[13]/TSEC2_TXD1	K18	I/O	NV_{DDF}	—
GPIO[14]/TSEC2_TXD0	J17	I/O	NV_{DDF}	—
GPIO[15]/TSEC2_TX_EN	K21	I/O	NV_{DDF}	—
USB/IEEE1588/GTM				
USBDR_PWR_FAULT	P20	I	NV_{DDH}	—
USBDR_CLK	R23	I	NV_{DDH}	—
USBDR_DIR	R21	I	NV_{DDH}	—
USBDR_NXT	P18	I	NV_{DDH}	—
USBDR_TXDRXD0	T22	I/O	NV_{DDH}	—
USBDR_TXDRXD1	T21	I/O	NV_{DDH}	—
USBDR_TXDRXD2	U23	I/O	NV_{DDH}	—
USBDR_TXDRXD3	U22	I/O	NV_{DDH}	—
USBDR_TXDRXD4	T20	I/O	NV_{DDH}	—
USBDR_TXDRXD5	R18	I/O	NV_{DDH}	—
USBDR_TXDRXD6	V23	I/O	NV_{DDH}	—
USBDR_TXDRXD7	V22	I/O	NV_{DDH}	—
USBDR_PCTL0	R17	O	NV_{DDH}	—

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the device

23.1 System Clocking

The device includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 21.2, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.3, “Core PLL Configuration.”

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} for core PLL and AV_{DD2} for the platform PLL). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low pass filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 54, one to each of the two AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs’ resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

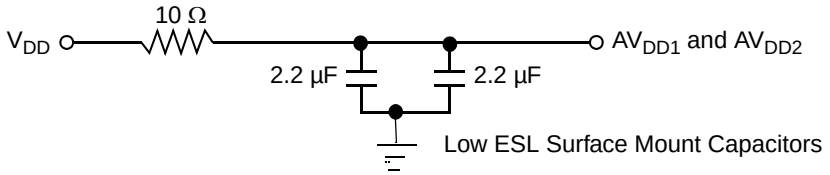
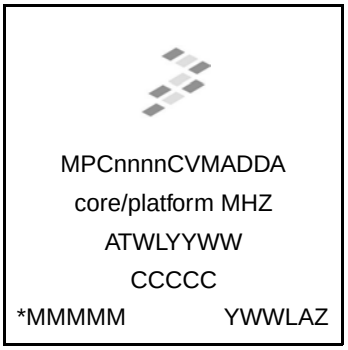


Figure 54. PLL Power Supply Filter Circuit

24.2 Part Marking

Parts are marked as in the example shown in this figure.



PBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 56. Freescale Part Marking for PBGA Devices

This table lists the SVR settings.

Table 62. SVR Settings

Device	Package	SVR
MPC8308	MAPBGA	0x8101 _0110

Note: PVR = 8085_0020 for the device.