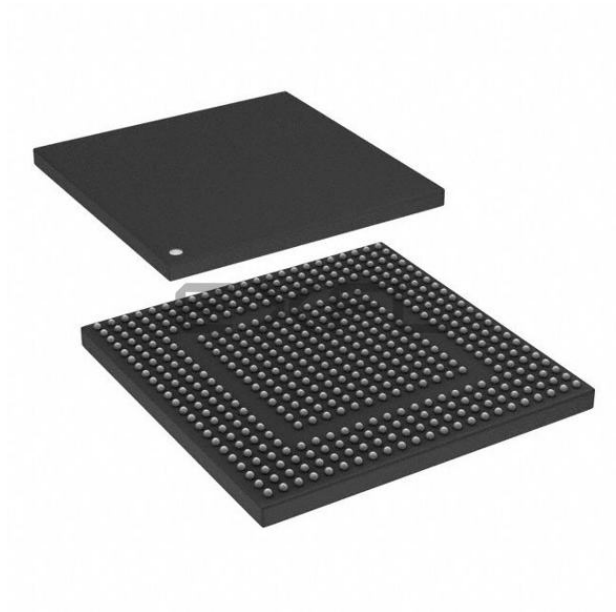

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8308czqagd

2.1.1 Absolute Maximum Ratings

This table lists the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1}, AV_{DD2}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.9	V	—
Local bus, DUART, system control and power management, eSDHC, I^2C, USB, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage		NV_{DD}	–0.3 to 3.6	V	7
SerDes PHY		$XCOREV_{DD}$, $XPADV_{DD}$, $SDAV_{DD}$	–0.3 to 1.26	V	—
eTSEC I/O Voltage		LV_{DD1}, LV_{DD2}	–0.3 to 2.75 or –0.3 to 3.6	V	6, 8
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	eTSEC	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5,8
	Local bus, DUART, system control and power management, eSDHC, I^2C, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage	OV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	3, 5,7
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M, L, O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2
6. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
7. NV_{DD} here refers to NV_{DDA}, NV_{DDB},NV_{DDG}, NV_{DDH}, NV_{DDJ}, NV_{DDP_K} from the ball map.
8. LV_{DD1} here refers to NV_{DDC} and LV_{DD2} refers to NV_{DDF} from the ball map

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.45	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.45	—	V	—

This table provides input AC timing specifications for the DDR2 SDRAM interface.

Table 17. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 1.8± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC 266 MHz	t_{CISKEW}	–875	875	ps	1, 2,3

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ or MECC signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = +/–(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Memory controller ODT value of 150 Ω is recommended

This figure illustrates the DDR2 input timing diagram showing the t_{DISKEW} timing parameter.

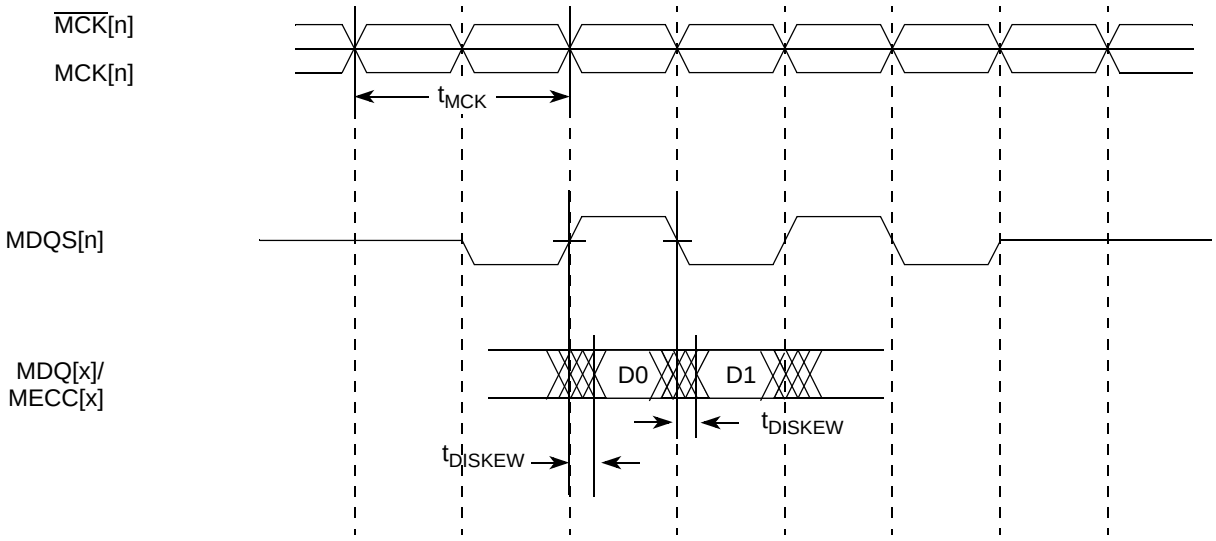


Figure 4. Timing Diagram for t_{DISKEW}

6.2.2 DDR2 SDRAM Output AC Timing Specifications

Table 18. DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}		—	ns	3
266 MHz		2.9			
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}		—	ns	3
266 MHz		2.33			
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}		—	ns	3
266 MHz		2.5			
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}		—	ns	3
266 MHz		3.15			
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4

This figure provides the AC test load for the DDR2 bus.

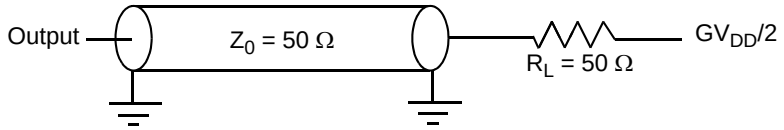


Figure 7. DDR2 AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.1	NV_{DD} + 0.3	V
Low-level input voltage NVDD	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	NV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NV_{DD})	I_{IN}	—	± 5	μA

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management. MPC8308 supports dual Ethernet controllers.

- **Common Mode Voltage, V_{cm}**

  The common mode voltage is equal to one-half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{TXn} + V_{\overline{TXn}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

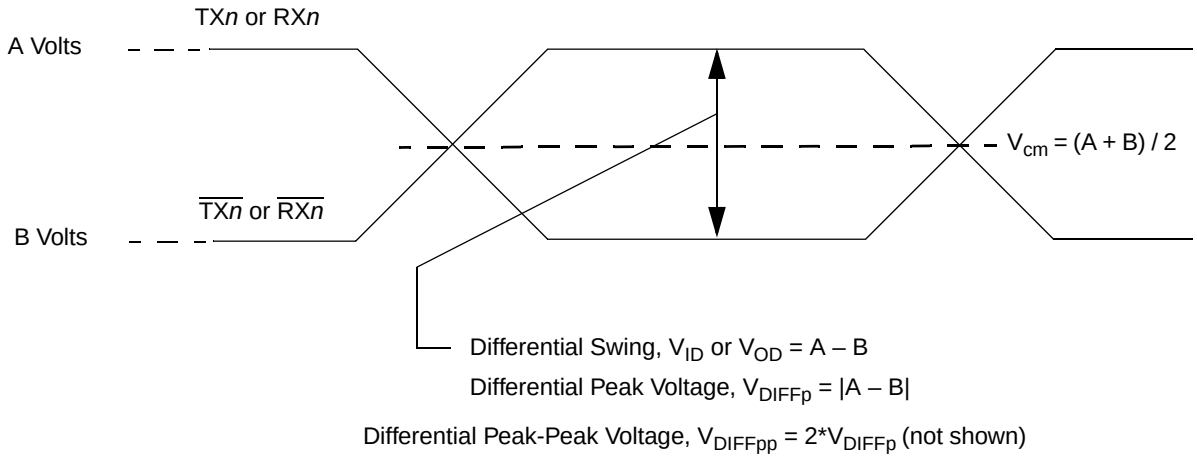


Figure 15. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

10.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for PCI Express.

The following sections describe the SerDes reference clock requirements and some application information.

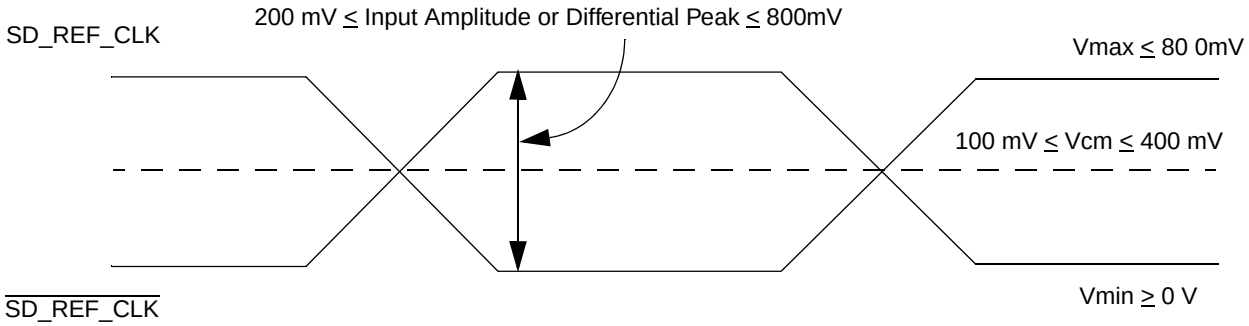


Figure 17. Differential Reference Clock Input DC Requirements (External DC-Coupled)

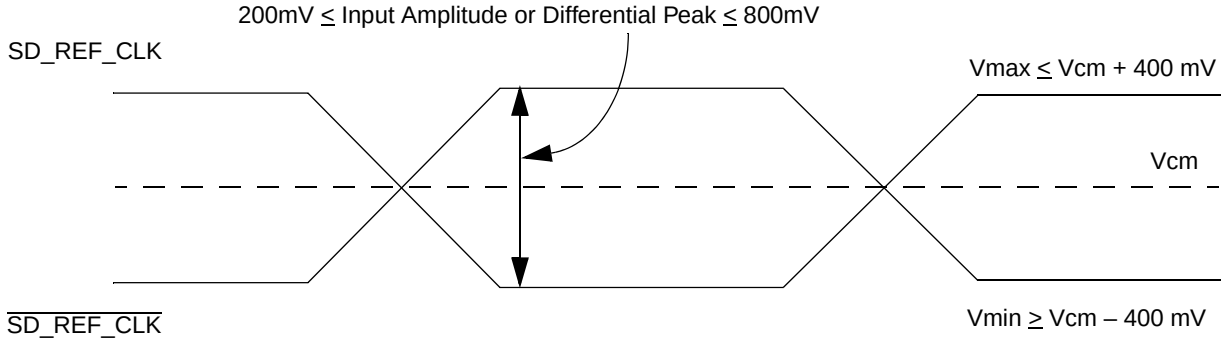


Figure 18. Differential Reference Clock Input DC Requirements (External AC-Coupled)

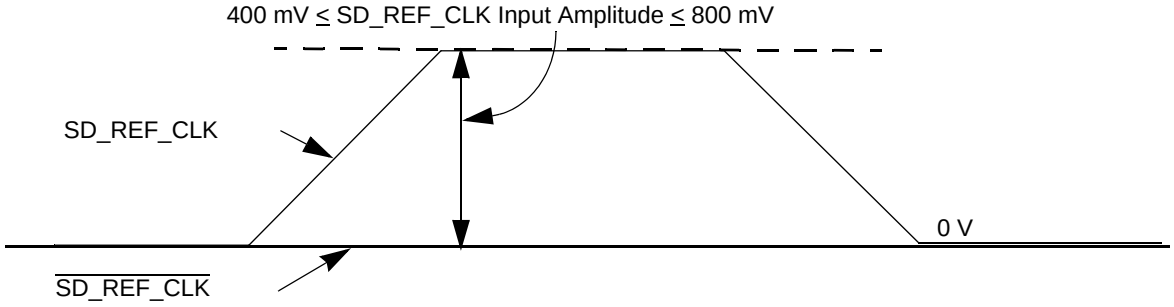


Figure 19. Single-Ended Reference Clock Input DC Requirements

10.2.3 Interfacing with Other Differential Signaling Levels

With on-chip termination to XCOREVSS, the differential reference clocks inputs are high-speed current steering logic (HCSL) compatible and DC coupled.

Many other low voltage differential type outputs like low-voltage differential signaling (LVDS) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100–400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 20–Figure 23 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very much possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8308 SerDes reference clock receiver requirement provided in this document.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8308 SerDes reference clock input's DC requirement.

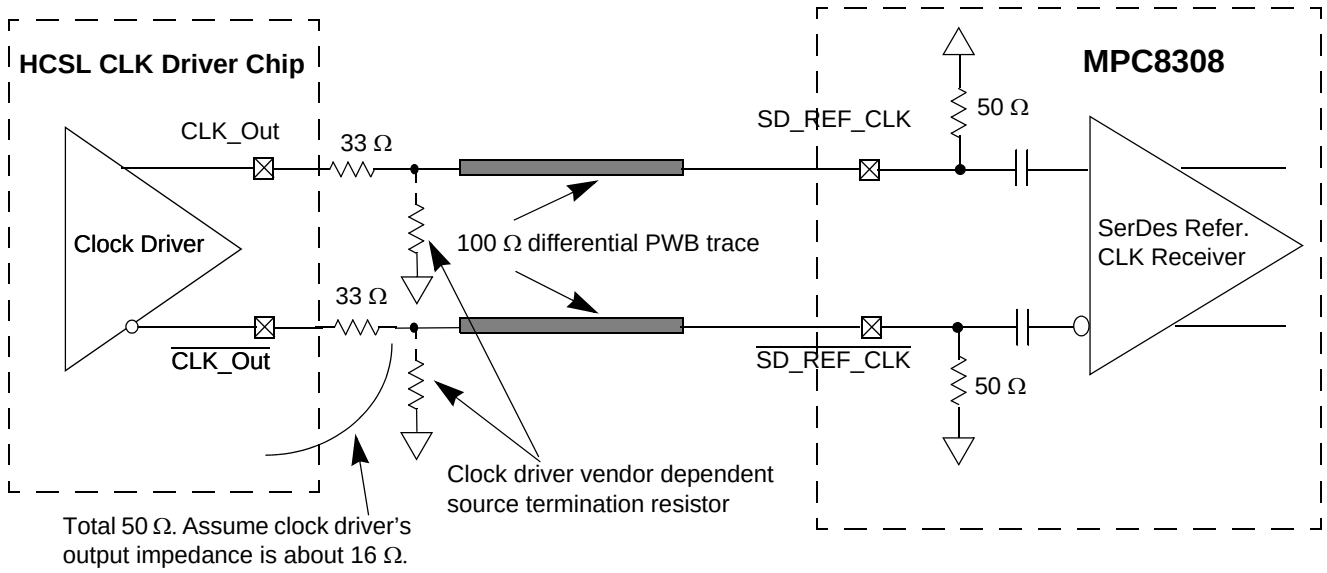


Figure 20. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8308's SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

11.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

11.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer please use the *PCI Express Base Specification*, Rev. 1.0a.

11.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 34. Differential Transmitter (TX) Output Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Unit interval	UI	Each U_{PETX} is 400 ps ± 300 ppm. U_{PETX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	$V_{PEDPPTX} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.8	—	1.2	V	2
De-Emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	Ratio of the $V_{PEDPPTX}$ of the second and following bits after a transition divided by the $V_{PEDPPTX}$ of the first bit after a transition.	–3.0	–3.5	–4.0	dB	2
Minimum TX eye width	T_{TX-EYE}	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - U_{PEEWTX} = 0.3$ UI.	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPTX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.15	UI	2, 3
D+/D- TX output rise/fall time	$T_{TX-RISE}$, $T_{TX-FALL}$	—	0.125	—	—	UI	2, 5
RMS AC peak common mode output voltage	$V_{TX-CM-ACp}$	$V_{PEACPCMTX} = RMS(\|V_{TXD+} + V_{TXD-}\|/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$	—	—	20	mV	2

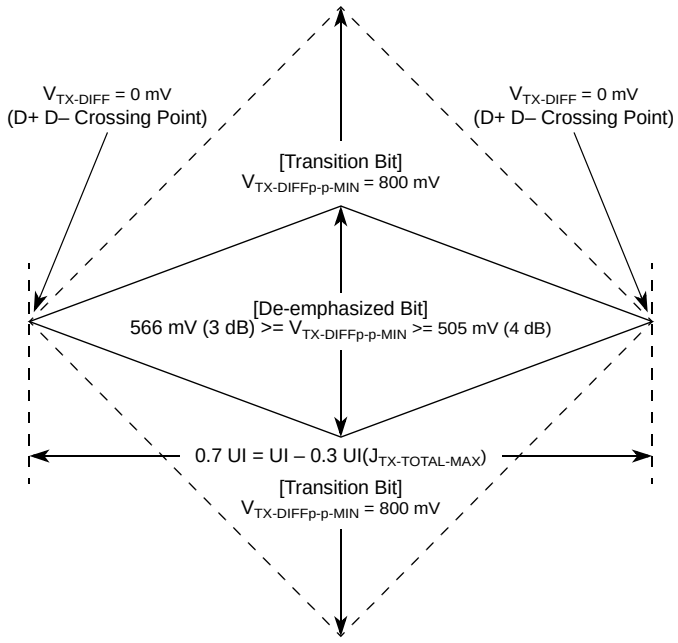


Figure 27. Minimum Transmitter Timing and Voltage Output Compliance Specifications

11.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 35. Differential Receiver (RX) Input Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Unit interval	UI	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{RX-DIFFp-p}$	$V_{PEDPPRX} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	—	1.200	V	2
Minimum receiver eye width	T_{RX-EYE}	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - U_{PEEWRX} = 0.6$ UI.	0.4	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPRX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.3	UI	2, 3, 7

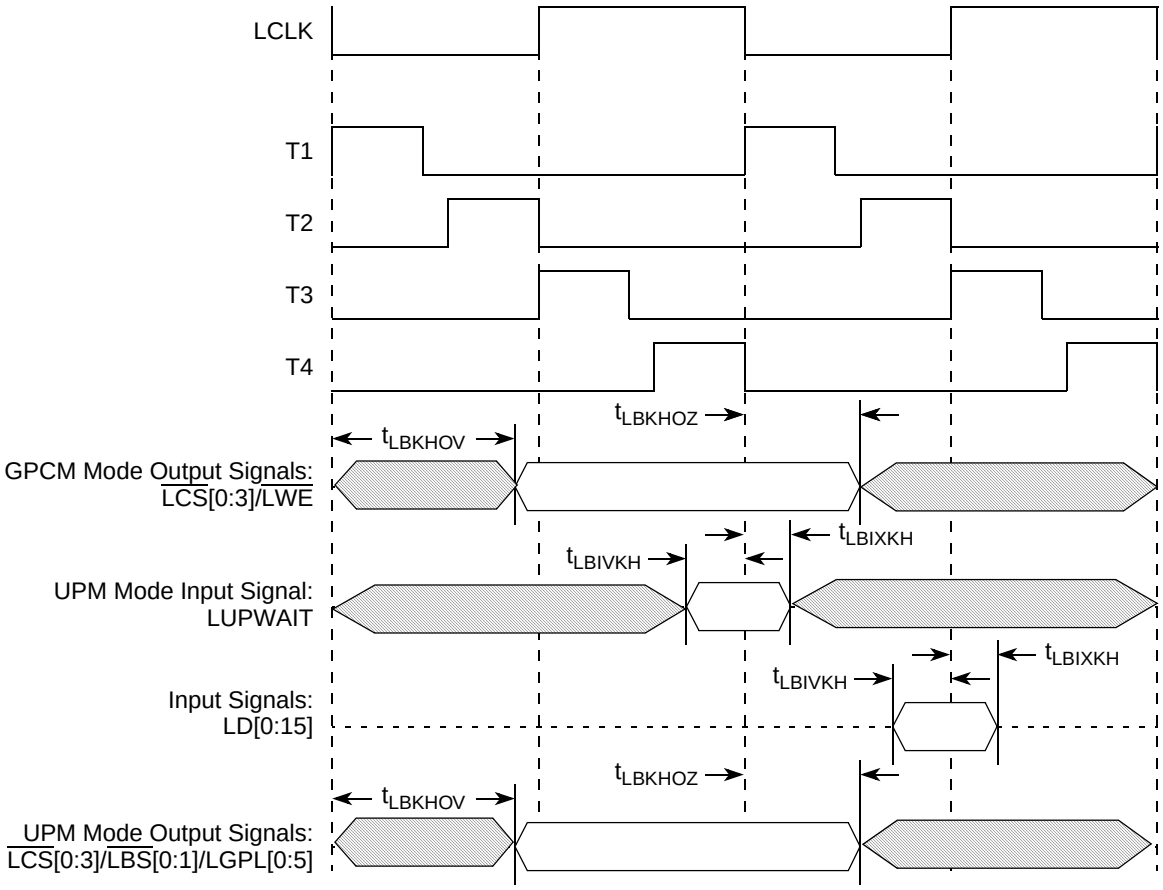


Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4

13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SD/MMC/SDIO) interface of the MPC8308.

The eSDHC controller always uses the falling edge of the SD_CLK in order to drive the SD_DAT[0:3]/CMD as outputs and rising edge to sample the SD_DAT[0:3], CMD, $\overline{\text{CD}}$ and WP as inputs. This behavior is true for both full and high speed modes.

13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device, compatible with SDHC specifications. The eSDHC NV_{DD} range is between 3.0 V and 3.6 V.

Table 38. eSDHC interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

Table 38. eSDHC interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V

13.2 eSDHC AC Timing Specifications (Full Speed Mode)

This section describes the AC electrical specifications for the eSDHC (SD/MMC) interface of the device. This table provides the eSDHC AC timing specifications for full speed mode as defined in Figure 35 and Figure 36.

Table 39. eSDHC AC Timing Specifications for Full Speed Mode

At recommended operating conditions NV_{DD} = 3.3 V ± 300 mV.

Parameter	Symbol [1]	Min	Max	Unit	Notes
SD_CLK clock frequency—full speed mode	f_{SFSCK}	0	25	MHz	—
SD_CLK clock cycle	t_{SFSCK}	40	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	kHz	—
SD_CLK clock low time	t_{SFSCKL}	15	—	ns	2
SD_CLK clock high time	t_{SFSCKH}	15	—	ns	2
SD_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	5	ns	2
Input setup times: SD_CMD, SD_DATx to SD_CLK	$t_{SFSIVKH}$	3	—	ns	2
Input hold times: SD_CMD, SD_DATx to SD_CLK	$t_{SFSIXKH}$	2	—	ns	2
Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOV}$	—	3	ns	2
Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOX}$	–3	—	—	—
SD card input setup	t_{ISU}	5	—	ns	3
SD card input hold	t_{IH}	5	—	ns	3
SD card output valid	t_{ODLY}	—	14	ns	3
SD card output hold	t_{OH}	0	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

17 GPIO

This section describes the DC and AC electrical specifications for the GPIO of MPC8308

17.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO.

Table 47. GPIO DC Electrical Characteristic

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

17.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 48. GPIO Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

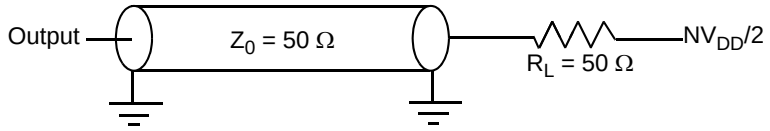


Figure 48. GPIO AC Test Load

2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

20.3 Pinout Listings

This table provides the pin-out listing for the MPC8308, MAPBGA package.

Table 53. MPC8308 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	V6	I/O	GV_{DDA}	—
MEMC_MDQ[1]	Y4	I/O	GV_{DDA}	—
MEMC_MDQ[2]	AB3	I/O	GV_{DDA}	—
MEMC_MDQ[3]	AA3	I/O	GV_{DDA}	—
MEMC_MDQ[4]	AA2	I/O	GV_{DDA}	—
MEMC_MDQ[5]	AA1	I/O	GV_{DDA}	—
MEMC_MDQ[6]	W4	I/O	GV_{DDA}	—
MEMC_MDQ[7]	Y2	I/O	GV_{DDA}	—
MEMC_MDQ[8]	W3	I/O	GV_{DDA}	—
MEMC_MDQ[9]	W1	I/O	GV_{DDA}	—
MEMC_MDQ[10]	Y1	I/O	GV_{DDA}	—
MEMC_MDQ[11]	W2	I/O	GV_{DDA}	—
MEMC_MDQ[12]	U4	I/O	GV_{DDA}	—
MEMC_MDQ[13]	U3	I/O	GV_{DDA}	—
MEMC_MDQ[14]	V4	I/O	GV_{DDA}	—
MEMC_MDQ[15]	U6	I/O	GV_{DDA}	—
MEMC_MDQ[16]	T3	I/O	GV_{DDB}	—
MEMC_MDQ[17]	T2	I/O	GV_{DDB}	—
MEMC_MDQ[18]	R4	I/O	GV_{DDB}	—
MEMC_MDQ[19]	R3	I/O	GV_{DDB}	—
MEMC_MDQ[20]	P4	I/O	GV_{DDB}	—
MEMC_MDQ[21]	N6	I/O	GV_{DDB}	—
MEMC_MDQ[22]	P2	I/O	GV_{DDB}	—
MEMC_MDQ[23]	P1	I/O	GV_{DDB}	—
MEMC_MDQ[24]	N4	I/O	GV_{DDB}	—
MEMC_MDQ[25]	N3	I/O	GV_{DDB}	—
MEMC_MDQ[26]	N2	I/O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LD11	AC21	I/O	NV_{DDP_K}	8
LD12	AB20	I/O	NV_{DDP_K}	8
LD13	V16	I/O	NV_{DDP_K}	8
LD14	AA19	I/O	NV_{DDP_K}	8
LD15	AC17	I/O	NV_{DDP_K}	8
LA0	AC20	O	NV_{DDP_K}	—
LA1	Y16	O	NV_{DDP_K}	—
LA2	U15	O	NV_{DDP_K}	—
LA3	V15	O	NV_{DDP_K}	—
LA4	AA18	O	NV_{DDP_K}	—
LA5	AA17	O	NV_{DDP_K}	—
LA6	AC19	O	NV_{DDP_K}	—
LA7	AA16	O	NV_{DDP_K}	—
LA8	AB18	O	NV_{DDP_K}	—
LA9	AC18	O	NV_{DDP_K}	—
LA10	V14	O	NV_{DDP_K}	—
LA11	AB17	O	NV_{DDP_K}	—
LA12	AA15	O	NV_{DDP_K}	—
LA13	AC16	O	NV_{DDP_K}	—
LA14	Y14	O	NV_{DDP_K}	—
LA15	AC15	O	NV_{DDP_K}	—
LA16	U13	O	NV_{DDP_K}	—
LA17	V13	O	NV_{DDP_K}	—
LA18	Y13	O	NV_{DDP_K}	—
LA19	AB15	O	NV_{DDP_K}	—
LA20	AA14	O	NV_{DDP_K}	—
LA21	AB14	O	NV_{DDP_K}	—
LA22	U12	O	NV_{DDP_K}	—
LA23	V12	O	NV_{DDP_K}	—
LA24	Y12	O	NV_{DDP_K}	—
LA25	AC14	O	NV_{DDP_K}	—
$\overline{\text{LCS}}$[0]	AA13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[1]	AB13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[2]	AA12	O	NV_{DDP_K}	4

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
USBDR_PCTL1	U20	O	NV_{DDH}	—
USBDR_STP	V21	O	NV_{DDH}	—
TSEC_TMR_CLK/ GPIO[8]	W23	I	NV_{DDH}	—
GTM1_TOUT3/ GPIO[9]	T18	O	NV_{DDH}	—
GTM1_TOUT4/ GPIO[10]	V20	O	NV_{DDH}	—
TSEC_TMR_TRIG1/ GPIO[11]	W21	I	NV_{DDH}	—
TSEC_TMR_TRIG2/ GPIO[12]	Y21	I	NV_{DDH}	—
TSEC_TMR_GCLK	L17	O	NV_{DDG}	—
TSEC_TMR_PP1	L18	O	NV_{DDG}	—
TSEC_TMR_PP2	L21	O	NV_{DDG}	—
TSEC_TMR_PP3/ GPIO[13]	L22	O	NV_{DDG}	—
TSEC_TMR_ALARM1	L23	O	NV_{DDG}	—
TSEC_TMR_ALARM2/ GPIO[14]	M23	O	NV_{DDG}	—
GPIO[7]	M22	IO	—	—
TSEC2_CRS/ GPIO[0]	M21	IO	NV_{DDG}	—
TSEC2_TMR_RX_ESFD/ GPIO[1]	M18	O	NV_{DDG}	—
TSEC2_TMR_TX_ESFD/ GPIO[2]	M20	O	NV_{DDG}	—
TSEC1_TMR_RX_ESFD/ GPIO[3]	N23	O	NV_{DDG}	—
TSEC1_TMR_TX_ESFD/ GPIO[4]	N21	O	NV_{DDG}	—
GTM1_TGATE3	N20	I	NV_{DDG}	—
GTM1_TIN4	N18	I	NV_{DDG}	—
GTM1_TGATE4/ GPIO[15]	P23	I	NV_{DDG}	—
GTM1_TIN3	P22	I	NV_{DDG}	—
GPIO[5]	N17	IO	NV_{DDH}	—
GPIO[6]	P21	IO	NV_{DDH}	—
Power and Ground Supplies				
AV_{DD1}	R6	I	—	—
AV_{DD2}	V10	I	—	—
NC, No Connection	B11, B16, D16	—	—	—

Table 53. MPC8308 Pinout Listing (continued)

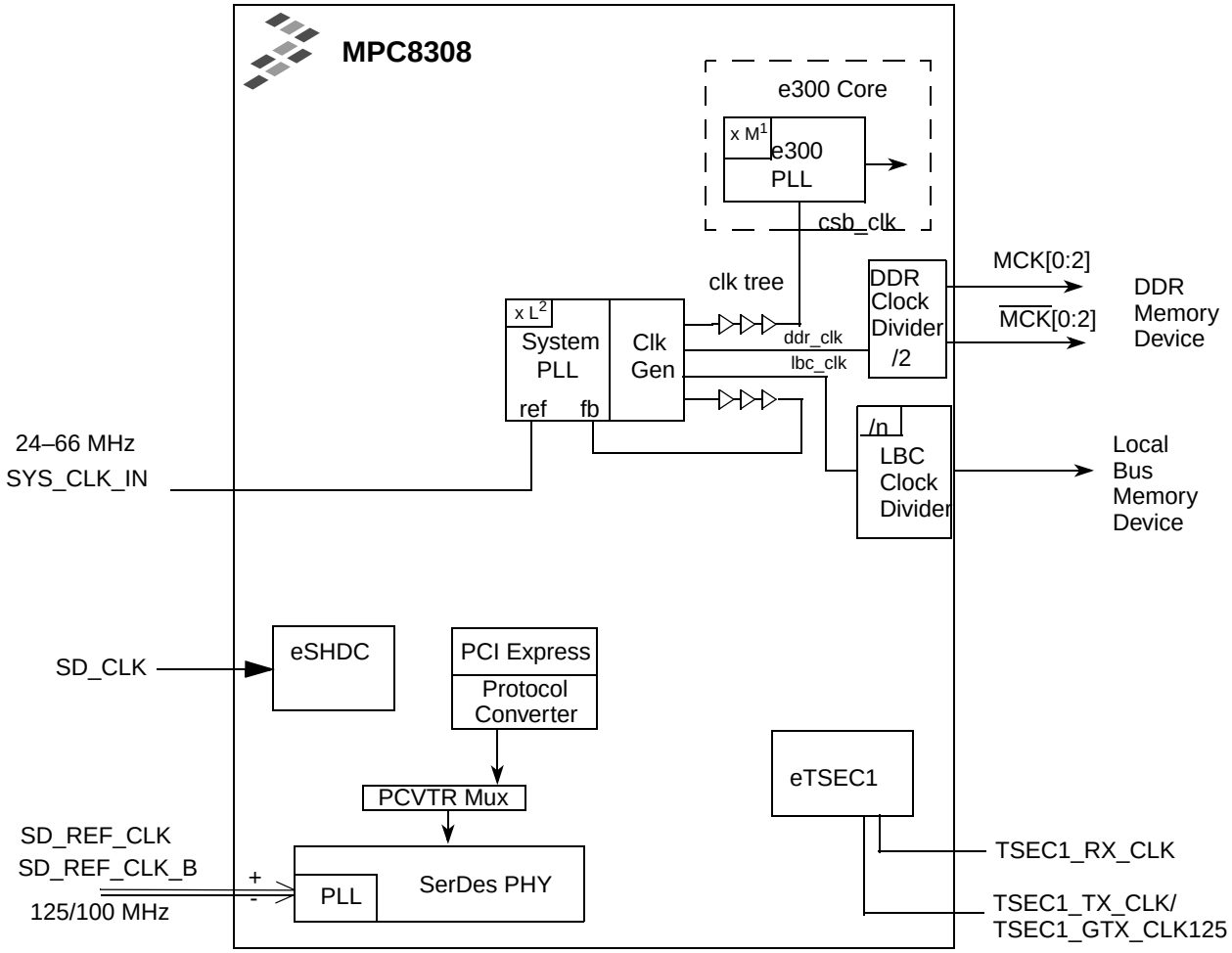
Signal	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	Y23, H8, H9, H10, H14, H15, H16, J8, J16, K8, K16, L8, L16, M8, M16, N8, N16, P8, P16, R8, R16, T8, T9, T10, T11, T12, T13, T14, T15, T16	I	—	—
VSS	A2, A21, B1, B19, B23, C4, C16, D6, D19, E3, F8, F15, F17, F23, G7, G8, G10, G15, G16, G17, G20, H2, H6, H7, H17, H23, J7, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, K15, L1, L7, L9, L10, L11, L12, L13, L14, L15, L20, M4, M9, M10, M11, M12, M13, M14, M15, N9, N10, N11, N12, N13, N14, N15, P6, P7, P9, P10, P11, P12, P13, P14, P15, R2, R7, R9, R10, R11, R12, R13, R14, R15, R22, T6, T7, U8, U17, U21, V2, V7, V9, V11, W20, Y8, Y15, AA4, AB1, AB6, AB12, AB19, AC2, AC9, AC23	I	—	—
NV_{DDA}	B7, B10, C7, D9, F9	I	—	—
NV_{DDB}	A16, A19, C18	I	—	—
NV_{DDC}	A23, B22, D23, E20, G18	I	—	—
NV_{DDF}	G22, J22, K17	I	—	—
NV_{DDG}	M17, N22	I	—	—
NV_{DDH}	P17, R20, T17, T23, W22, Y22	I	—	—
NV_{DDJ}	AB23, AA22	I	—	—
NV_{DDP_K}	U10, U14, Y5, Y18, AA11, AB8, AB16, AB22, AC4, AC13	I	—	—
GV_{DD}	A1, A6, B3, D1, F1, F6, G4, J1, J4, K7, N1, N7, T1, T4, U7, Y3, AC1	I	—	—
XPADVDD	D15, F10, F14	I	—	—
XPADVSS	A10, B15, D14, G13, G14, H12	I	—	—
XCOREVDD	A14, B12, C13	I	—	—
XCOREVSS	A12, B14, C11, D11, D13, G11, H11, H13	I	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. This pin has weak internal pull-up that is always enabled. 5. This pin must always be tied to VSS.
6. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
7. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a buffer released to high impedance is needed.
8. This pin has weak internal pull-down that is always enabled

21 Clocking

This figure shows the internal distribution of clocks within the device.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4, 5 and 6. Value is decided by RCWLR[SPMF].

Figure 53. MPC8308 Clock Subsystem

The following external clock sources are utilized on the MPC8308:

- System clock (SYS_CLK_IN)
- Ethernet Clock (TSEC1_RX_CLK/TSEC1_TX_CLK/TSEC1_GTX_CLK125 for eTSEC)
- SerDes PHY clock
- eSHDC clock (SD_CLK)

  For more information, see the SerDes chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

All clock inputs can be supplied using an external canned oscillator, a clock generation chip, or some other source that provides a standard CMOS square wave input.

21.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 58. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk: csb_clk* Ratio[1]	VCO Divider (VCOD)[2]
0–1	**2–5**	**6**		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	***nnnn***	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8

Note:

1 For any *core_clk:csb_clk* ratios, the *core_clk* must not exceed its maximum operating frequency of 400 MHz.

2 Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

22 Thermal

This section describes the thermal specifications of the device.

23.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8308 system, and the MPC8308 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, NV_{DD}, GV_{DD} and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, and V_{SS} power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, NV_{DD}, GV_{DD}, LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

23.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, LV_{DD} as required. Unused active high inputs should be connected to VSS. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, AV_{DD1}, AV_{DD2}, GV_{DD}, LV_{DD} and V_{SS} pins of the device.

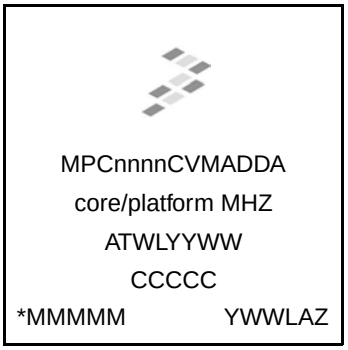
23.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C, MDIO and HRESET)

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS}. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (Figure 55). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

24.2 Part Marking

Parts are marked as in the example shown in this figure.



PBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 56. Freescale Part Marking for PBGA Devices

This table lists the SVR settings.

Table 62. SVR Settings

Device	Package	SVR
MPC8308	MAPBGA	0x8101 _0110

Note: PVR = 8085_0020 for the device.