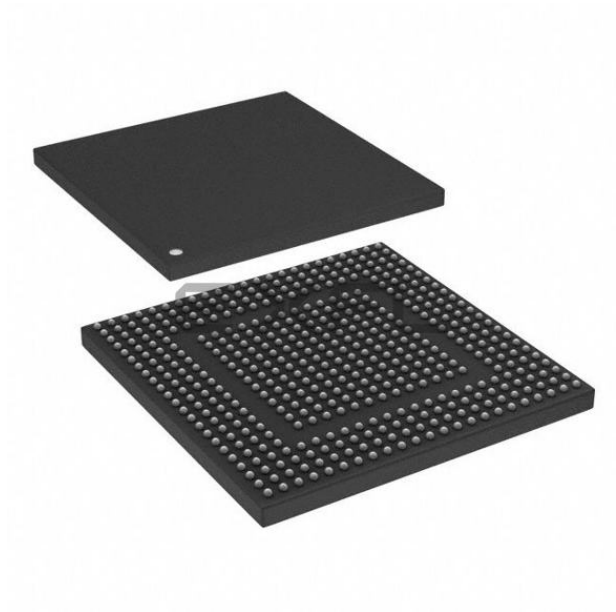

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8308vmadd

2.1.1 Absolute Maximum Ratings

This table lists the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1}, AV_{DD2}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.9	V	—
Local bus, DUART, system control and power management, eSDHC, I^2C, USB, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage		NV_{DD}	–0.3 to 3.6	V	7
SerDes PHY		$XCOREV_{DD}$, $XPADV_{DD}$, $SDAV_{DD}$	–0.3 to 1.26	V	—
eTSEC I/O Voltage		LV_{DD1}, LV_{DD2}	–0.3 to 2.75 or –0.3 to 3.6	V	6, 8
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	eTSEC	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5,8
	Local bus, DUART, system control and power management, eSDHC, I^2C, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage	OV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	3, 5,7
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M, L, O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2
6. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
7. NV_{DD} here refers to NV_{DDA}, NV_{DDB},NV_{DDG}, NV_{DDH}, NV_{DDJ}, NV_{DDP_K} from the ball map.
8. LV_{DD1} here refers to NV_{DDC} and LV_{DD2} refers to NV_{DDF} from the ball map

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ//MDM/MECC output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}		—	ps	5
266 MHz		900			
MDQ//MDM/MECC output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}		—	ps	5
266 MHz		1100			
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

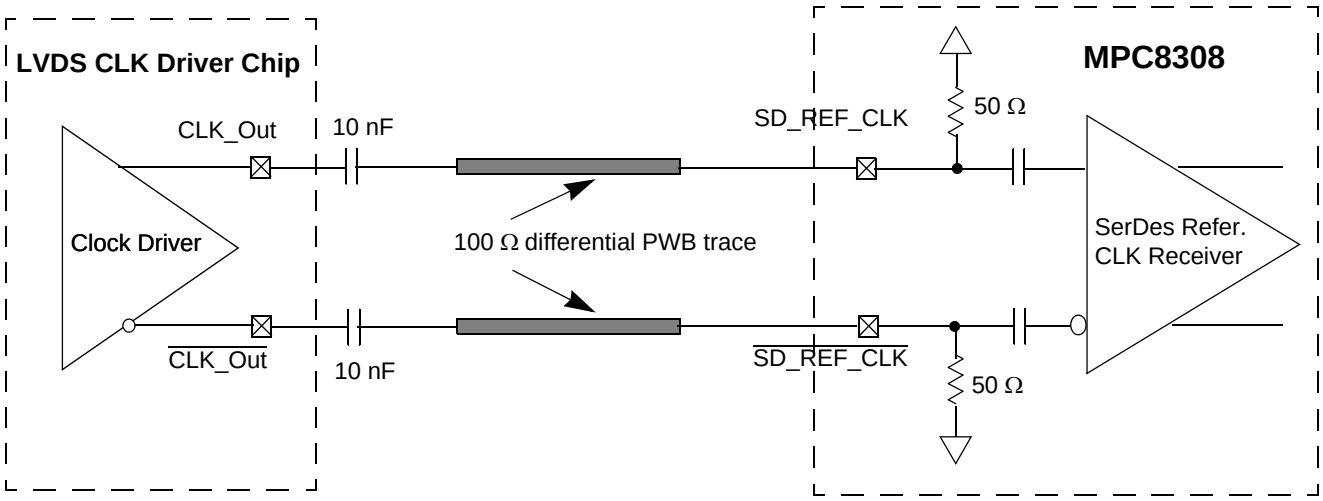


Figure 21. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 22 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8308 SerDes reference clock input's DC requirement, AC-coupling has to be used.

This figure assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8308's SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

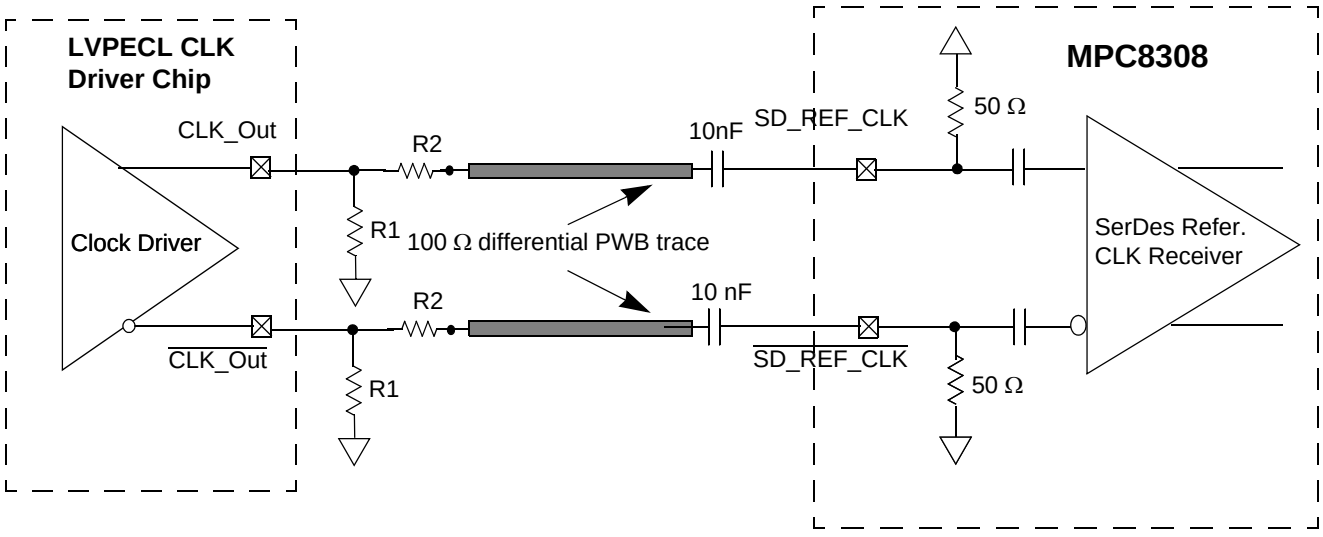


Figure 22. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the device's SerDes reference clock input's DC requirement.

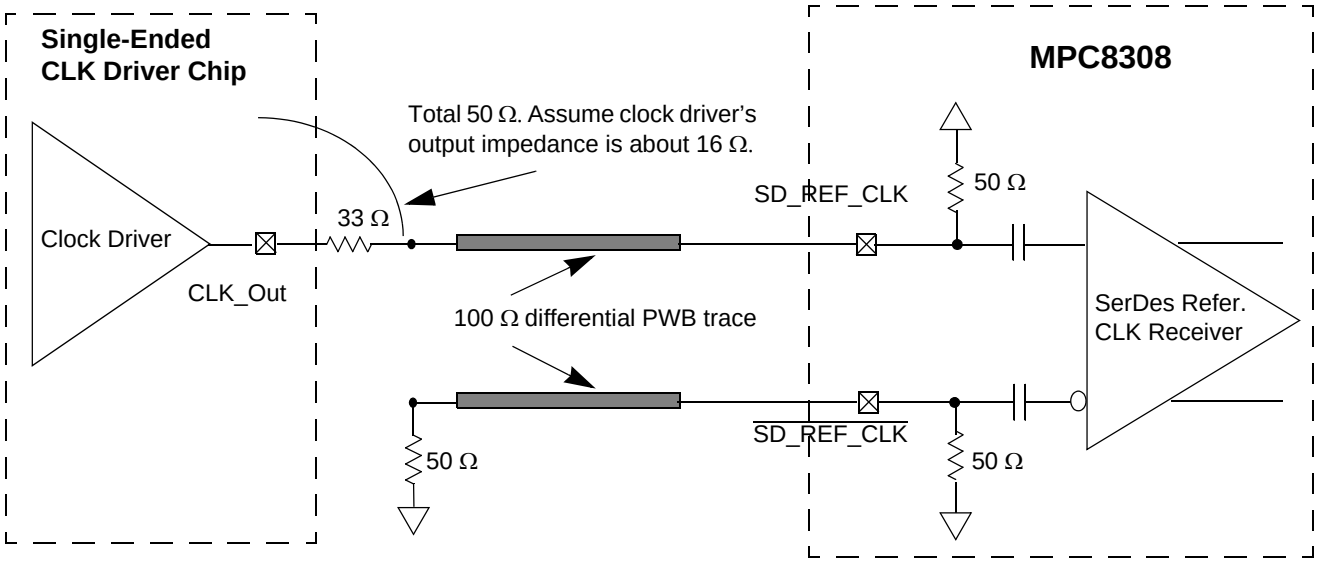


Figure 23. Single-Ended Connection (Reference Only)

10.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for PCI Express protocol.

Table 32. SerDes Reference Clock AC Parameters

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2

Table 32. SerDes Reference Clock AC Parameters (continued)

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
Rising edge rate (SD_REF_CLK) to falling edge rate ($\overline{\text{SD\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing (Figure 24).
4. Matching applies to rising edge rate for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate (See Figure 25).

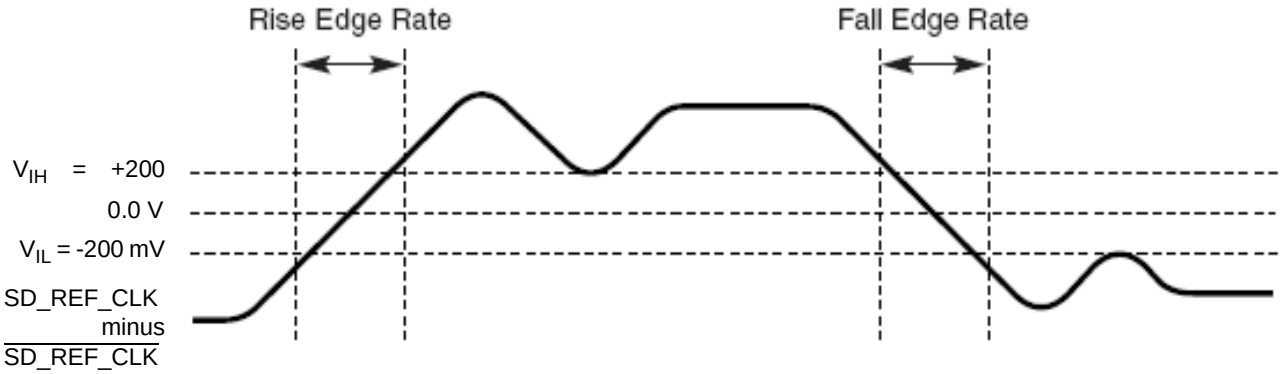


Figure 24. Differential Measurement Points for Rise and Fall Time

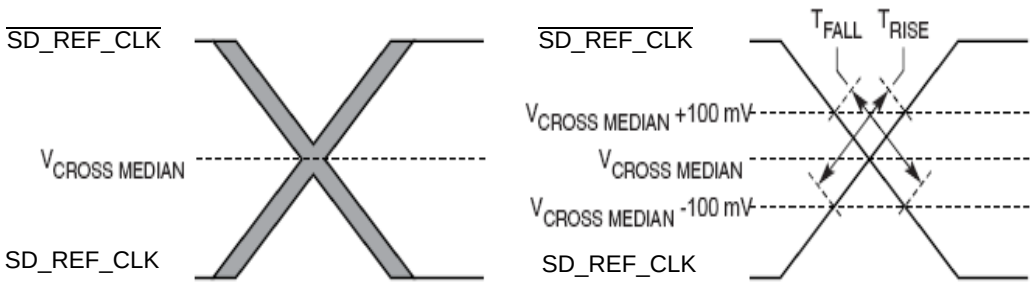


Figure 25. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. For detailed information, see the following sections:

- Section 11.2, “AC Requirements for PCI Express SerDes Clocks”

10.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

10.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

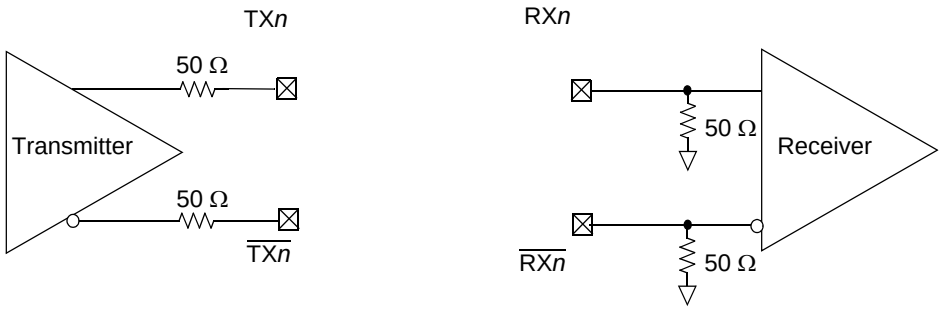


Figure 26. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in Section 11, "PCI Express."

Note that external AC coupling capacitor is required for the PCI Express serial transmission protocol with the capacitor value defined in specification of PCI Express protocol section.

11 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

11.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 10.2, "SerDes Reference Clocks."

11.2 AC Requirements for PCI Express SerDes Clocks

This table lists the PCI Express SerDes clock AC requirements.

Table 33. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Units	Notes
t_{REF}	REFCLK cycle time (for 125 MHz and 100 MHz)	8	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

11.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

11.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer please use the *PCI Express Base Specification*, Rev. 1.0a.

11.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 34. Differential Transmitter (TX) Output Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Unit interval	UI	Each U_{PETX} is 400 ps ± 300 ppm. U_{PETX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	$V_{PEDPPTX} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.8	—	1.2	V	2
De-Emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	Ratio of the $V_{PEDPPTX}$ of the second and following bits after a transition divided by the $V_{PEDPPTX}$ of the first bit after a transition.	–3.0	–3.5	–4.0	dB	2
Minimum TX eye width	T_{TX-EYE}	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - U_{PEEWTX} = 0.3$ UI.	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPTX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.15	UI	2, 3
D+/D- TX output rise/fall time	$T_{TX-RISE}$, $T_{TX-FALL}$	—	0.125	—	—	UI	2, 5
RMS AC peak common mode output voltage	$V_{TX-CM-ACp}$	$V_{PEACPCMTX} = RMS(\|V_{TXD+} + V_{TXD-}\|/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$	—	—	20	mV	2

Table 35. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
AC peak common mode input voltage	$V_{RX-CM-ACp}$	$V_{PEACPCMRX} = \lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$	—	—	150	mV	2
Differential return loss	$RL_{RX-DIFF}$	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively.	15	—	—	dB	4
Common mode return loss	RL_{RX-CM}	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V.	6	—	—	dB	4
DC differential input impedance	$Z_{RX-DIFF-DC}$	RX DC differential mode impedance.	80	100	120	Ω	5
DC Input Impedance	Z_{RX-DC}	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance).	40	50	60	Ω	2, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	$V_{PEEIDT} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

13.3.1 High Speed Output Path (Write)

This figure provides the data and command output timing diagram.

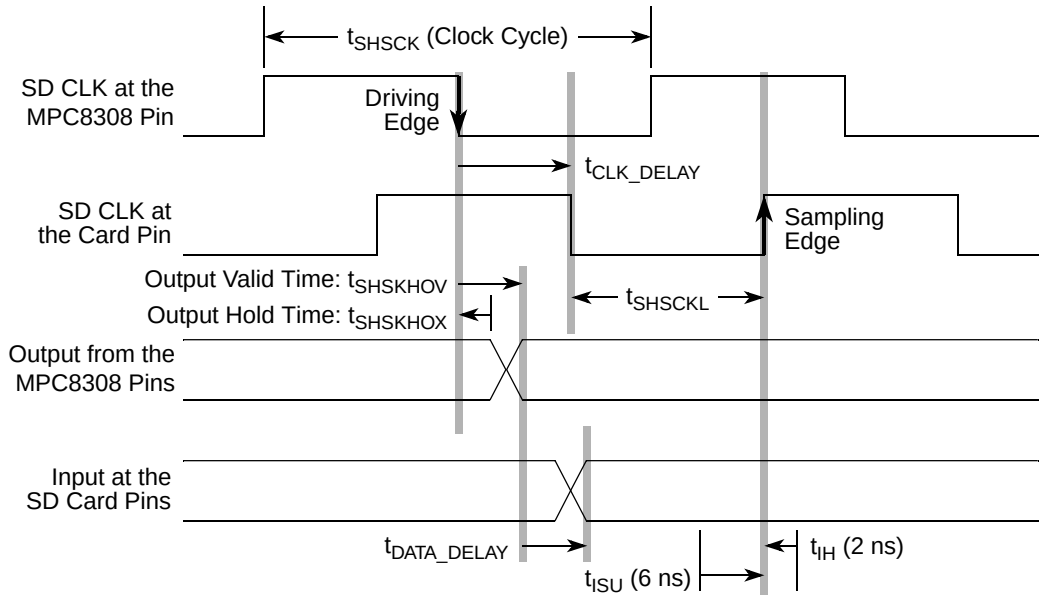


Figure 38. High Speed Output Path

13.3.2 High Speed Input Path (Read)

This figure provides the data and command input timing diagram.

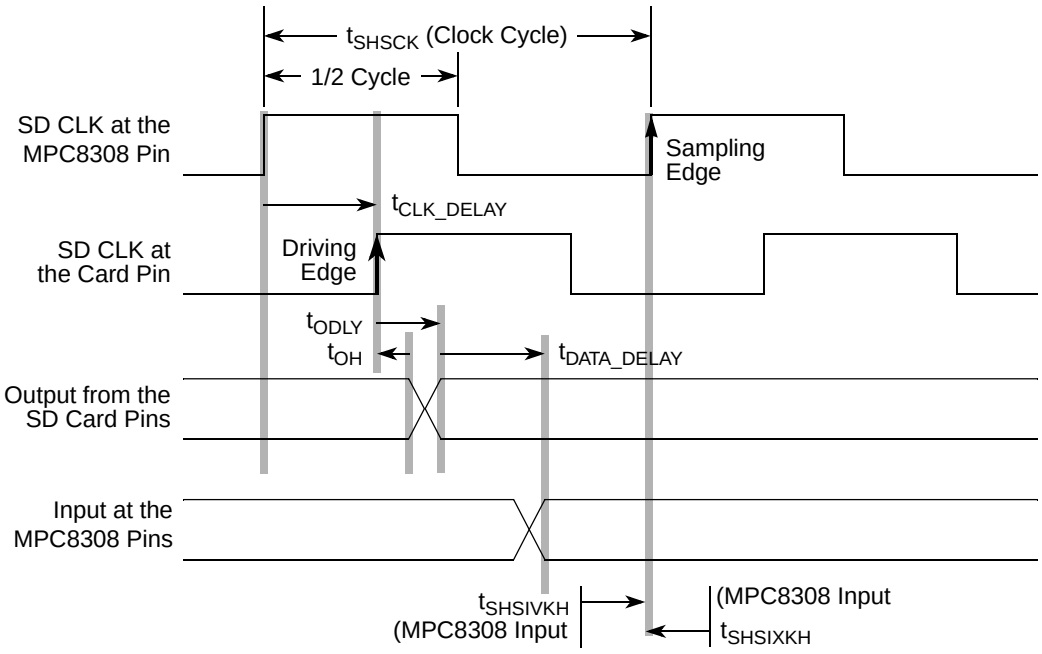


Figure 39. High Speed Input Path

Table 44. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The device does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

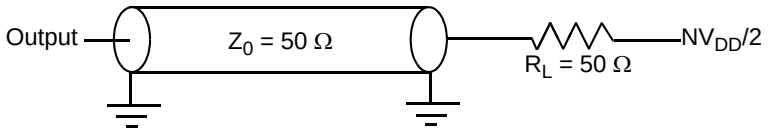


Figure 45. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

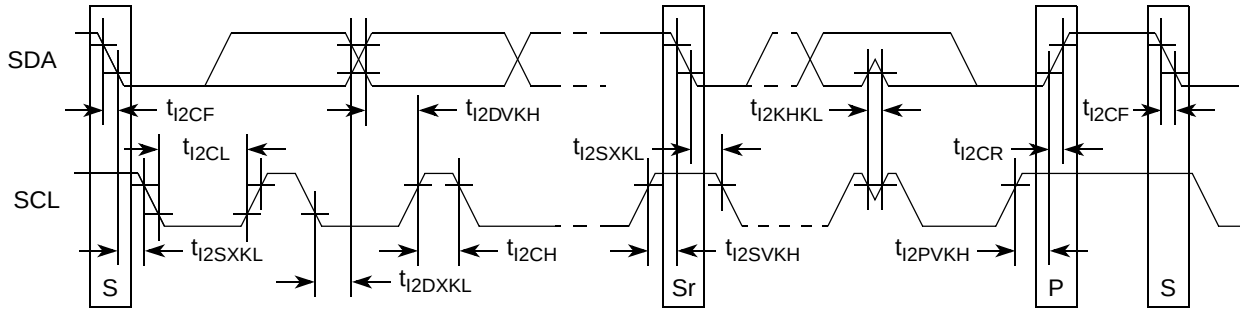
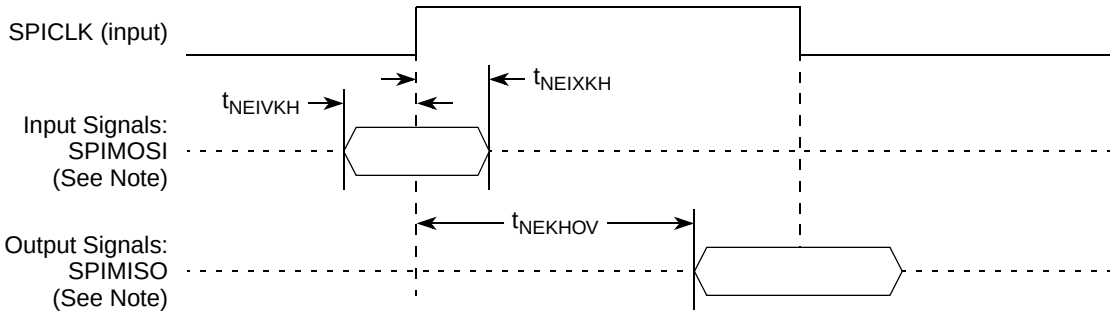


Figure 46. I²C Bus AC Timing Diagram

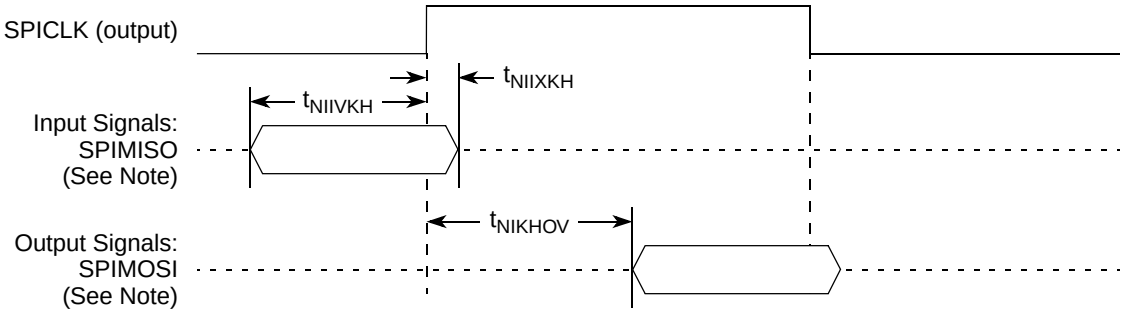
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 51. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8308 is available in a moulded array process ball grid array (MAPBGA). For information on the MAPBGA, see Section 20.1, "Package Parameters for the MPC8308 MAPBGA," and Section 20.2, "Mechanical Dimensions of the MPC8308 MAPBGA."

20.1 Package Parameters for the MPC8308 MAPBGA

The package parameters are as provided in the following list. The package type is 19 mm × 19 mm, 473 MAPBGA.

Package outline	19 mm × 19 mm
Interconnects	473
Pitch	0.80 mm
Module height (typical)	1.39 mm
Solder Balls	96.5 Sn/ 3.5Ag
Ball diameter (typical)	0.40 mm

2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

20.3 Pinout Listings

This table provides the pin-out listing for the MPC8308, MAPBGA package.

Table 53. MPC8308 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	V6	I/O	GV_{DDA}	—
MEMC_MDQ[1]	Y4	I/O	GV_{DDA}	—
MEMC_MDQ[2]	AB3	I/O	GV_{DDA}	—
MEMC_MDQ[3]	AA3	I/O	GV_{DDA}	—
MEMC_MDQ[4]	AA2	I/O	GV_{DDA}	—
MEMC_MDQ[5]	AA1	I/O	GV_{DDA}	—
MEMC_MDQ[6]	W4	I/O	GV_{DDA}	—
MEMC_MDQ[7]	Y2	I/O	GV_{DDA}	—
MEMC_MDQ[8]	W3	I/O	GV_{DDA}	—
MEMC_MDQ[9]	W1	I/O	GV_{DDA}	—
MEMC_MDQ[10]	Y1	I/O	GV_{DDA}	—
MEMC_MDQ[11]	W2	I/O	GV_{DDA}	—
MEMC_MDQ[12]	U4	I/O	GV_{DDA}	—
MEMC_MDQ[13]	U3	I/O	GV_{DDA}	—
MEMC_MDQ[14]	V4	I/O	GV_{DDA}	—
MEMC_MDQ[15]	U6	I/O	GV_{DDA}	—
MEMC_MDQ[16]	T3	I/O	GV_{DDB}	—
MEMC_MDQ[17]	T2	I/O	GV_{DDB}	—
MEMC_MDQ[18]	R4	I/O	GV_{DDB}	—
MEMC_MDQ[19]	R3	I/O	GV_{DDB}	—
MEMC_MDQ[20]	P4	I/O	GV_{DDB}	—
MEMC_MDQ[21]	N6	I/O	GV_{DDB}	—
MEMC_MDQ[22]	P2	I/O	GV_{DDB}	—
MEMC_MDQ[23]	P1	I/O	GV_{DDB}	—
MEMC_MDQ[24]	N4	I/O	GV_{DDB}	—
MEMC_MDQ[25]	N3	I/O	GV_{DDB}	—
MEMC_MDQ[26]	N2	I/O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDQ[27]	M6	I/O	GV_{DDB}	—
MEMC_MDQ[28]	M2	I/O	GV_{DDB}	—
MEMC_MDQ[29]	M3	I/O	GV_{DDB}	—
MEMC_MDQ[30]	L2	I/O	GV_{DDB}	—
MEMC_MDQ[31]	L3	I/O	GV_{DDB}	—
MEMC_MDM[0]	AB2	O	GV_{DDA}	—
MEMC_MDM[1]	V3	O	GV_{DDA}	—
MEMC_MDM[2]	P3	O	GV_{DDB}	—
MEMC_MDM[3]	M7	O	GV_{DDB}	—
MEMC_MDM[8]	K2	O	GV_{DDB}	—
MEMC_MDQS[0]	AC3	I/O	GV_{DDA}	—
MEMC_MDQS[1]	V1	I/O	GV_{DDA}	—
MEMC_MDQS[2]	R1	I/O	GV_{DDB}	—
MEMC_MDQS[3]	M1	I/O	GV_{DDB}	—
MEMC_MDQS[8]	K1	I/O	GV_{DDB}	—
MEMC_MBA[0]	C3	O	GV_{DDB}	—
MEMC_MBA[1]	B2	O	GV_{DDB}	—
MEMC_MBA[2]	H4	O	GV_{DDB}	—
MEMC_MA0	C2	O	GV_{DDB}	—
MEMC_MA1	D2	O	GV_{DDB}	—
MEMC_MA2	D3	O	GV_{DDB}	—
MEMC_MA3	D4	O	GV_{DDB}	—
MEMC_MA4	E4	O	GV_{DDB}	—
MEMC_MA5	F4	O	GV_{DDB}	—
MEMC_MA6	E2	O	GV_{DDB}	—
MEMC_MA7	E1	O	GV_{DDB}	—
MEMC_MA8	F2	O	GV_{DDB}	—
MEMC_MA9	F3	O	GV_{DDB}	—
MEMC_MA10	C1	O	GV_{DDB}	—
MEMC_MA11	F7	O	GV_{DDB}	—
MEMC_MA12	G2	O	GV_{DDB}	—
MEMC_MA13	G3	O	GV_{DDB}	—
$\overline{\text{MEMC\_MWE}}$	D5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MRAS}}$	B4	O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPICLK	AA5	I/O	NV_{DDP_K}	—
SPISEL	AB4	I	NV_{DDP_K}	—
GPIO/ETSEC2				
GPIO[0]/TSEC2_COL	G21	I/O	NV_{DDF}	—
GPIO[1]/TSEC2_TX_ER	K23	I/O	NV_{DDF}	—
GPIO[2]/TSEC2_GTX_CLK	H18	I/O	NV_{DDF}	—
GPIO[3]/TSEC2_RX_CLK	G23	I/O	NV_{DDF}	—
GPIO[4]/TSEC2_RX_DV	J18	I/O	NV_{DDF}	—
GPIO[5]/TSEC2_RXD3	J20	I/O	NV_{DDF}	—
GPIO[6]/TSEC2_RXD2	H22	I/O	NV_{DDF}	—
GPIO[7]/TSEC2_RXD1	H21	I/O	NV_{DDF}	—
GPIO[8]/TSEC2_RXD0	H20	I/O	NV_{DDF}	—
GPIO[9]/TSEC2_RX_ER	J21	I/O	NV_{DDF}	—
GPIO[10]/TSEC2_TX_CLK/ TSEC2_GTX_CLK125	J23	I/O	NV_{DDF}	—
GPIO[11]/TSEC2_TXD3	K22	I/O	NV_{DDF}	—
GPIO[12]/TSEC2_TXD2	K20	I/O	NV_{DDF}	—
GPIO[13]/TSEC2_TXD1	K18	I/O	NV_{DDF}	—
GPIO[14]/TSEC2_TXD0	J17	I/O	NV_{DDF}	—
GPIO[15]/TSEC2_TX_EN	K21	I/O	NV_{DDF}	—
USB/IEEE1588/GTM				
USBDR_PWR_FAULT	P20	I	NV_{DDH}	—
USBDR_CLK	R23	I	NV_{DDH}	—
USBDR_DIR	R21	I	NV_{DDH}	—
USBDR_NXT	P18	I	NV_{DDH}	—
USBDR_TXDRXD0	T22	I/O	NV_{DDH}	—
USBDR_TXDRXD1	T21	I/O	NV_{DDH}	—
USBDR_TXDRXD2	U23	I/O	NV_{DDH}	—
USBDR_TXDRXD3	U22	I/O	NV_{DDH}	—
USBDR_TXDRXD4	T20	I/O	NV_{DDH}	—
USBDR_TXDRXD5	R18	I/O	NV_{DDH}	—
USBDR_TXDRXD6	V23	I/O	NV_{DDH}	—
USBDR_TXDRXD7	V22	I/O	NV_{DDH}	—
USBDR_PCTL0	R17	O	NV_{DDH}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	Y23, H8, H9, H10, H14, H15, H16, J8, J16, K8, K16, L8, L16, M8, M16, N8, N16, P8, P16, R8, R16, T8, T9, T10, T11, T12, T13, T14, T15, T16	I	—	—
VSS	A2, A21, B1, B19, B23, C4, C16, D6, D19, E3, F8, F15, F17, F23, G7, G8, G10, G15, G16, G17, G20, H2, H6, H7, H17, H23, J7, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, K15, L1, L7, L9, L10, L11, L12, L13, L14, L15, L20, M4, M9, M10, M11, M12, M13, M14, M15, N9, N10, N11, N12, N13, N14, N15, P6, P7, P9, P10, P11, P12, P13, P14, P15, R2, R7, R9, R10, R11, R12, R13, R14, R15, R22, T6, T7, U8, U17, U21, V2, V7, V9, V11, W20, Y8, Y15, AA4, AB1, AB6, AB12, AB19, AC2, AC9, AC23	I	—	—
NV_{DDA}	B7, B10, C7, D9, F9	I	—	—
NV_{DDB}	A16, A19, C18	I	—	—
NV_{DDC}	A23, B22, D23, E20, G18	I	—	—
NV_{DDF}	G22, J22, K17	I	—	—
NV_{DDG}	M17, N22	I	—	—
NV_{DDH}	P17, R20, T17, T23, W22, Y22	I	—	—
NV_{DDJ}	AB23, AA22	I	—	—
NV_{DDP_K}	U10, U14, Y5, Y18, AA11, AB8, AB16, AB22, AC4, AC13	I	—	—
GV_{DD}	A1, A6, B3, D1, F1, F6, G4, J1, J4, K7, N1, N7, T1, T4, U7, Y3, AC1	I	—	—
XPADVDD	D15, F10, F14	I	—	—
XPADVSS	A10, B15, D14, G13, G14, H12	I	—	—
XCOREVDD	A14, B12, C13	I	—	—
XCOREVSS	A12, B14, C11, D11, D13, G11, H11, H13	I	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. This pin has weak internal pull-up that is always enabled. 5. This pin must always be tied to VSS.
6. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
7. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a buffer released to high impedance is needed.
8. This pin has weak internal pull-down that is always enabled

22.1 Thermal Characteristics

This table provides the package thermal characteristics for the 473, 19 × 19 mm MAPBGA.

Table 59. Package Thermal Characteristics for MAPBGA

Characteristic	Board Type	Symbol	Value	Unit	Note
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	42	°C/W	1, 2
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	27	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	35	°C/W	1, 3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W	1, 3
Junction to Board	—	$R_{\theta JB}$	17	°C/W	4
Junction to Case	—	$R_{\theta JC}$	9	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

22.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

22.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-t-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is

appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)
T_B = board temperature at the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)
T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8308 system, and the MPC8308 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, NV_{DD}, GV_{DD} and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, and V_{SS} power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, NV_{DD}, GV_{DD}, LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

23.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, LV_{DD} as required. Unused active high inputs should be connected to VSS. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, AV_{DD1}, AV_{DD2}, GV_{DD}, LV_{DD} and V_{SS} pins of the device.

23.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C, MDIO and HRESET)

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS}. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (Figure 55). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

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