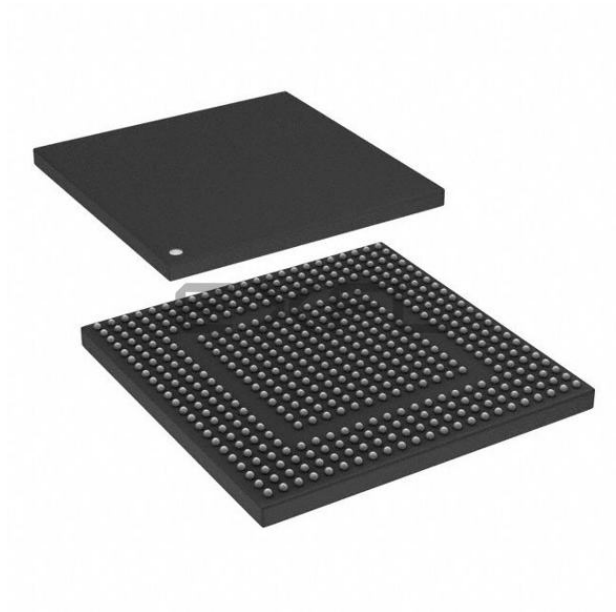

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Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8308vmadda

2.1.1 Absolute Maximum Ratings

This table lists the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1}, AV_{DD2}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.9	V	—
Local bus, DUART, system control and power management, eSDHC, I^2C, USB, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage		NV_{DD}	–0.3 to 3.6	V	7
SerDes PHY		$XCOREV_{DD}$, $XPADV_{DD}$, $SDAV_{DD}$	–0.3 to 1.26	V	—
eTSEC I/O Voltage		LV_{DD1}, LV_{DD2}	–0.3 to 2.75 or –0.3 to 3.6	V	6, 8
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	eTSEC	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5,8
	Local bus, DUART, system control and power management, eSDHC, I^2C, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage	OV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	3, 5,7
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M, L, O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2
6. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
7. NV_{DD} here refers to NV_{DDA}, NV_{DDB},NV_{DDG}, NV_{DDH}, NV_{DDJ}, NV_{DDP_K} from the ball map.
8. LV_{DD1} here refers to NV_{DDC} and LV_{DD2} refers to NV_{DDF} from the ball map

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8308 Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	NV_{DD} (3.3 V)	LV_{DD}/ (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR2 R_S = 22 Ω R_t = 75 Ω	250 MHz 32 bits+ECC 266 MHz 32 bits+ECC	0.302 0.309	—	—	—	W	—
Local bus I/O load = 20 pF	62.5 MHz 66 MHZ	—	0.038 0.040	—	—	W	—
TSEC I/O load = 20 pF	MII, 25 MHz	—	—	0.008	—	W	2 controllers
	RGMII, 125 MHz	—	—	0.078	0.044	W	
eSDHC IO Load = 40 pF	50 MHz	—	—	0.008	—	W	—
USB IO Load = 20 pF	60 MHz	—	—	0.012		W	—
Other I/O	—	—	0.017	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN) DC electrical specifications for the device.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V $\le V_{IN} \le NV_{DD}$	I_{IN}	—	±10	μA

This table provides the RTC clock input (RTC_PIT_CLOCK) DC electrical specifications for the device.

Table 7. RTC_PIT_CLOCK DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	3.3 V – 400 mV		V
Input low voltage	—	V_{IL}	0	0.4	V

4.2 AC Electrical Characteristics

The primary clock source for the device is SYS_CLK_IN. This table provides the system clock input (SYS_CLK_IN) AC timing specifications for the device.

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ//MDM/MECC output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}		—	ps	5
266 MHz		900			
MDQ//MDM/MECC output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}		—	ps	5
266 MHz		1100			
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure shows the MII transmit AC timing diagram.

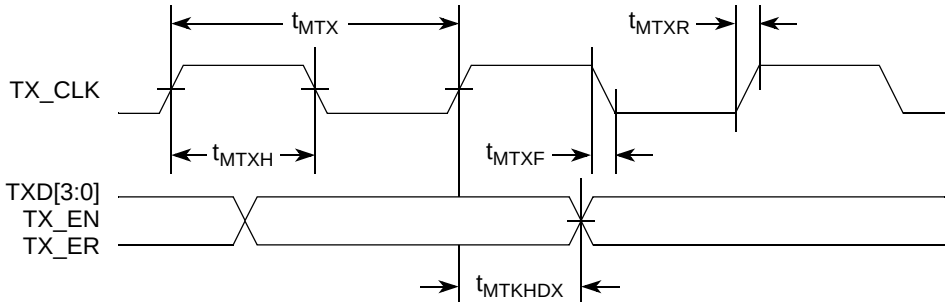


Figure 8. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 28. GPIO DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NVDD$	—	± 5	μA

8.4.2 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

Table 29. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	—
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Note:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9 USB

9.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

9.1.1 USB DC Electrical Characteristics

This table lists the DC electrical characteristics for the USB interface.

Table 30. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LVDD + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	LVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

- **Common Mode Voltage, V_{cm}**

  The common mode voltage is equal to one-half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{TXn} + V_{\overline{TXn}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

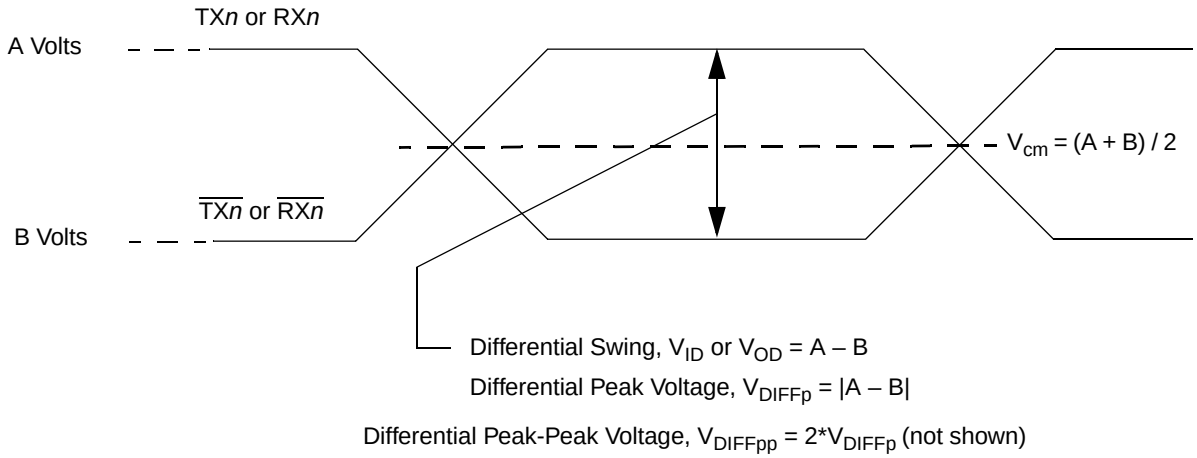


Figure 15. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

10.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for PCI Express.

The following sections describe the SerDes reference clock requirements and some application information.

10.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8308 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 10.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 17 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 18 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 19 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

Table 34. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Absolute delta of DC common mode voltage during L0 and electrical idle	$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	$\lvert V_{TX\text{-}CM\text{-}DC\ (during\ L0)} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ (During\ Electrical\ Idle)}\rvert <= 100$ mV $V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [L0] $V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [Electrical Idle]	0	—	100	mV	2
Absolute delta of DC common mode between D+ and D–	$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	$\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-}\rvert <= 25$ mV $V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+}\rvert$ $V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D-}\rvert$	0	—	25	mV	2
Electrical idle differential peak output voltage	$V_{TX\text{-}IDLE\text{-}DIFFp}$	$V_{PEEIDPTX} = \lvert V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-}\rvert <= 20$ mV	0	—	20	mV	2
Amount of voltage change allowed during receiver detection	$V_{TX\text{-}RCV\text{-}DETECT}$	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present.	—	600	—	mV	6
TX DC common mode voltage	$V_{TX\text{-}DC\text{-}CM}$	The allowed DC Common Mode voltage under any conditions.	—	3.6	—	V	6
TX short circuit current limit	$I_{TX\text{-}SHORT}$	The total current the Transmitter can provide when shorted to its ground	—	—	90	mA	—
Minimum time spent in electrical idle	$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set	50	—	—	UI	—
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.	—	—	20	UI	—
Maximum time to transition to valid TX specifications after leaving an electrical idle condition	$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle	—	—	20	UI	—
Differential return loss	$RL_{TX\text{-}DIFF}$	Measured over 50 MHz to 1.25 GHz.	12	—	—	dB	4
Common mode return loss	$RL_{TX\text{-}CM}$	Measured over 50 MHz to 1.25 GHz.	6	—	—	dB	4
DC differential TX impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	TX DC Differential mode Low Impedance	80	100	120	Ω	—
Transmitter DC impedance	$Z_{TX\text{-}DC}$	Required TX D+ as well as D- DC Impedance during all states	40	—	—	Ω	—
Lane-to-Lane output skew	$L_{TX\text{-}SKEW}$	Static skew between any two Transmitter Lanes within a single Link	—	—	500 + 2 UI	ps	—

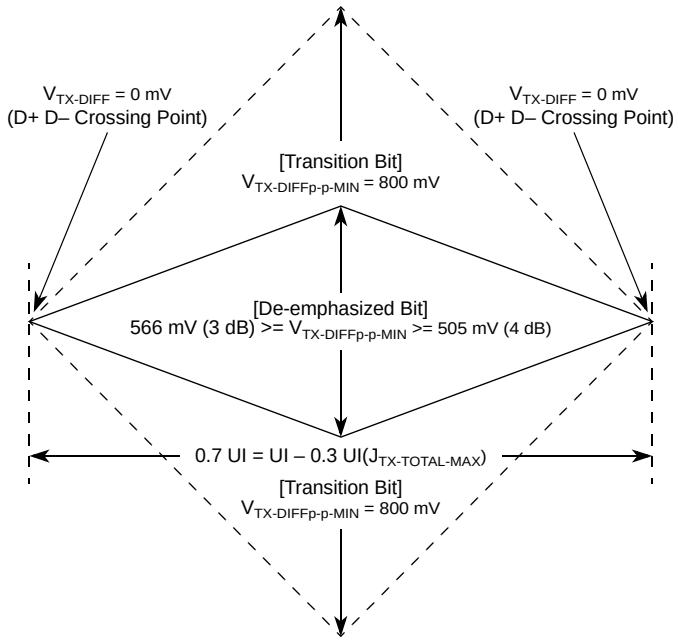


Figure 27. Minimum Transmitter Timing and Voltage Output Compliance Specifications

11.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 35. Differential Receiver (RX) Input Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Unit interval	UI	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{RX-DIFFp-p}$	$V_{PEDPPRX} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	—	1.200	V	2
Minimum receiver eye width	T_{RX-EYE}	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - U_{PEEWRX} = 0.6$ UI.	0.4	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPRX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.3	UI	2, 3, 7

Figure 31 through Figure 33 show the local bus signals. In what follows, T1, T2, T3, and T4 are internal clock reference phase signals corresponding to LCCR[CLKDIV].

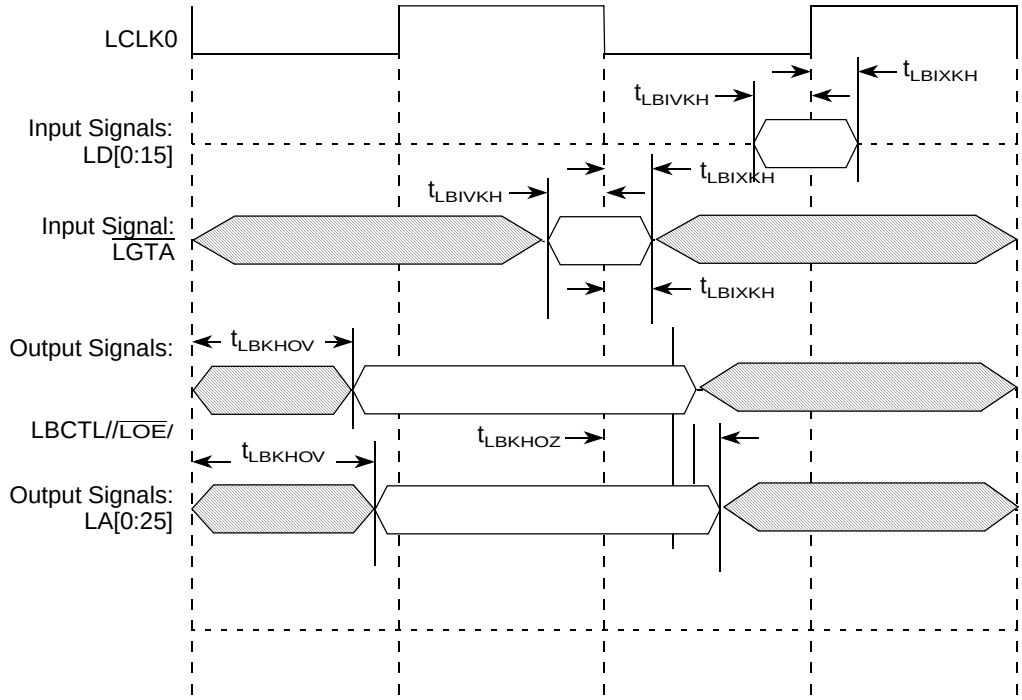


Figure 31. Local Bus Signals, Non-Special Signals Only

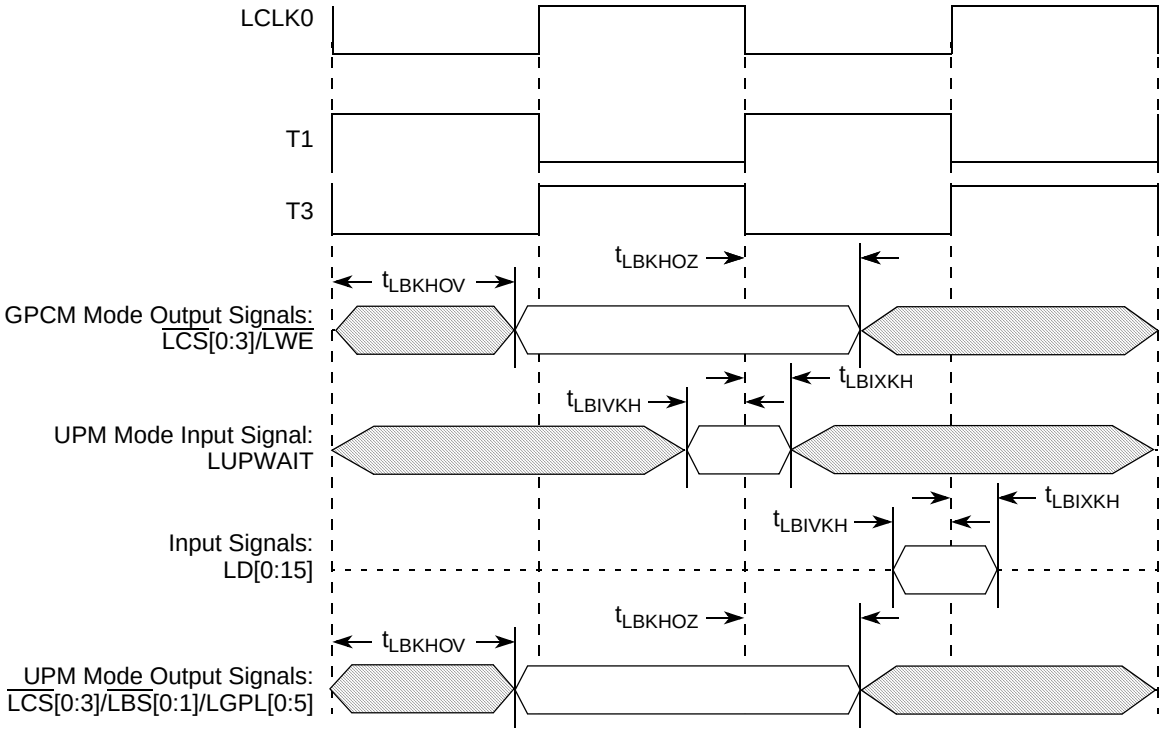


Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2

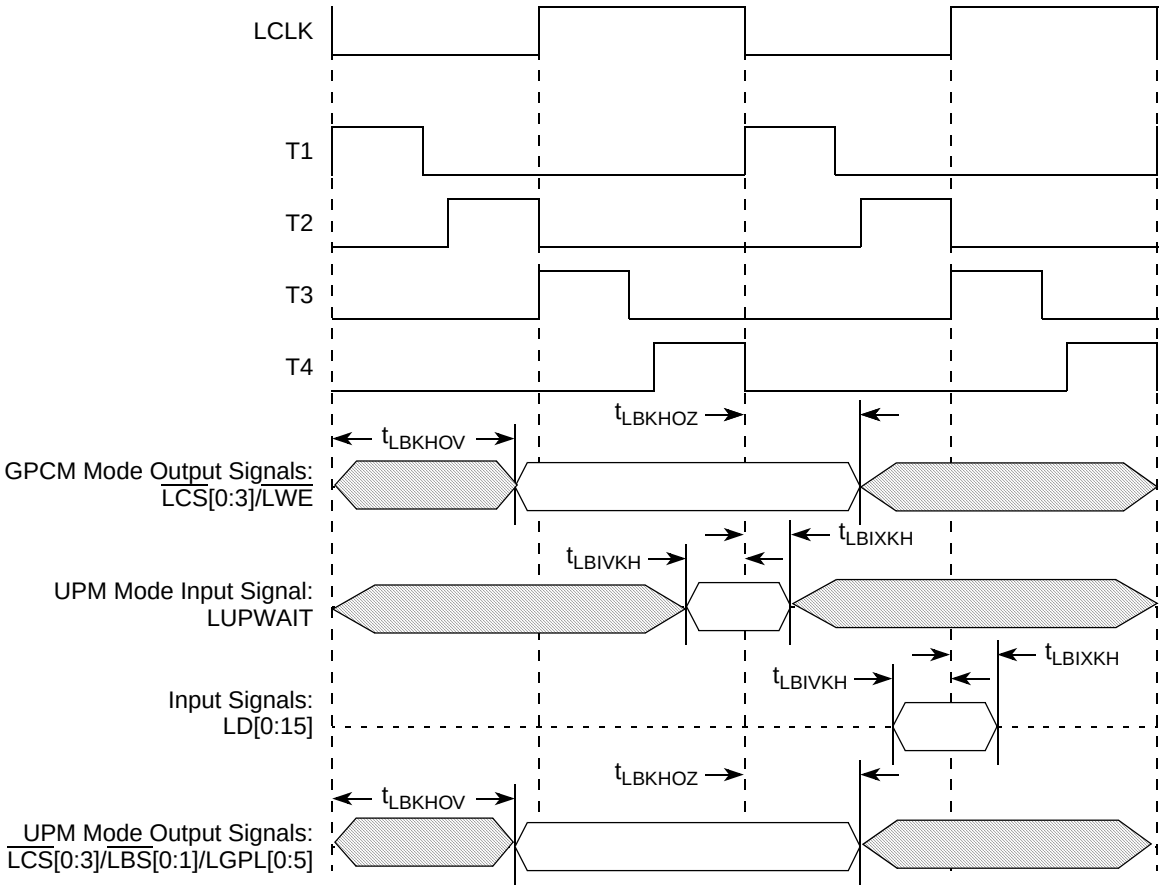


Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4

13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SD/MMC/SDIO) interface of the MPC8308.

The eSDHC controller always uses the falling edge of the SD_CLK in order to drive the SD_DAT[0:3]/CMD as outputs and rising edge to sample the SD_DAT[0:3], CMD, $\overline{\text{CD}}$ and WP as inputs. This behavior is true for both full and high speed modes.

13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device, compatible with SDHC specifications. The eSDHC NV_{DD} range is between 3.0 V and 3.6 V.

Table 38. eSDHC interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

Table 40. eSDHC AC Timing Specifications for High Speed Mode (continued)

At recommended operating conditions NV_{DD} = 3.3 V ± 300 mV.

Parameter	Symbol [1]	Min	Max	Unit	Notes
SD Card Output Valid	t_{ODLY}	—	14	ns	3
SD Card Output Hold	t_{OH}	2.5	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.

This figure provides the eSDHC clock input timing diagram.

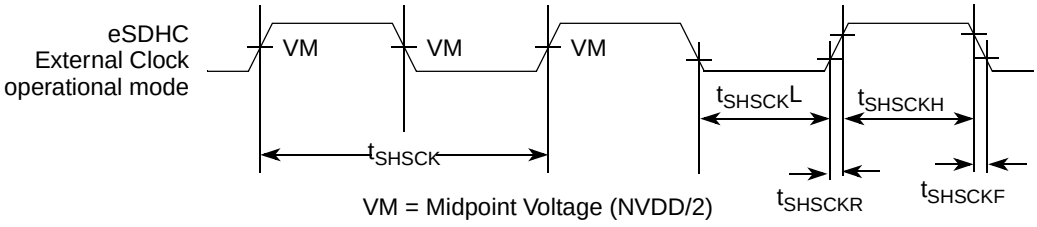


Figure 37. eSDHC Clock Input Timing Diagram

13.3.1 High Speed Output Path (Write)

This figure provides the data and command output timing diagram.

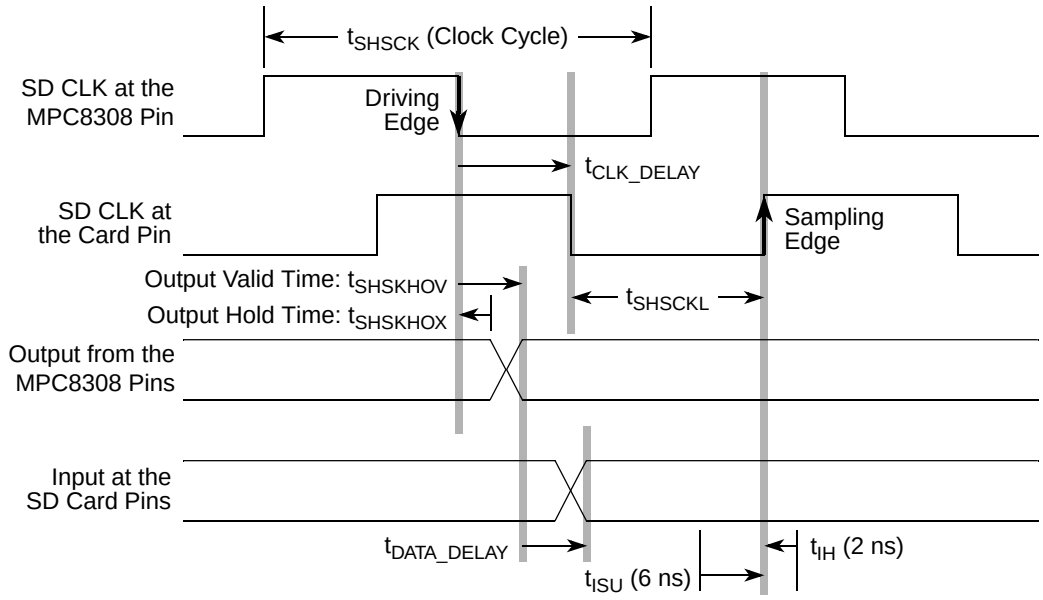


Figure 38. High Speed Output Path

13.3.2 High Speed Input Path (Read)

This figure provides the data and command input timing diagram.

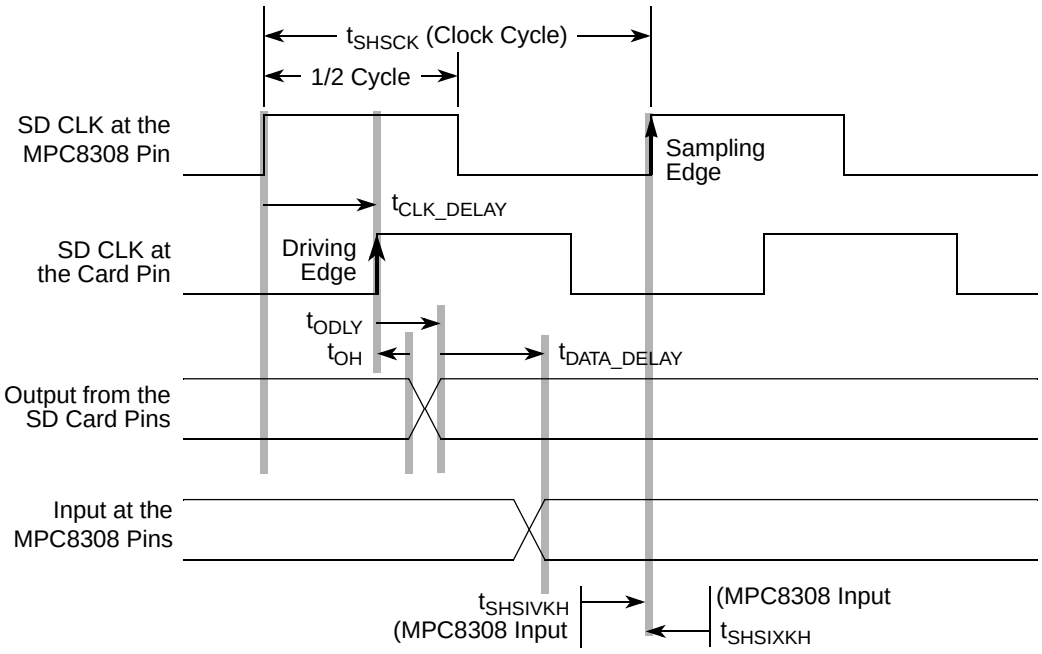


Figure 39. High Speed Input Path

17 GPIO

This section describes the DC and AC electrical specifications for the GPIO of MPC8308

17.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO.

Table 47. GPIO DC Electrical Characteristic

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

17.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 48. GPIO Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

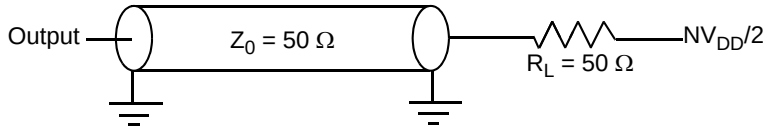


Figure 48. GPIO AC Test Load

Table 51. SPI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

19.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 52. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns
SPI outputs valid—slave mode (external clock) delay	t_{NEKHOV}		8.5	ns
SPI outputs hold—slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

This figure provides the AC test load for the SPI.

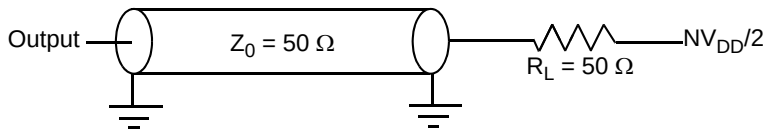


Figure 49. SPI AC Test Load

Figure 50 through Figure 51 represent the AC timing from Table 52. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 53. MPC8308 Pinout Listing (continued)

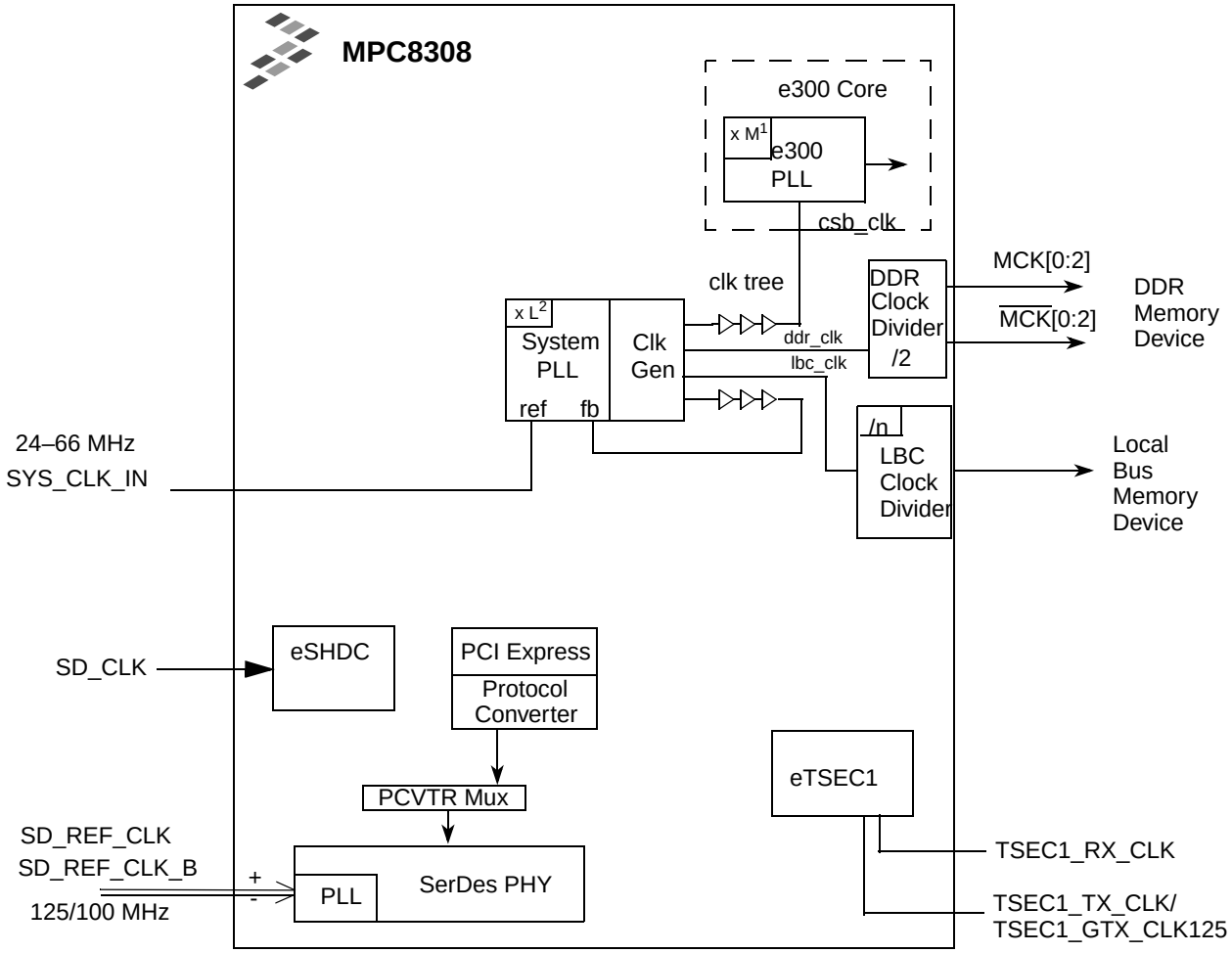
Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDQ[27]	M6	I/O	GV_{DDB}	—
MEMC_MDQ[28]	M2	I/O	GV_{DDB}	—
MEMC_MDQ[29]	M3	I/O	GV_{DDB}	—
MEMC_MDQ[30]	L2	I/O	GV_{DDB}	—
MEMC_MDQ[31]	L3	I/O	GV_{DDB}	—
MEMC_MDM[0]	AB2	O	GV_{DDA}	—
MEMC_MDM[1]	V3	O	GV_{DDA}	—
MEMC_MDM[2]	P3	O	GV_{DDB}	—
MEMC_MDM[3]	M7	O	GV_{DDB}	—
MEMC_MDM[8]	K2	O	GV_{DDB}	—
MEMC_MDQS[0]	AC3	I/O	GV_{DDA}	—
MEMC_MDQS[1]	V1	I/O	GV_{DDA}	—
MEMC_MDQS[2]	R1	I/O	GV_{DDB}	—
MEMC_MDQS[3]	M1	I/O	GV_{DDB}	—
MEMC_MDQS[8]	K1	I/O	GV_{DDB}	—
MEMC_MBA[0]	C3	O	GV_{DDB}	—
MEMC_MBA[1]	B2	O	GV_{DDB}	—
MEMC_MBA[2]	H4	O	GV_{DDB}	—
MEMC_MA0	C2	O	GV_{DDB}	—
MEMC_MA1	D2	O	GV_{DDB}	—
MEMC_MA2	D3	O	GV_{DDB}	—
MEMC_MA3	D4	O	GV_{DDB}	—
MEMC_MA4	E4	O	GV_{DDB}	—
MEMC_MA5	F4	O	GV_{DDB}	—
MEMC_MA6	E2	O	GV_{DDB}	—
MEMC_MA7	E1	O	GV_{DDB}	—
MEMC_MA8	F2	O	GV_{DDB}	—
MEMC_MA9	F3	O	GV_{DDB}	—
MEMC_MA10	C1	O	GV_{DDB}	—
MEMC_MA11	F7	O	GV_{DDB}	—
MEMC_MA12	G2	O	GV_{DDB}	—
MEMC_MA13	G3	O	GV_{DDB}	—
$\overline{\text{MEMC\_MWE}}$	D5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MRAS}}$	B4	O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{LCS}}$[3]	Y11	O	NV_{DDP_K}	4
$\overline{\text{LWE}}$[0] /$\overline{\text{LFWE}}$0/$\overline{\text{LBS}}$0	AB11	O	NV_{DDP_K}	—
$\overline{\text{LWE}}$[1]/$\overline{\text{LBS}}$1	AC11	O	NV_{DDP_K}	—
LBCTL	U11	O	NV_{DDP_K}	—
LGPL0/LFCLE	Y10	O	NV_{DDP_K}	—
LGPL1/LFALE	AA10	O	NV_{DDP_K}	—
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AB10	O	NV_{DDP_K}	4
LGPL3/$\overline{\text{LFWP}}$	AC10	O	NV_{DDP_K}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LFRB	AB9	I/O	NV_{DDP_K}	4
LGPL5	Y9	O	NV_{DDP_K}	—
LCLK0	AC12	O	NV_{DDP_K}	—
DUART				
UART_SOUT1/MSRCID0/ LSRCID0	C17	O	NV_{DDB}	—
UART_SIN1/MSRCID1/ LSRCID1	B18	I/O	NV_{DDB}	—
UART_SOUT2/MSRCID2/ LSRCID2	D17	O	NV_{DDB}	—
UART_SIN2/MSRCID3/ LSRCID3	D18	I/O	NV_{DDB}	—
PEX PHY				
TXA	C14	O	XPADVDD	—
$\overline{\text{TXA}}$	C15	O	XPADVDD	—
RXA	A13	I	XCOREVDD	—
$\overline{\text{RXA}}$	B13	I	XCOREVDD	—
SD_IMP_CAL_RX	A15	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	C12	I	XCOREVDD	—
SD_REF_CLK	D12	I	XCOREVDD	—
SD_PLL_TPD	F13	O	—	—
SD_IMP_CAL_TX	A11	I	XPADVDD	—
SD_PLL_TPA_ANA	F11	O	—	—
SDAVDD_0	G12	I	—	—
SDAVSS_0	F12	I	—	—
I^2C interface				
IIC_SDA1	C9	I/O	NV_{DDA}	2

21 Clocking

This figure shows the internal distribution of clocks within the device.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4, 5 and 6. Value is decided by RCWLR[SPMF].

Figure 53. MPC8308 Clock Subsystem

The following external clock sources are utilized on the MPC8308:

- System clock (SYS_CLK_IN)
- Ethernet Clock (TSEC1_RX_CLK/TSEC1_TX_CLK/TSEC1_GTX_CLK125 for eTSEC)
- SerDes PHY clock
- eSHDC clock (SD_CLK)

  For more information, see the SerDes chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

All clock inputs can be supplied using an external canned oscillator, a clock generation chip, or some other source that provides a standard CMOS square wave input.

21.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 58. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk: csb_clk* Ratio[1]	VCO Divider (VCOD)[2]
0–1	**2–5**	**6**		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	***nnnn***	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8

Note:

1 For any *core_clk:csb_clk* ratios, the *core_clk* must not exceed its maximum operating frequency of 400 MHz.

2 Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

22 Thermal

This section describes the thermal specifications of the device.

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