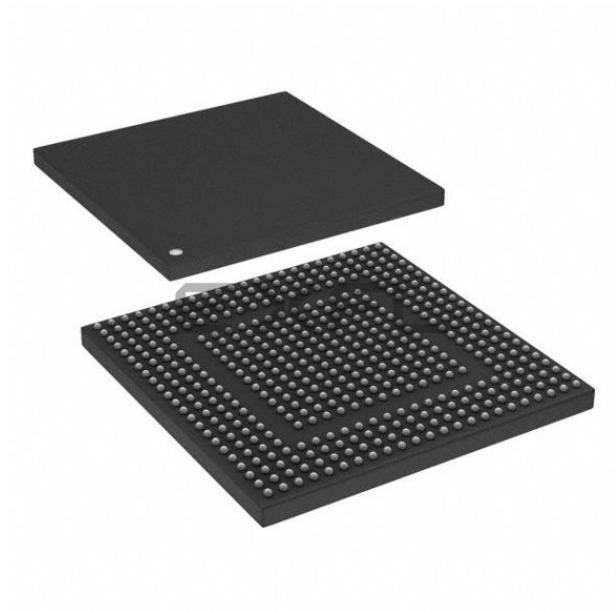

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8308vmaff

The I/O power supply ramp-up slew rate should be slower than 4V/100 μs, this requirement is for ESD circuit. Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD}, LV_{DD}, and NV_{DD}) do not have any ordering requirements with respect to one another.

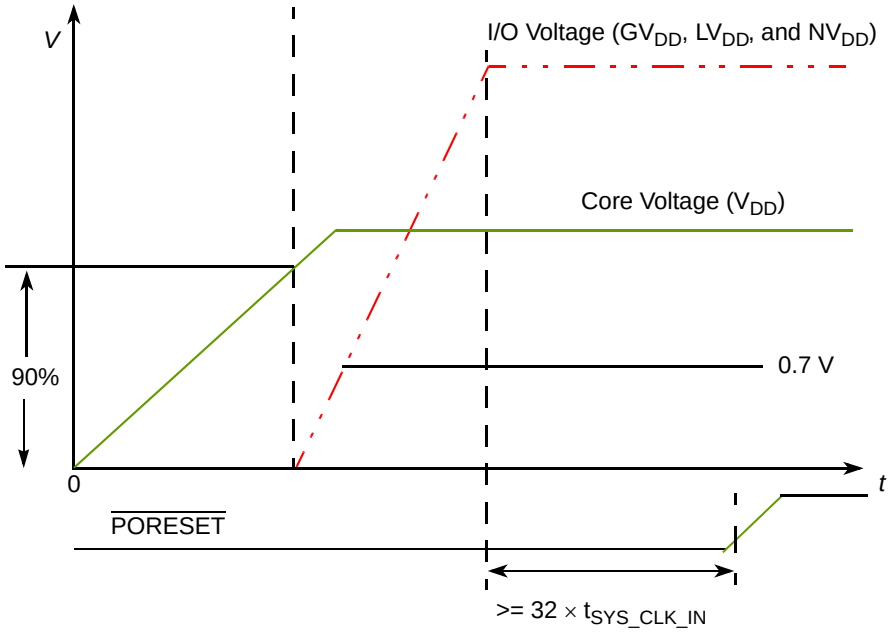


Figure 3. Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power for the device is shown in this table. Table 5 shows the estimated typical I/O power dissipation.

Table 4. MPC8308 Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	Typical[2]	Maximum [3]	Unit
266	133	530	900	mW
333	133	565	950	mW
400	133	600	1000	mW

Note:

1 The values do not include I/O supply power but do include core (V_{DD}) and PLL (AV_{DD1}, AV_{DD2}, $XCOREV_{DD}$, $XPADV_{DD}$, and $SDAV_{DD}$)

2 Typical power is based on best process, a voltage of V_{DD} = 1.0 V and ambient temperature of T_A = 25° C and an artificial smoker test.

3 Maximum power is estimated based on best process, a voltage of V_{DD} = 1.05 V, a junction temperature of T_J = 105° C

Table 25. RGMII AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of t_{RGT} represents the RGMII receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $0.5*LV_{DD}$
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

This figure shows the RGMII AC timing and multiplexing diagrams.

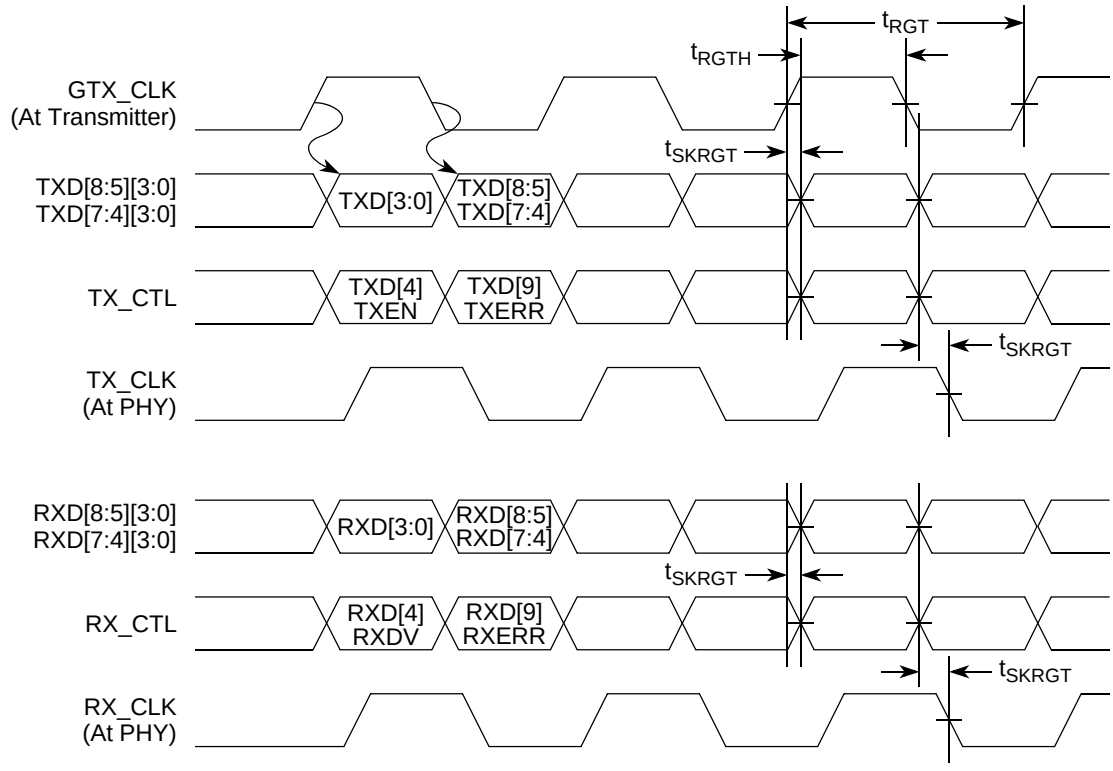


Figure 11. RGMII AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII

10 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

10.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 15 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX*n* and $\overline{\text{TX}n}$) or a receiver input (RX*n* and $\overline{\text{RX}n}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- **Single-Ended Swing**

  The transmitter output signals and the receiver input signals TX*n*, $\overline{\text{TX}n}$, RX*n*, and $\overline{\text{RX}n}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's single-ended swing.
- **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**)

  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.
- **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**)

  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.
- **Differential Peak Voltage, V_{DIFFp}**

  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, V_{DIFFp} = |A – B| Volts.
- **Differential Peak-to-Peak, $V_{DIFFp-p}$**

  Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.
- **Differential Waveform**

  The differential waveform is constructed by subtracting the inverting signal (for example, $\overline{\text{TX}n}$) from the non-inverting signal (for example, TX*n*) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 24 as an example for differential waveform.

10.2.1 SerDes Reference Clock Receiver Characteristics

Figure 16 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XCOREVDD are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 16. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above XCOREVSS. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to XCOREVSS DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

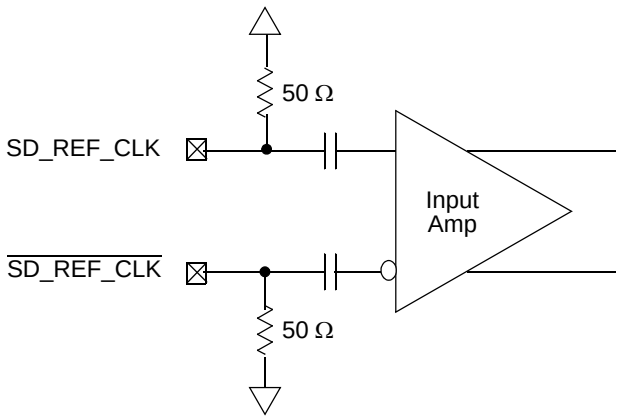


Figure 16. Receiver of SerDes Reference Clocks

10.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8308 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 10.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 17 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 18 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 19 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

12.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 36. Local Bus DC Electrical Characteristics at 3.3 V

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	NV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current, (V_{IN}[1] = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±5	μA
High-level output voltage, (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	NV_{DD} – 0.2	—	V
Low-level output voltage, (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.2	V

Note: The parameters stated in above table are valid for all revisions unless explicitly mentioned.

12.2 Enhanced Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface.

Table 37. Local Bus General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1	—	ns	3, 4
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LD	t_{LBKHOZ}	—	4	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $NV_{DD}/2$ of the rising/falling edge of LCLK0 to 0.4 × NV_{DD} of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

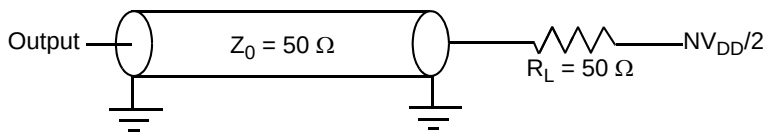


Figure 30. Local Bus AC Test Load

This figure provides the eSDHC clock input timing diagram.

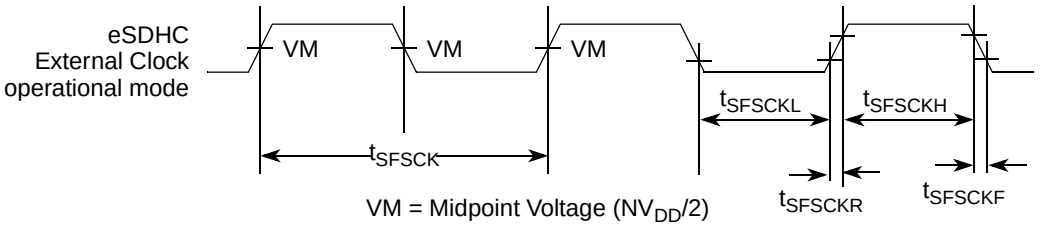


Figure 34. eSDHC Clock Input Timing Diagram

13.2.1 Full Speed Output Path (Write)

This figure provides the data and command output timing diagram.

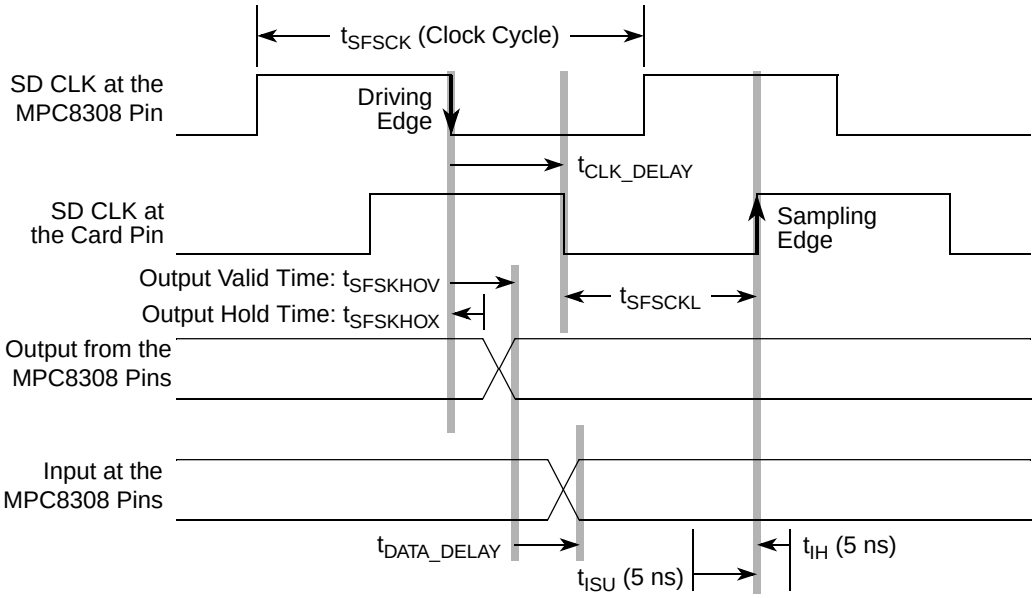


Figure 35. Full Speed Output Path

13.3.1 High Speed Output Path (Write)

This figure provides the data and command output timing diagram.

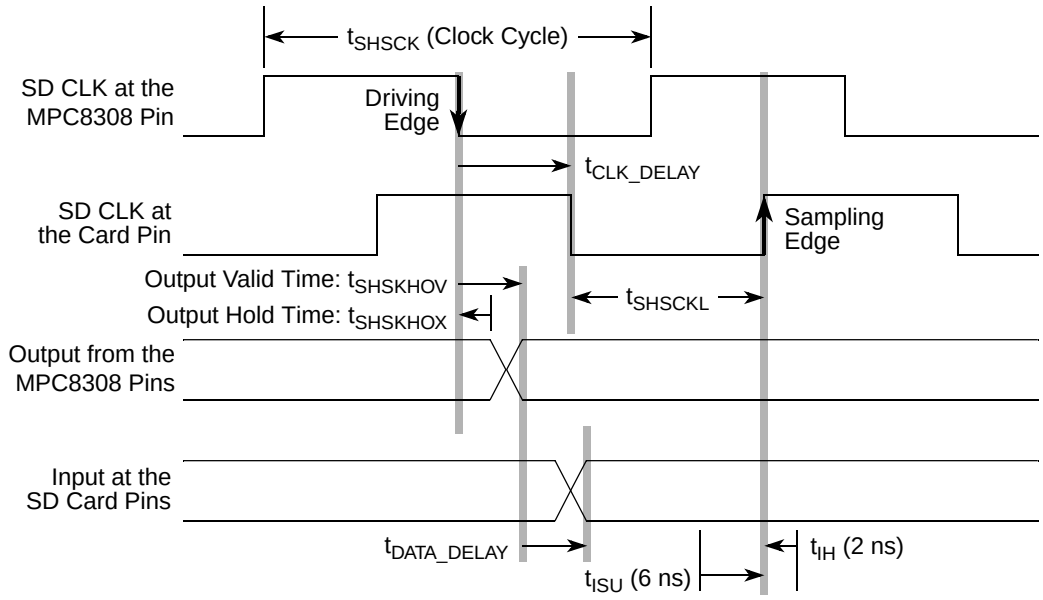


Figure 38. High Speed Output Path

13.3.2 High Speed Input Path (Read)

This figure provides the data and command input timing diagram.

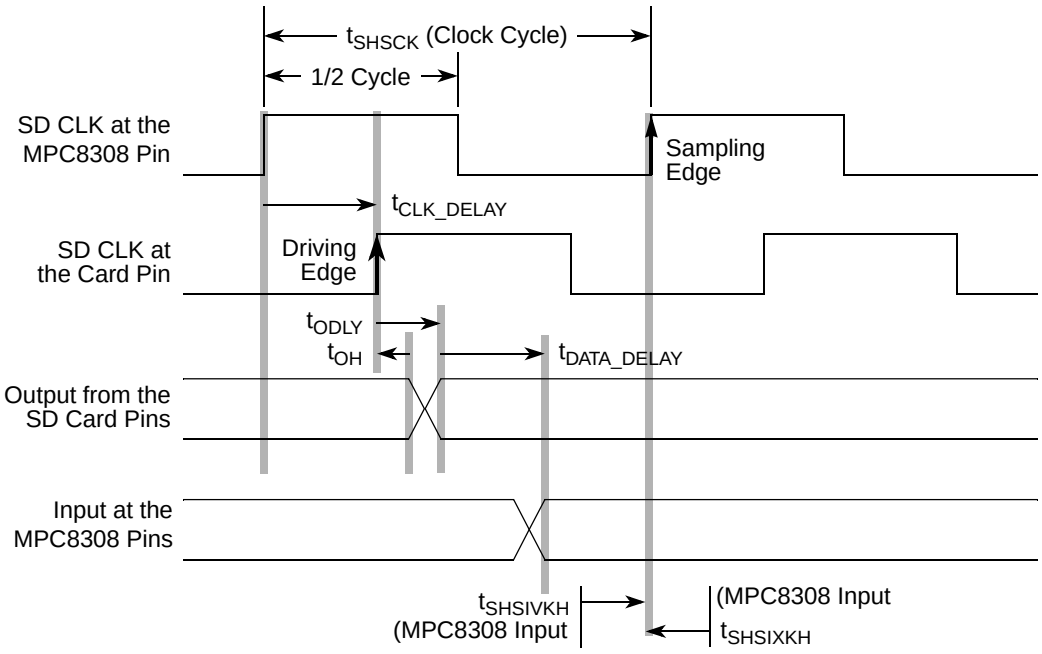


Figure 39. High Speed Input Path

14 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

14.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 41. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—		±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

14.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

This table provides the JTAG AC timing specifications as defined in Figure 41 through Figure 44.

Table 42. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5

Table 51. SPI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

19.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 52. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns
SPI outputs valid—slave mode (external clock) delay	t_{NEKHOV}		8.5	ns
SPI outputs hold—slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

This figure provides the AC test load for the SPI.

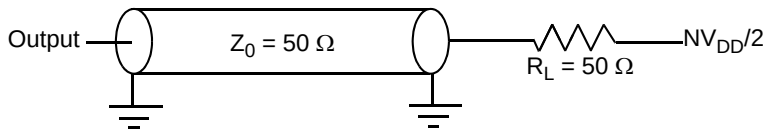
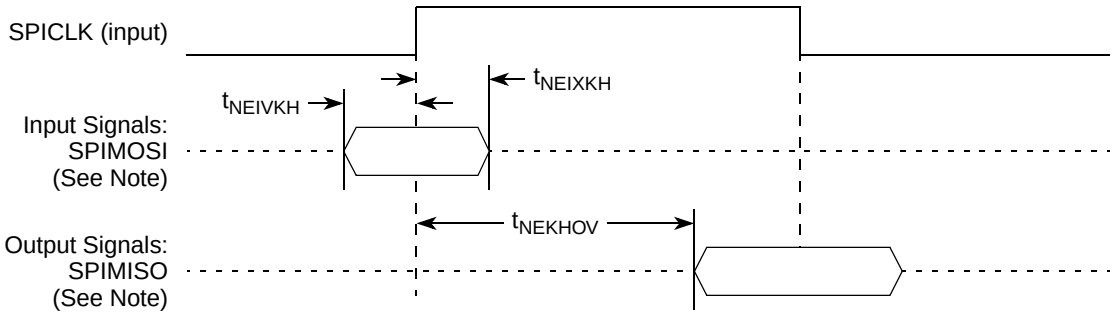


Figure 49. SPI AC Test Load

Figure 50 through Figure 51 represent the AC timing from Table 52. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

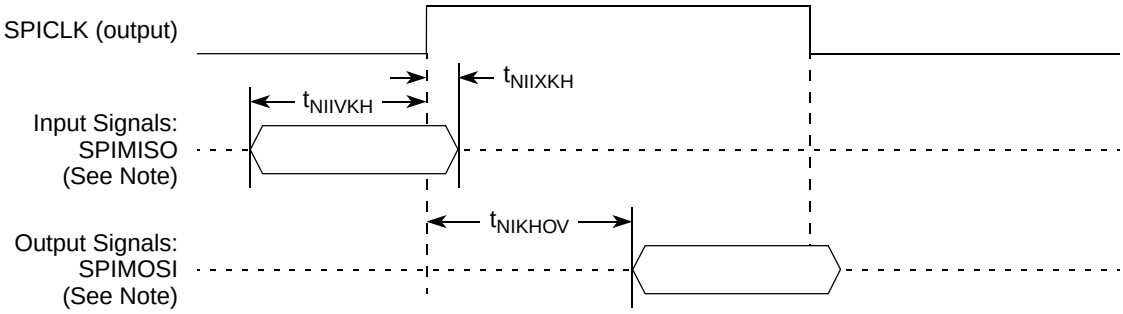
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 51. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8308 is available in a moulded array process ball grid array (MAPBGA). For information on the MAPBGA, see Section 20.1, "Package Parameters for the MPC8308 MAPBGA," and Section 20.2, "Mechanical Dimensions of the MPC8308 MAPBGA."

20.1 Package Parameters for the MPC8308 MAPBGA

The package parameters are as provided in the following list. The package type is 19 mm × 19 mm, 473 MAPBGA.

Package outline	19 mm × 19 mm
Interconnects	473
Pitch	0.80 mm
Module height (typical)	1.39 mm
Solder Balls	96.5 Sn/ 3.5Ag
Ball diameter (typical)	0.40 mm

20.2 Mechanical Dimensions of the MPC8308 MAPBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the MAPBGA package.

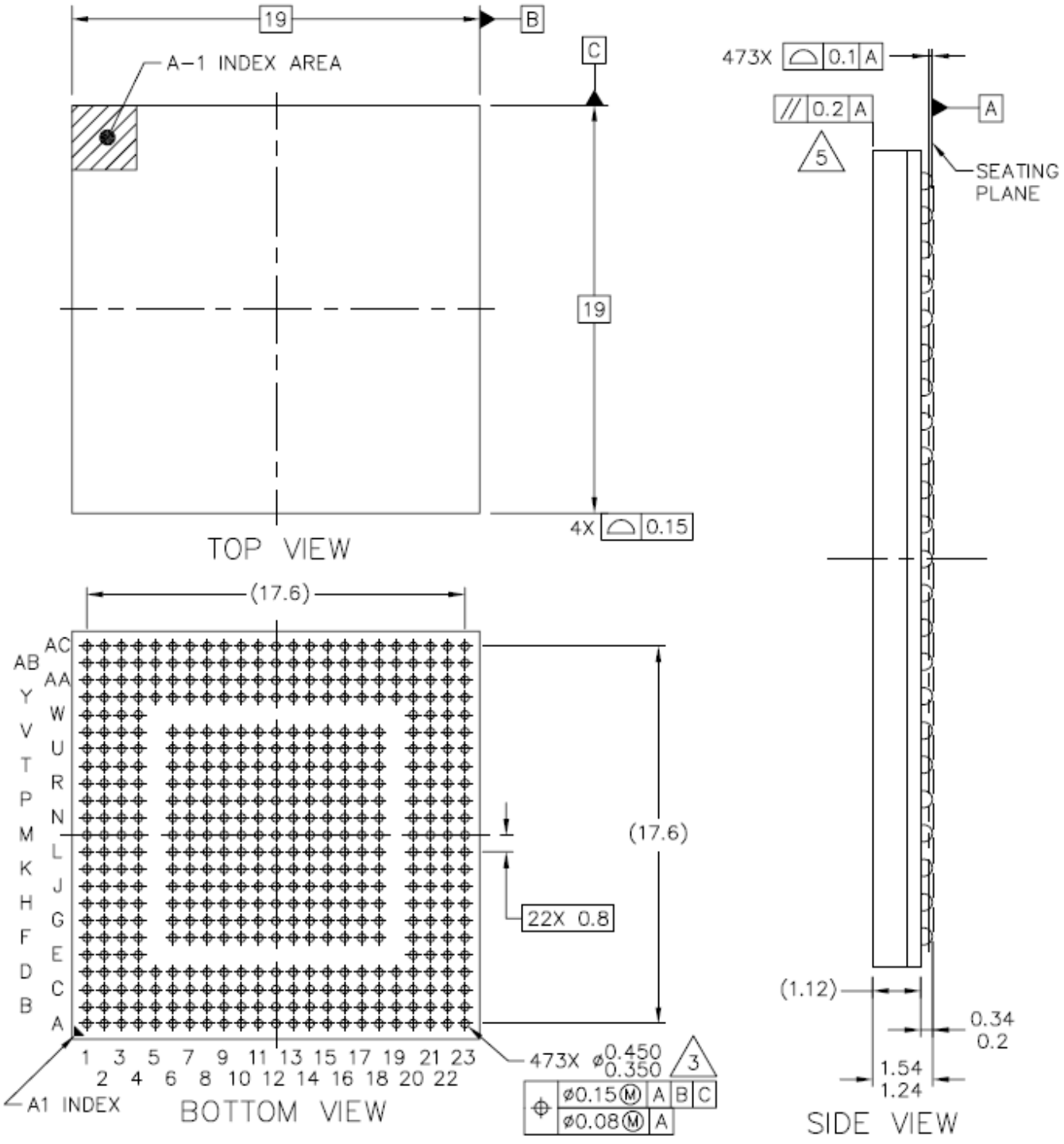


Figure 52. Mechanical Dimension and Bottom Surface Nomenclature of the MPC8308 MAPBG

Notes:
1. All dimensions are in millimeters.

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MEMC\_MCAS}}$	C5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCS}}$[0]	B6	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCS}}$[1]	C6	O	GV_{DDB}	—
MEMC_MCKE	H3	O	GV_{DDB}	3
MEMC_MCK [0]	A3	O	GV_{DDB}	—
MEMC_MCK [1]	U2	O	GV_{DDB}	—
MEMC_MCK [2]	G1	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [0]	A4	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [1]	U1	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [2]	H1	O	GV_{DDB}	—
MEMC_MODT[0]	A5	O	GV_{DDB}	—
MEMC_MODT[1]	B5	O	GV_{DDB}	—
MEMC_MECC[0]	L4	I/O	GV_{DDB}	—
MEMC_MECC[1]	L6	I/O	GV_{DDB}	—
MEMC_MECC[2]	K4	I/O	GV_{DDB}	—
MEMC_MECC[3]	K3	I/O	GV_{DDB}	—
MEMC_MECC[4]	J2	I/O	GV_{DDB}	—
MEMC_MECC[5]	K6	I/O	GV_{DDB}	—
MEMC_MECC[6]	J3	I/O	GV_{DDB}	—
MEMC_MECC[7]	J6	I/O	GV_{DDB}	—
MV_{REF}	G6	I	GV_{DDB}	—
Local Bus Controller Interface				
LD0	U18	I/O	NV_{DDP_K}	8
LD1	V18	I/O	NV_{DDP_K}	8
LD2	U16	I/O	NV_{DDP_K}	8
LD3	Y20	I/O	NV_{DDP_K}	8
LD4	AA21	I/O	NV_{DDP_K}	8
LD5	AC22	I/O	NV_{DDP_K}	8
LD6	V17	I/O	NV_{DDP_K}	8
LD7	AB21	I/O	NV_{DDP_K}	8
LD8	Y19	I/O	NV_{DDP_K}	8
LD9	AA20	I/O	NV_{DDP_K}	8
LD10	Y17	I/O	NV_{DDP_K}	8

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LD11	AC21	I/O	NV_{DDP_K}	8
LD12	AB20	I/O	NV_{DDP_K}	8
LD13	V16	I/O	NV_{DDP_K}	8
LD14	AA19	I/O	NV_{DDP_K}	8
LD15	AC17	I/O	NV_{DDP_K}	8
LA0	AC20	O	NV_{DDP_K}	—
LA1	Y16	O	NV_{DDP_K}	—
LA2	U15	O	NV_{DDP_K}	—
LA3	V15	O	NV_{DDP_K}	—
LA4	AA18	O	NV_{DDP_K}	—
LA5	AA17	O	NV_{DDP_K}	—
LA6	AC19	O	NV_{DDP_K}	—
LA7	AA16	O	NV_{DDP_K}	—
LA8	AB18	O	NV_{DDP_K}	—
LA9	AC18	O	NV_{DDP_K}	—
LA10	V14	O	NV_{DDP_K}	—
LA11	AB17	O	NV_{DDP_K}	—
LA12	AA15	O	NV_{DDP_K}	—
LA13	AC16	O	NV_{DDP_K}	—
LA14	Y14	O	NV_{DDP_K}	—
LA15	AC15	O	NV_{DDP_K}	—
LA16	U13	O	NV_{DDP_K}	—
LA17	V13	O	NV_{DDP_K}	—
LA18	Y13	O	NV_{DDP_K}	—
LA19	AB15	O	NV_{DDP_K}	—
LA20	AA14	O	NV_{DDP_K}	—
LA21	AB14	O	NV_{DDP_K}	—
LA22	U12	O	NV_{DDP_K}	—
LA23	V12	O	NV_{DDP_K}	—
LA24	Y12	O	NV_{DDP_K}	—
LA25	AC14	O	NV_{DDP_K}	—
$\overline{\text{LCS}}$[0]	AA13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[1]	AB13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[2]	AA12	O	NV_{DDP_K}	4

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
IIC_SCL1	A9	I/O	NV_{DDA}	2
IIC_SDA2/$\overline{\text{CKSTOP\_OUT}}$	D10	I/O	NV_{DDA}	2
IIC_SCL2/$\overline{\text{CKSTOP\_IN}}$	C10	I/O	NV_{DDA}	2
Interrupts				
IRQ[0]/$\overline{\text{MCP\_IN}}$	A17	I	NV_{DDB}	—
IRQ[1]/$\overline{\text{MCP\_OUT}}$	F16	I/O	NV_{DDB}	—
IRQ[2] /$\overline{\text{CKSTOP\_OUT}}$	B17	I/O	NV_{DDB}	—
IRQ[3] /$\overline{\text{CKSTOP\_IN}}$	A18	I	NV_{DDB}	—
JTAG				
TCK	Y7	I	NV_{DDP_K}	—
TDI	U9	I	NV_{DDP_K}	4
TDO	AC5	O	NV_{DDP_K}	3
TMS	AA6	I	NV_{DDP_K}	4
$\overline{\text{TRST}}$	V8	I	NV_{DDP_K}	4
TEST				
TEST_MODE	AC6	I	NV_{DDP_K}	5
System Control				
$\overline{\text{HRESET}}$	AA9	I/O	NV_{DDP_K}	1
$\overline{\text{PORESET}}$	AA8	I	NV_{DDP_K}	—
$\overline{\text{SRESET}}$	AB7	I/O	NV_{DDP_K}	—
Clocks				
SYS_CLK_IN	AC8	I	NV_{DDP_K}	—
RTC_PIT_CLOCK	AA23	I	NV_{DDJ}	—
MISC				
QUIESCE	AA7	O	NV_{DDP_K}	—
THERM0	AC7	I	NV_{DDP_K}	6
ETSEC1				
TSEC1_COL	B20	I	NV_{DDC}	—
TSEC1_CRS	B21	I	NV_{DDC}	—
TSEC1_GTX_CLK	F18	O	NV_{DDC}	3
TSEC1_RX_CLK	A22	I	NV_{DDC}	—
TSEC1_RX_DV	D21	I	NV_{DDC}	—
TSEC1_RXD[3]	C22	I	NV_{DDC}	—
TSEC1_RXD[2]	C21	I	NV_{DDC}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC1_RXD[1]	C20	I	NV_{DDC}	—
TSEC1_RXD[0]	D20	I	NV_{DDC}	—
TSEC1_RX_ER	C23	I	NV_{DDC}	—
TSEC1_TX_CLK/ TSEC1_GTX_CLK125	E23	I	NV_{DDC}	—
TSEC1_TXD[3]/ CFG_RESET_SOURCE[0]	F22	I/O	NV_{DDC}	—
TSEC1_TXD[2]/ CFG_RESET_SOURCE[1]	F21	I/O	NV_{DDC}	—
TSEC1_TXD[1]/ CFG_RESET_SOURCE[2]	E21	I/O	NV_{DDC}	—
TSEC1_TXD[0]/ CFG_RESET_SOURCE[3]	D22	I/O	NV_{DDC}	—
TSEC1_TX_EN/ LBC_PM_REF_10	F20	O	NV_{DDC}	—
TSEC1_TX_ER/ LB_POR_CFG_BOOT_ECC	E22	I/O	NV_{DDC}	7
Ethernet Mgmt				
TSEC1_MDC	A20	O	NV_{DDB}	—
TSEC1_MDIO	C19	I/O	NV_{DDB}	2
eSDHC/GTM				
SD_CLK/GPIO[16]	D7	O	NV_{DDA}	—
SD_CMD/GPIO[17]	G9	I/O	NV_{DDA}	—
$\overline{\text{SD\_CD}}$/GTM1_TIN1/ GPIO[18]	A7	I	NV_{DDA}	—
SD_WP/$\overline{\text{GTM1\_TGATE1}}$/ GPIO[19]	D8	I	NV_{DDA}	—
SD_DAT[0]/$\overline{\text{GTM1\_TOUT1}}$/ GPIO[20]	C8	I/O	NV_{DDA}	—
SD_DAT[1]/$\overline{\text{GTM1\_TOUT2}}$/ GPIO[21]	B8	I/O	NV_{DDA}	—
SD_DAT[2]/GTM1_TIN2/ GPIO[22]	A8	I/O	NV_{DDA}	—
SD_DAT[3]/$\overline{\text{GTM1\_TGATE2}}$/ GPIO[23]	B9	I/O	NV_{DDA}	—
SPI				
SPIMOSI/MSRCID4/ LSRCID4	AB5	I/O	NV_{DDP_K}	—
SPIMISO/MDVAL/LDVAL	Y6	I/O	NV_{DDP_K}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	Y23, H8, H9, H10, H14, H15, H16, J8, J16, K8, K16, L8, L16, M8, M16, N8, N16, P8, P16, R8, R16, T8, T9, T10, T11, T12, T13, T14, T15, T16	I	—	—
VSS	A2, A21, B1, B19, B23, C4, C16, D6, D19, E3, F8, F15, F17, F23, G7, G8, G10, G15, G16, G17, G20, H2, H6, H7, H17, H23, J7, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, K15, L1, L7, L9, L10, L11, L12, L13, L14, L15, L20, M4, M9, M10, M11, M12, M13, M14, M15, N9, N10, N11, N12, N13, N14, N15, P6, P7, P9, P10, P11, P12, P13, P14, P15, R2, R7, R9, R10, R11, R12, R13, R14, R15, R22, T6, T7, U8, U17, U21, V2, V7, V9, V11, W20, Y8, Y15, AA4, AB1, AB6, AB12, AB19, AC2, AC9, AC23	I	—	—
NV_{DDA}	B7, B10, C7, D9, F9	I	—	—
NV_{DDB}	A16, A19, C18	I	—	—
NV_{DDC}	A23, B22, D23, E20, G18	I	—	—
NV_{DDF}	G22, J22, K17	I	—	—
NV_{DDG}	M17, N22	I	—	—
NV_{DDH}	P17, R20, T17, T23, W22, Y22	I	—	—
NV_{DDJ}	AB23, AA22	I	—	—
NV_{DDP_K}	U10, U14, Y5, Y18, AA11, AB8, AB16, AB22, AC4, AC13	I	—	—
GV_{DD}	A1, A6, B3, D1, F1, F6, G4, J1, J4, K7, N1, N7, T1, T4, U7, Y3, AC1	I	—	—
XPADVDD	D15, F10, F14	I	—	—
XPADVSS	A10, B15, D14, G13, G14, H12	I	—	—
XCOREVDD	A14, B12, C13	I	—	—
XCOREVSS	A12, B14, C11, D11, D13, G11, H11, H13	I	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. This pin has weak internal pull-up that is always enabled. 5. This pin must always be tied to VSS.
6. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
7. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a buffer released to high impedance is needed.
8. This pin has weak internal pull-down that is always enabled

appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)
T_B = board temperature at the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)
T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the device

23.1 System Clocking

The device includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 21.2, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.3, “Core PLL Configuration.”

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} for core PLL and AV_{DD2} for the platform PLL). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low pass filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 54, one to each of the two AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs’ resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

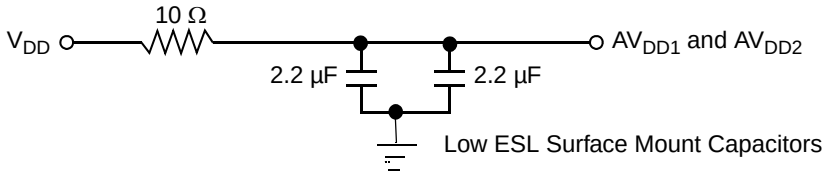


Figure 54. PLL Power Supply Filter Circuit

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