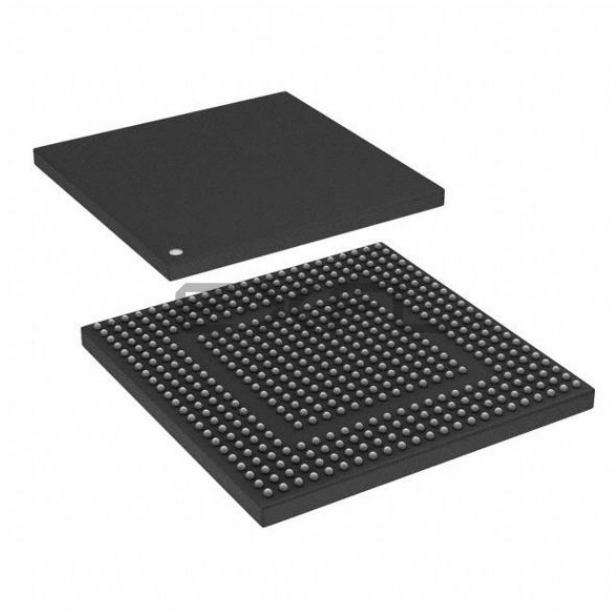

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8308vmagd

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.45	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.45	—	V	—

This table provides input AC timing specifications for the DDR2 SDRAM interface.

Table 17. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 1.8± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC 266 MHz	t_{CISKEW}	–875	875	ps	1, 2,3

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ or MECC signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = +/–(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Memory controller ODT value of 150 Ω is recommended

This figure shows the DDR2 SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

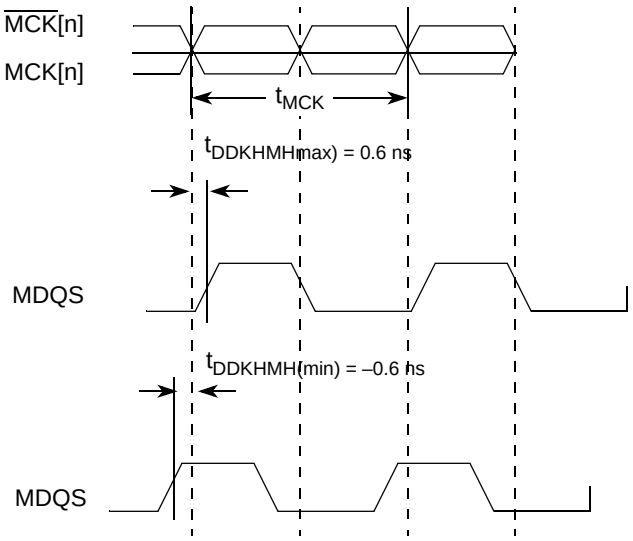


Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR2 SDRAM output timing diagram.

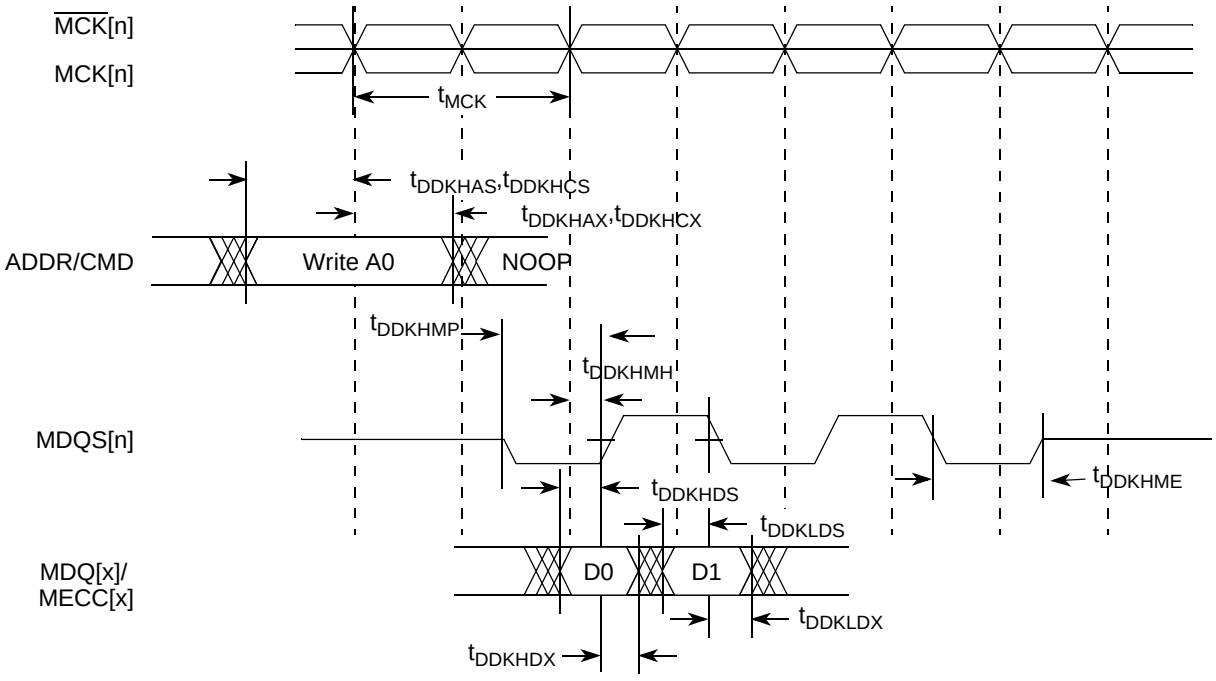


Figure 6. DDR2 SDRAM Output Timing Diagram

This figure provides the AC test load for the DDR2 bus.

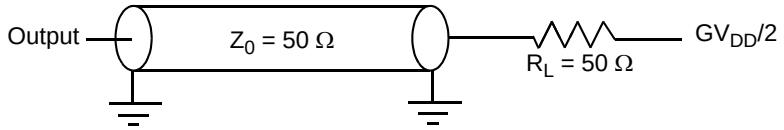


Figure 7. DDR2 AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.1	NV_{DD} + 0.3	V
Low-level input voltage NVDD	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	NV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NV_{DD})	I_{IN}	—	± 5	μA

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management. MPC8308 supports dual Ethernet controllers.

9.1.2 USB AC Electrical Specifications

This table lists the general timing parameters of the USB-ULPI interface.

Table 31. USB General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	1, 2
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	1, 4
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	1, 4
USB clock to output valid—all outputs	t_{USKHOV}	—	9	ns	1
Output hold from USB clock—all outputs	t_{USKHOX}	1	—	ns	1

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes usb timing (US) for the input (I) to go invalid (X) with respect to the time the usb clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes usb timing (US) for the usb clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from NVDD/2 of the rising edge of USB clock to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

The following two figures provide the AC test load and signals for the USB, respectively.

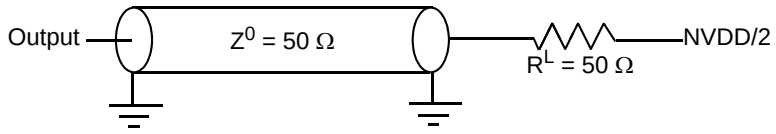


Figure 13. USB AC Test Load

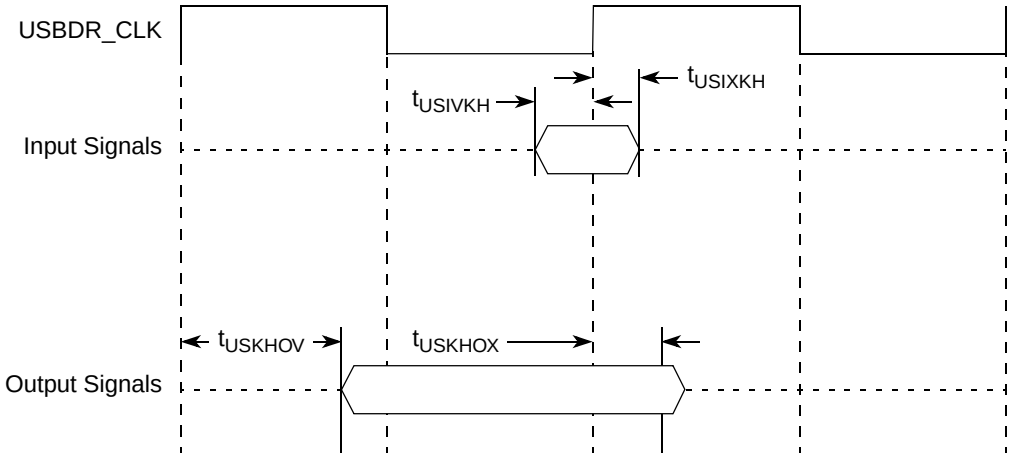


Figure 14. USB Signals

10 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

10.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 15 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX*n* and $\overline{\text{TX}n}$) or a receiver input (RX*n* and $\overline{\text{RX}n}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- **Single-Ended Swing**

  The transmitter output signals and the receiver input signals TX*n*, $\overline{\text{TX}n}$, RX*n*, and $\overline{\text{RX}n}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's single-ended swing.
- **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**)

  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.
- **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**)

  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.
- **Differential Peak Voltage, V_{DIFFp}**

  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, V_{DIFFp} = |A – B| Volts.
- **Differential Peak-to-Peak, $V_{DIFFp-p}$**

  Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.
- **Differential Waveform**

  The differential waveform is constructed by subtracting the inverting signal (for example, $\overline{\text{TX}n}$) from the non-inverting signal (for example, TX*n*) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 24 as an example for differential waveform.

10.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8308 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 10.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 17 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 18 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 19 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

Table 32. SerDes Reference Clock AC Parameters (continued)

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
Rising edge rate (SD_REF_CLK) to falling edge rate ($\overline{\text{SD\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing (Figure 24).
4. Matching applies to rising edge rate for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate (See Figure 25).

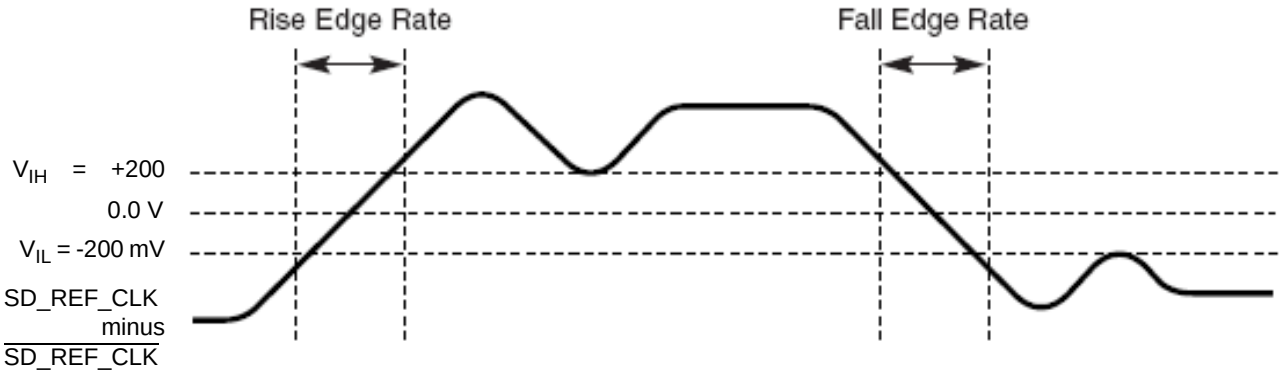


Figure 24. Differential Measurement Points for Rise and Fall Time

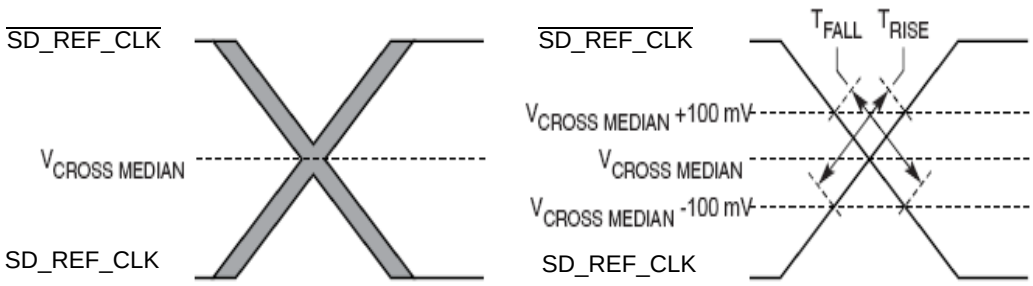


Figure 25. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. For detailed information, see the following sections:

- Section 11.2, “AC Requirements for PCI Express SerDes Clocks”

Table 34. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Absolute delta of DC common mode voltage during L0 and electrical idle	$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	$\lvert V_{TX\text{-}CM\text{-}DC\ (during\ L0)} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ (During\ Electrical\ Idle)}\rvert <= 100$ mV $V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [L0] $V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [Electrical Idle]	0	—	100	mV	2
Absolute delta of DC common mode between D+ and D–	$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	$\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-}\rvert <= 25$ mV $V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+}\rvert$ $V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D-}\rvert$	0	—	25	mV	2
Electrical idle differential peak output voltage	$V_{TX\text{-}IDLE\text{-}DIFFp}$	$V_{PEEIDPTX} = \lvert V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-}\rvert <= 20$ mV	0	—	20	mV	2
Amount of voltage change allowed during receiver detection	$V_{TX\text{-}RCV\text{-}DETECT}$	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present.	—	600	—	mV	6
TX DC common mode voltage	$V_{TX\text{-}DC\text{-}CM}$	The allowed DC Common Mode voltage under any conditions.	—	3.6	—	V	6
TX short circuit current limit	$I_{TX\text{-}SHORT}$	The total current the Transmitter can provide when shorted to its ground	—	—	90	mA	—
Minimum time spent in electrical idle	$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set	50	—	—	UI	—
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.	—	—	20	UI	—
Maximum time to transition to valid TX specifications after leaving an electrical idle condition	$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle	—	—	20	UI	—
Differential return loss	$RL_{TX\text{-}DIFF}$	Measured over 50 MHz to 1.25 GHz.	12	—	—	dB	4
Common mode return loss	$RL_{TX\text{-}CM}$	Measured over 50 MHz to 1.25 GHz.	6	—	—	dB	4
DC differential TX impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	TX DC Differential mode Low Impedance	80	100	120	Ω	—
Transmitter DC impedance	$Z_{TX\text{-}DC}$	Required TX D+ as well as D- DC Impedance during all states	40	—	—	Ω	—
Lane-to-Lane output skew	$L_{TX\text{-}SKEW}$	Static skew between any two Transmitter Lanes within a single Link	—	—	500 + 2 UI	ps	—

13.3.1 High Speed Output Path (Write)

This figure provides the data and command output timing diagram.

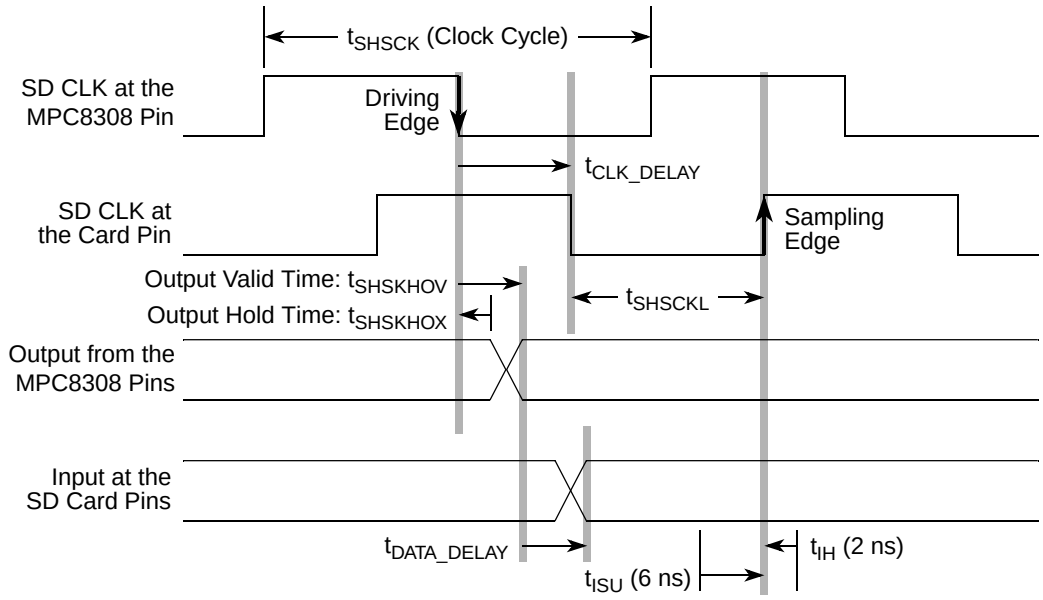


Figure 38. High Speed Output Path

13.3.2 High Speed Input Path (Read)

This figure provides the data and command input timing diagram.

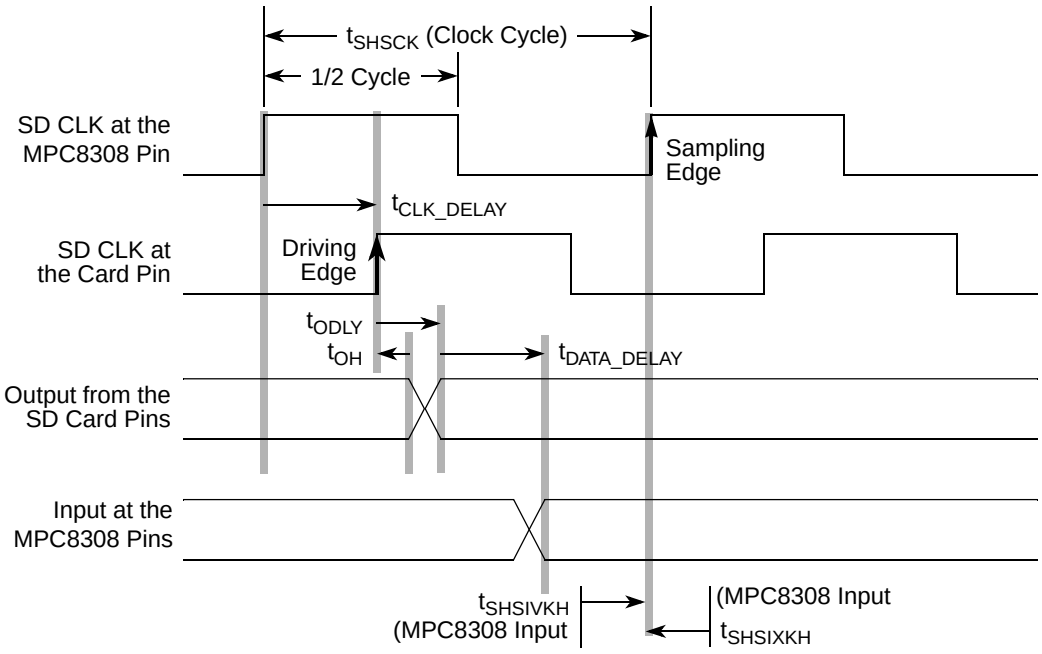


Figure 39. High Speed Input Path

15 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

15.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 43. I²C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times NV_{DD}$	$NV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times NV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times NV_{DD}$	V	1
High level output voltage	V_{OH}	$0.8 \times NV_{DD}$	$NV_{DD} + 0.3$	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current, ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	μA	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. For information on the digital filter used, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

15.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface.

Table 44. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	μs
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns

17 GPIO

This section describes the DC and AC electrical specifications for the GPIO of MPC8308

17.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO.

Table 47. GPIO DC Electrical Characteristic

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

17.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 48. GPIO Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

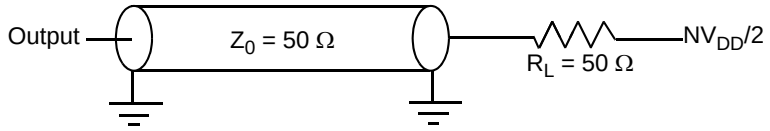


Figure 48. GPIO AC Test Load

18 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

18.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 49. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

18.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 50. IPIC Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

19 SPI

This section describes the DC and AC electrical specifications for the SPI of the device.

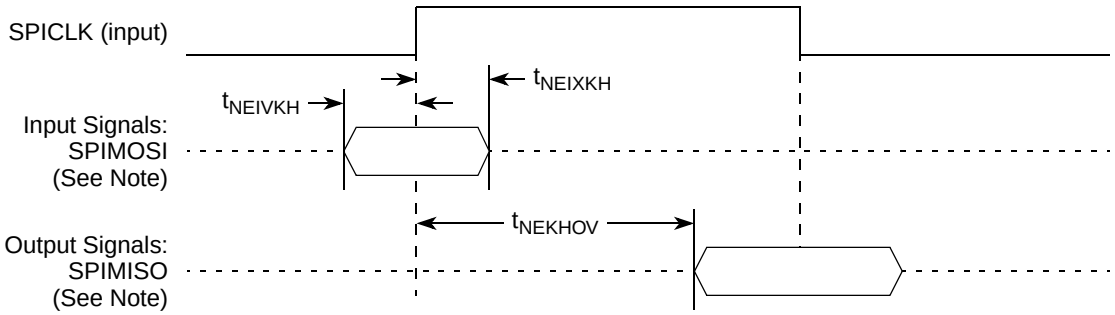
19.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8308 SPI.

Table 51. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

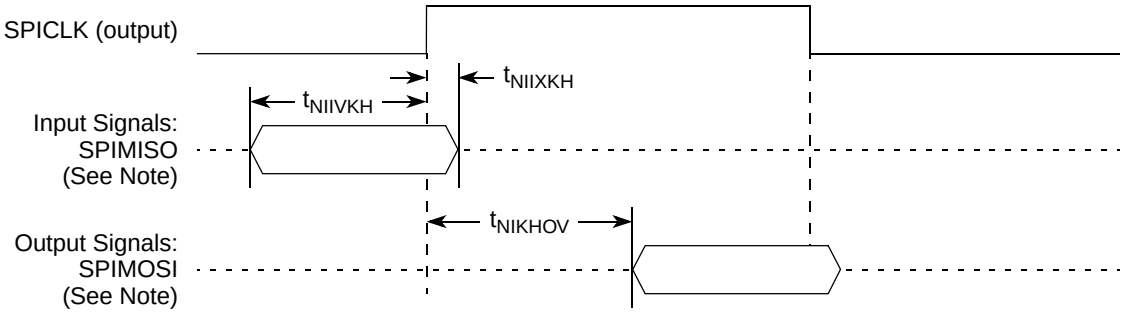
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 51. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8308 is available in a moulded array process ball grid array (MAPBGA). For information on the MAPBGA, see Section 20.1, "Package Parameters for the MPC8308 MAPBGA," and Section 20.2, "Mechanical Dimensions of the MPC8308 MAPBGA."

20.1 Package Parameters for the MPC8308 MAPBGA

The package parameters are as provided in the following list. The package type is 19 mm × 19 mm, 473 MAPBGA.

Package outline	19 mm × 19 mm
Interconnects	473
Pitch	0.80 mm
Module height (typical)	1.39 mm
Solder Balls	96.5 Sn/ 3.5Ag
Ball diameter (typical)	0.40 mm

20.2 Mechanical Dimensions of the MPC8308 MAPBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the MAPBGA package.

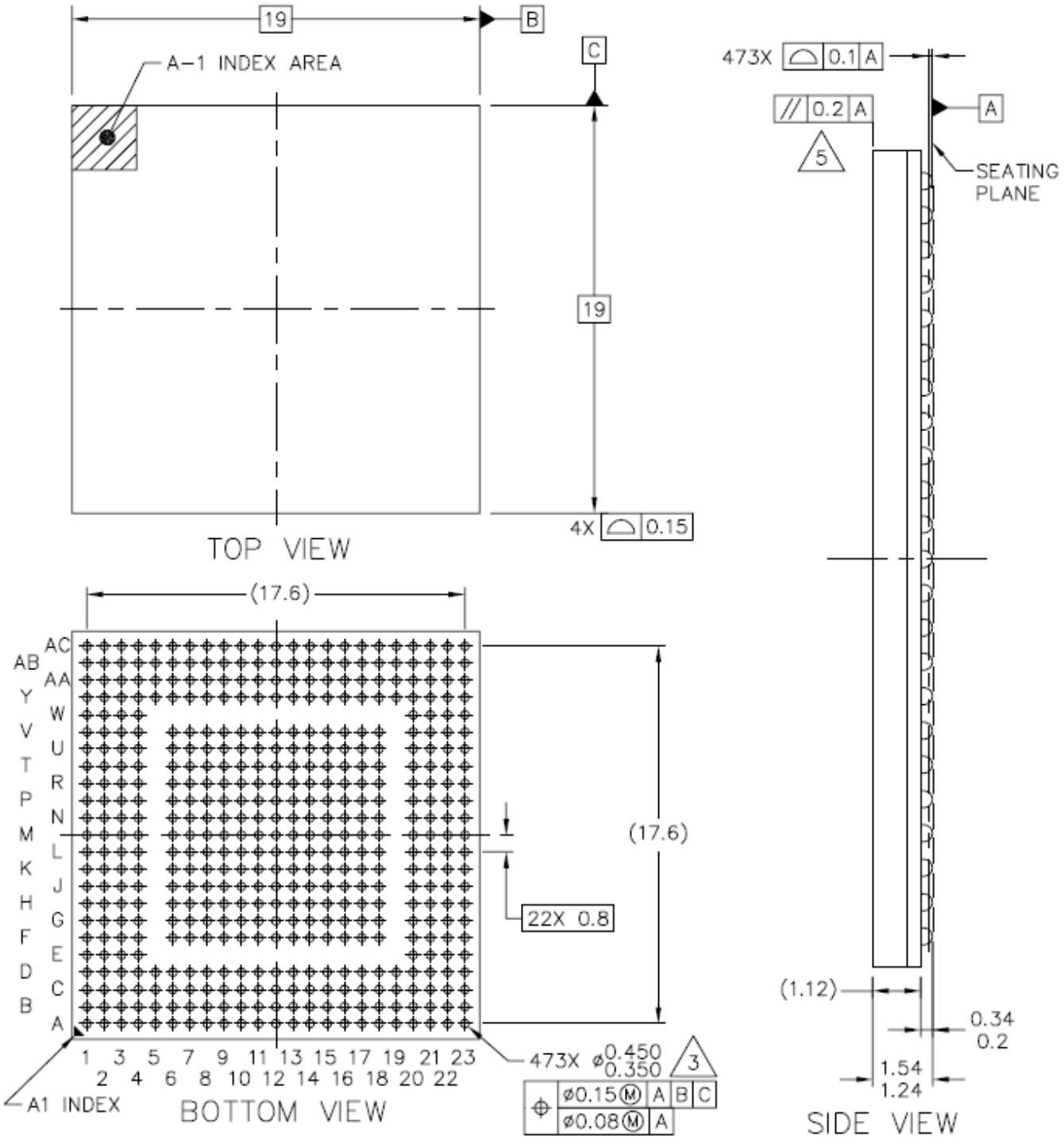


Figure 52. Mechanical Dimension and Bottom Surface Nomenclature of the MPC8308 MAPBG

Notes:
1. All dimensions are in millimeters.

21.1 System Clock Domains

The primary clock input (SYS_CLK_IN) frequency is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus interface unit (*lbc_clk*)

The *csb_clk* frequency is derived as follows:

csb_clk = [SYS_CLK_IN] × SPMF

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. For more information, see the Reset Clock Configuration chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

The DDR SDRAM memory controller will operate with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller will operate with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK0:2). The LBC clock divider ratio is controlled by LCCR[CLKDIV]. For more information, see the Reset Clock Configuration chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 54 specifies which units have a configurable clock frequency. For more information, see Reset Clock Configuration chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

Table 54. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1,eTSEC2	*csb_clk/3*	Off, *csb_clk, csb_clk/2, csb_clk/3*
I^2C	*csb_clk*	Off, *csb_clk*,*csb_clk*/2, *csb_clk*/3
DMA complex	*csb_clk*	Off, *csb_clk*,*csb_clk/2*,*csb_clk/3*
PCIEXP	*csb_clk*	Off, *csb_clk*
eSDHC	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
USB	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*

NOTE

The clock ratios of these units must be set before they are accessed.

This table provides the operating frequencies for the device under recommended operating conditions (Table 2).

Table 55. Operating Frequencies for MPC8308

Characteristic[1]	Maximum Operating Frequency	Unit
e300 core frequency (*core_clk*)	400	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
DDR2 memory bus frequency (MCK)[2]	133	MHz
Local bus frequency (LCLK*0*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK0, and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCCR[CLKDIV]) which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

21.2 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

Table 56. System PLL Ratio

RCWL[SPMF]	csb_clk: SYS_CLK_IN
0000	Reserved
0001	Reserved
0010	2 : 1
0011	3 : 1
0100	4 : 1
0101	5 : 1
0110–1111	Reserved

As described in Section 21, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (SYS_CLK_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN ratios.

Table 57. CSB Frequency Options

SPMF *csb_clk* :Input Clock Ratio		Input Clock Frequency (MHz)		
		25	33.33	66.67
0010	2:1			133
0100	4:1		133	
0101	5:1	125	167	

appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)
T_B = board temperature at the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)
T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the device

23.1 System Clocking

The device includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 21.2, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.3, “Core PLL Configuration.”

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} for core PLL and AV_{DD2} for the platform PLL). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low pass filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 54, one to each of the two AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs’ resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

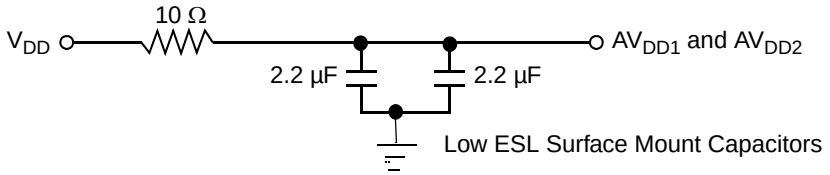
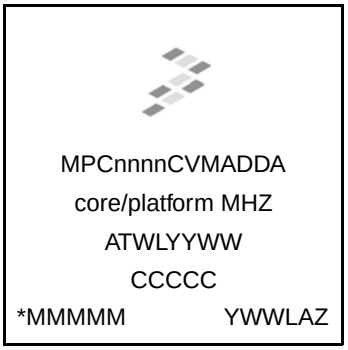


Figure 54. PLL Power Supply Filter Circuit

24.2 Part Marking

Parts are marked as in the example shown in this figure.



PBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 56. Freescale Part Marking for PBGA Devices

This table lists the SVR settings.

Table 62. SVR Settings

Device	Package	SVR
MPC8308	MAPBGA	0x8101 _0110

Note: PVR = 8085_0020 for the device.

25 Document Revision History

This table summarizes a revision history for this document.

Table 63. Document Revision History

Rev. Number	Date	Substantive Change(s)
3	10/2011	• In Section 2.1.4, "Power Sequencing," changed description. • In Table 53, updated GPIOs pins as I/O. • In Table 54, removed PCI Express = csb_clk/2 and csb_clk/3 options. • In Table 61, added note 4.
2	02/2011	• Added NV_{DDJ} to Note-7 in Table 1. • In Table 2, Added Note-2 Added NV_{DDJ} to Note-3 Added "Extended Temperature range from -40 to 105 °C, in the last row of the table Changed "characteristic name Junction temperature" to "Operating temperature range" • In Table 4, Note-3, changed ambient temperature to junction temperature, T_J = 105° C • In Table 18, t_{DDKHCS} changed from 3.15ns to 2.5ns t_{DDKHMP} and t_{DDKHME} values updated • In Figure 6, corrected t_{DDKHMP} & t_{DDKHME} waveform • In Table 53, Y23 Package Pin Number changed from NC to V_{DD} signal group TSEC2_CRS is muxed with GPIO[0], shown as TSEC2_CRS/ GPIO[0] • In Table 58, note-1, core_clk maximum operating frequency 333 MHz replaced with 400 MHz
1	06/2010	• In Table 4, T_A = 105 replaced with T_J = 105 • In Table 8, $f_{SYS\_CLK\_IN}$ (Max) = 66 replaced with 66.67 and $t_{SYS\_CLK\_IN}$ (Min) = 15.15 replaced with 15 • In Table 53, TSEC1_TMR_RX_ESFD replaced with TSEC2_TMR_RX_ESFD TSEC1_TMR_TX_ESFD replaced with TSEC2_TMR_TX_ESFD TSEC0_TMR_RX_ESFD replaced with TSEC1_TMR_RX_ESFD TSEC0_TMR_TX_ESFD replaced with TSEC1_TMR_TX_ESFD • In Table 56, rows from 1000 to 1111 removed • In Table 57, SPMF 5:1 Option 167 MHz added.
0	05/2010	Initial release