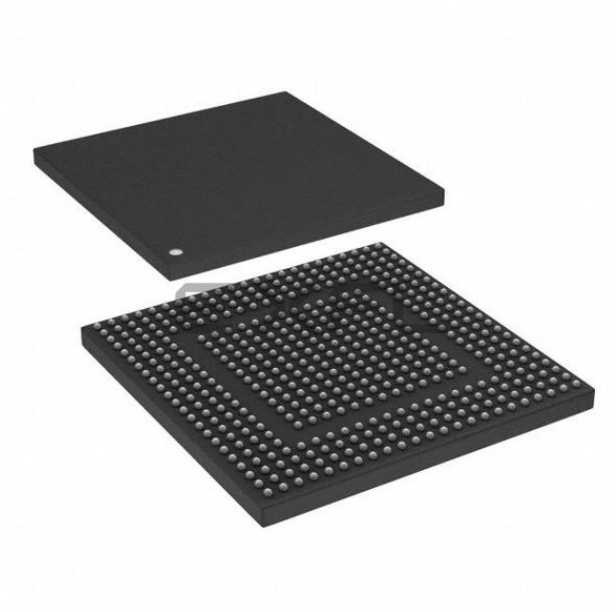

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Last Time Buy |
| Core Processor | PowerPC e300c3 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (3) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 473-LFBGA |
| Supplier Device Package | 473-MAPBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8308vmagda |

## 2.1.1 Absolute Maximum Ratings

This table lists the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 1.26 | V | — |
| PLL supply voltage | | $AV_{DD1}$, $AV_{DD2}$ | –0.3 to 1.26 | V | — |
| DDR2 DRAM I/O voltage | | $GV_{DD}$ | –0.3 to 1.9 | V | — |
| Local bus, DUART, system control and power management, eSDHC, $I^2C$, USB, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage | | $NV_{DD}$ | –0.3 to 3.6 | V | 7 |
| SerDes PHY | | $XCOREV_{DD}$, $XPADV_{DD}$, $SDAV_{DD}$ | –0.3 to 1.26 | V | — |
| eTSEC I/O Voltage | | $LV_{DD1}$, $LV_{DD2}$ | –0.3 to 2.75 or –0.3 to 3.6 | V | 6, 8 |
| Input voltage | DDR2 DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | DDR2 DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | eTSEC | $LV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3) | V | 4, 5,8 |
| | Local bus, DUART, system control and power management, eSDHC, $I^2C$, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage | $OV_{IN}$ | –0.3 to ($NV_{DD}$ + 0.3) | V | 3, 5,7 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $NV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $LV_{IN}$ must not exceed $LV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M, L, O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2
6. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
7. $NV_{DD}$ here refers to $NV_{DDA}$, $NV_{DDB}$,$NV_{DDG}$, $NV_{DDH}$, $NV_{DDJ}$, $NV_{DDP\_K}$ from the ball map.
8. $LV_{DD1}$ here refers to $NV_{DDC}$ and $LV_{DD2}$ refers to $NV_{DDF}$ from the ball map

## 2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

## 5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

**Table 11. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ (input) to activate reset flow | 32 | — | $t_{SYS\_CLK\_IN}$ | 1 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable power and clock applied to SYS_CLK_IN | 32 | — | $t_{SYS\_CLK\_IN}$ | — |
| $\overline{\text{HRESET}}$ assertion (output) | 512 | — | $t_{SYS\_CLK\_IN}$ | 1 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of PORESET | 4 | — | $t_{SYS\_CLK\_IN}$ | — |
| Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | — |
| Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$ | — | 4 | ns | 2 |
| Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$ | 1 | — | ns | 1, 2 |

**Notes:**
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN.
2. POR configuration signals consists of CFG_RESET_SOURCE[0:3].

This table provides the PLL lock times.

**Table 12. PLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Note |
|---|---|---|---|---|
| System PLL lock time | — | 100 | μs | — |
| e300 core PLL lock time | — | 100 | μs | — |

This figure illustrates the DDR2 input timing diagram showing the $t_{DISKEW}$ timing parameter.

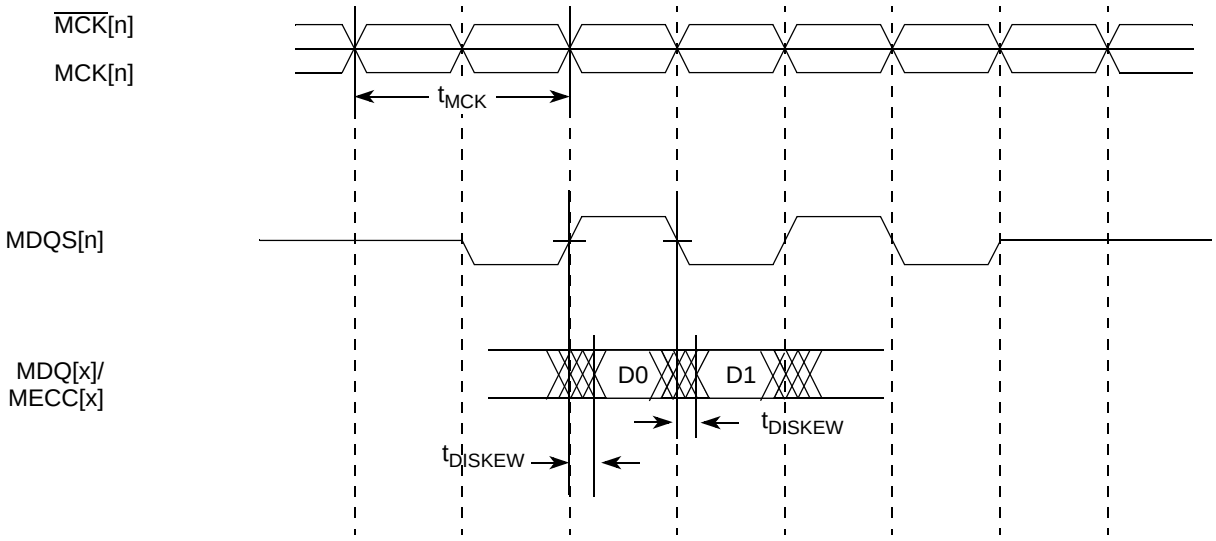


**Figure 4. Timing Diagram for $t_{DISKEW}$**

## 6.2.2 DDR2 SDRAM Output AC Timing Specifications

**Table 18. DDR2 SDRAM Output AC Timing Specifications**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing | $t_{MCK}$ | 7.5 | 10 | ns | 2 |
| ADDR/CMD output setup with respect to MCK | $t_{DDKHAS}$ | | — | ns | 3 |
| 266 MHz | | 2.9 | | | |
| ADDR/CMD output hold with respect to MCK | $t_{DDKHAX}$ | | — | ns | 3 |
| 266 MHz | | 2.33 | | | |
| $\overline{\text{MCS}}$[n] output setup with respect to MCK | $t_{DDKHCS}$ | | — | ns | 3 |
| | | | | | |
| 266 MHz | | 2.5 | | | |
| $\overline{\text{MCS}}$[n] output hold with respect to MCK | $t_{DDKHCX}$ | | — | ns | 3 |
| 266 MHz | | 3.15 | | | |
| MCK to MDQS Skew | $t_{DDKHMH}$ | –0.6 | 0.6 | ns | 4 |

**Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MDQ//MDM/MECC output setup with respect to MDQS | $t_{DDKHDS}$, $t_{DDKLDS}$ | | — | ps | 5 |
| 266 MHz | | 900 | | | |
| MDQ//MDM/MECC output hold with respect to MDQS | $t_{DDKHDX}$, $t_{DDKLDX}$ | | — | ps | 5 |
| 266 MHz | | 1100 | | | |
| MDQS preamble start | $t_{DDKHMP}$ | 0.75 x $t_{MCK}$ | — | ns | 6 |
| MDQS epilogue end | $t_{DDKHME}$ | 0.4 x $t_{MCK}$ | 0.6 x $t_{MCK}$ | ns | 6 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.

This figure shows the DDR2 SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

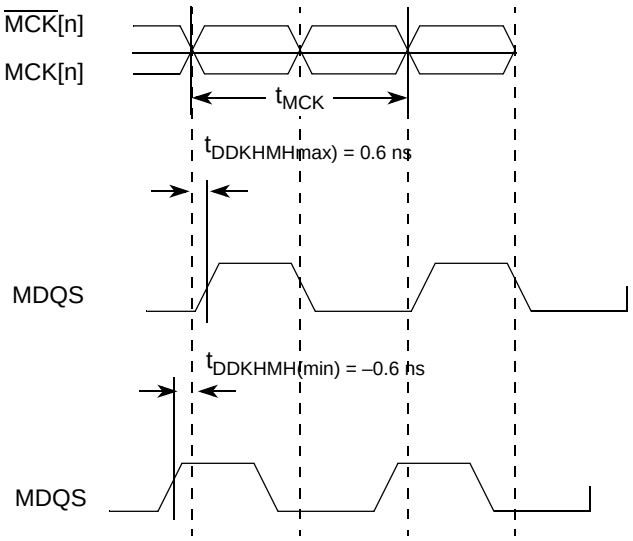


**Figure 5. Timing Diagram for $t_{DDKHMH}$**

This figure shows the DDR2 SDRAM output timing diagram.

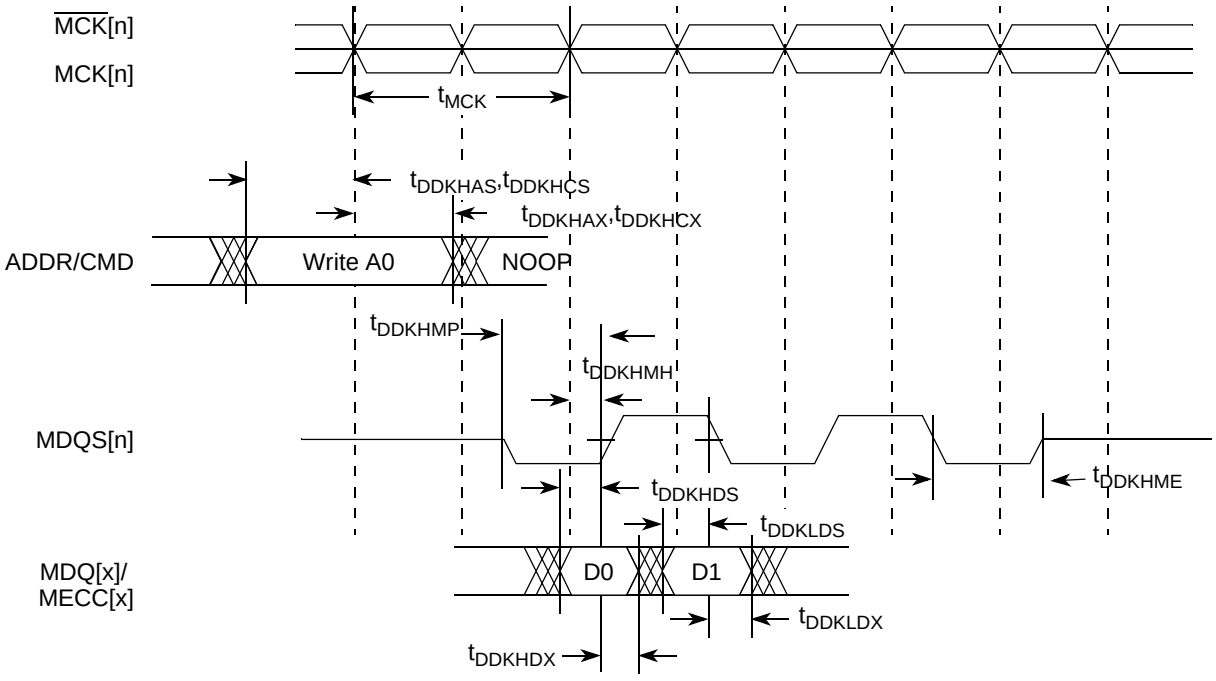


**Figure 6. DDR2 SDRAM Output Timing Diagram**

This figure provides the AC test load for the DDR2 bus.

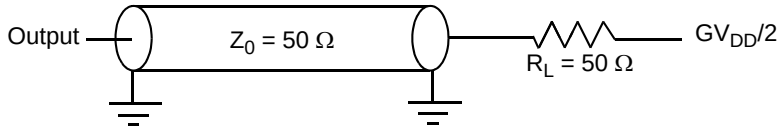


**Figure 7. DDR2 AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

## 7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

**Table 19. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2.1 | $NV_{DD}$ + 0.3 | V |
| Low-level input voltage NVDD | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $NV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |
| Input current (0 V ≤$V_{IN}$ ≤ $NV_{DD}$) | $I_{IN}$ | — | ± 5 | μA |

## 7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

**Table 20. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | 256 | baud | — |
| Maximum baud rate | > 1,000,000 | baud | 1 |
| Oversample rate | 16 | — | 2 |

**Notes:**
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8$^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16$^{th}$ sample.

# 8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management. MPC8308 supports dual Ethernet controllers.

This figure shows the MII receive AC timing diagram.

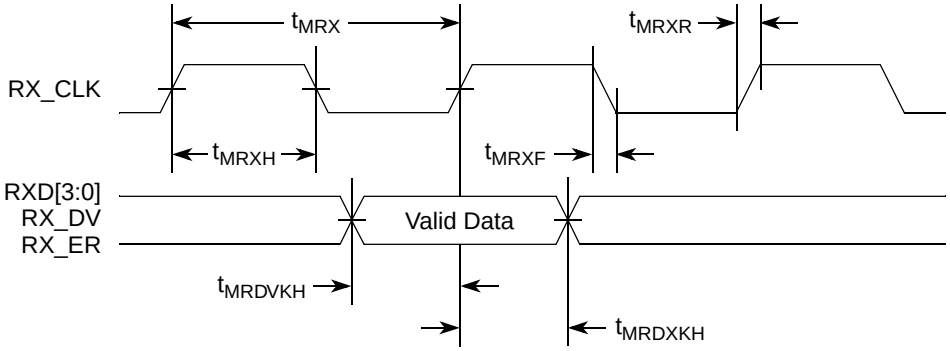


**Figure 9. MII Receive AC Timing Diagram RMII AC Timing Specifications**

This figure provides the AC test load.

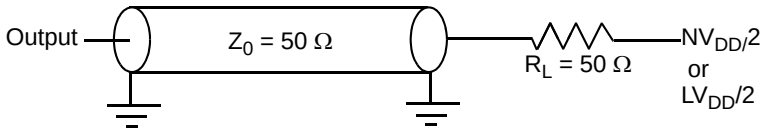


**Figure 10. AC Test Load**

## 8.2.2 RGMII AC Timing Specifications

This table presents the RGMII AC timing specifications.

**Table 25. RGMII AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$ | –0.6 | — | 0.6 | ns |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.6 | ns |
| Clock cycle duration [3] | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 1000Base-T [4, 5] | $t_{RGTH}/t_{RGT}$ | 45 | 50 | 55 | % |
| Duty cycle for 10BASE-T and 100BASE-TX [3, 5] | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns |

**Table 25. RGMII AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}$ of 2.5 V ± 5%.

| | | | | | |
|---|---|---|---|---|---|
| GTX_CLK125 reference clock period | $t_{G12}$ [6] | — | 8.0 | — | ns |
| GTX_CLK125 reference clock duty cycle | $t_{G125H}/t_{G125}$ | 47 | — | 53 | % |

**Notes:**

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of $t_{RGT}$ represents the RGMII receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. Duty cycle reference is $0.5*LV_{DD}$
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

This figure shows the RGMII AC timing and multiplexing diagrams.

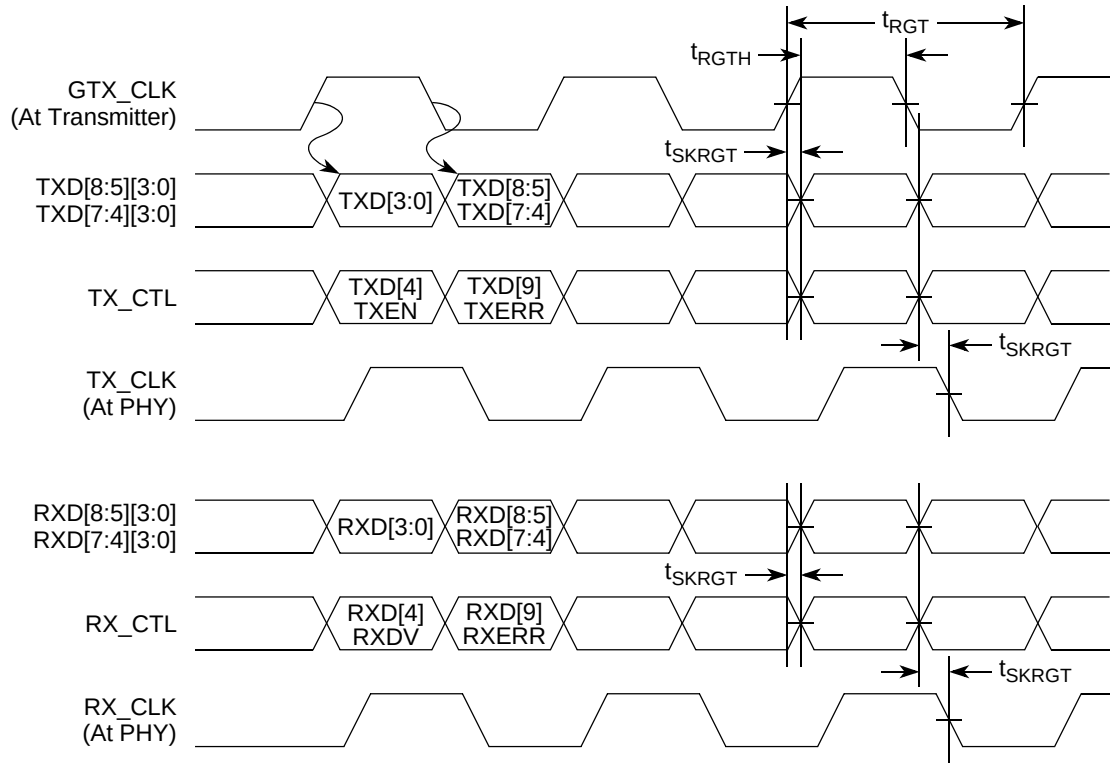


**Figure 11. RGMII AC Timing and Multiplexing Diagrams**

## 8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII

and RGMII are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII Electrical Characteristics."

### 8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. This table provides the DC electrical characteristics for MDIO and MDC.

**Table 26. MII Management DC Electrical Characteristics When Powered at 3.3 V**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (3.3 V) | $NV_{DD}$ | — | | 3.0 | 3.6 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $NV_{DD}$ = Min | 2.10 | $NV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $LV_{DD}$ = Min | VSS | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | | 2.0 | — | V |
| Input low voltage | $V_{IL}$ | — | | — | 0.80 | V |
| Input high current | $I_{IH}$ | $NV_{DD}$ = Max | $V_{IN}$ [1] = 2.1 V | — | 40 | μA |
| Input low current | $I_{IL}$ | $NV_{DD}$ = Max | $V_{IN}$ = 0.5 V | –600 | — | μA |

**Note:**
1. $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

### 8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

**Table 27. MII Management AC Timing Specifications**

At recommended operating conditions with $LV_{DDA}/LV_{DDB}$ is 3.3 V ± 0.3V

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | 2 |
| MDC period | $t_{MDC}$ | — | 400 | — | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO delay | $t_{MDKHDX}$ | 10 | — | 170 | ns | 3 |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |

**Table 27. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DDA}/LV_{DDB}$ is 3.3 V ± 0.3V

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols used for timing specifications Follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)
3. This parameter is dependent on the cbs_clk speed (that is, for a csb_clk of 133 MHz, the delay is 60 ns).

This figure shows the MII management AC timing diagram.

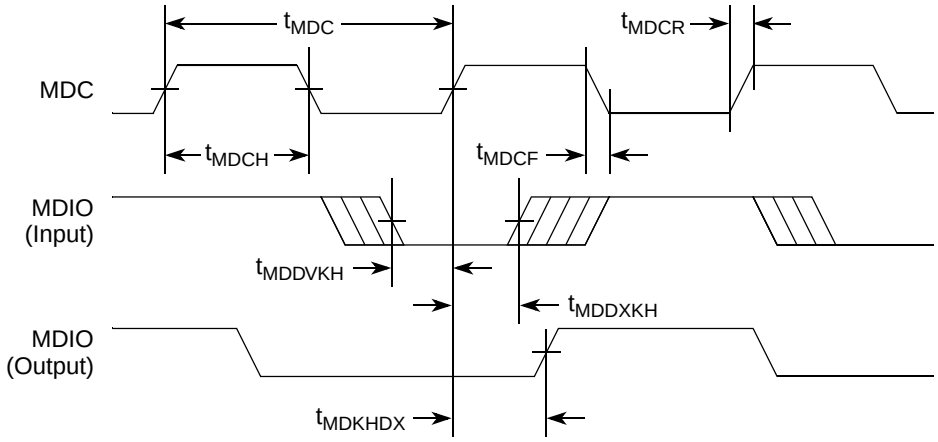


**Figure 12. MII Management Interface Timing Diagram**

## 8.4 IEEE Std 1588™ Timer Specifications

This section describes the DC and AC electrical specifications for the 1588 timer.

### 8.4.1 IEEE 1588 Timer DC Specifications

This table provides the IEEE 1588 timer DC specifications.

**Table 28. GPIO DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |
| Input high voltage | $V_{IH}$ | — | 2.0 | NVDD + 0.3 | V |

**Table 28. GPIO DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le NVDD$ | — | ± 5 | μA |

### 8.4.2 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

**Table 29. IEEE 1588 Timer AC Specifications**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Timer clock cycle time | $t_{TMRCK}$ | 0 | 70 | MHz | 1 |
| Input setup to timer clock | $t_{TMRCKS}$ | — | — | — | 2, 3 |
| Input hold from timer clock | $t_{TMRCKH}$ | — | — | — | 2, 3 |
| Output clock to output valid | $t_{GCLKNV}$ | 0 | 6 | ns | — |
| Timer alarm to output valid | $t_{TMRAL}$ | — | — | — | 2 |

**Note:**
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

# 9 USB

## 9.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

### 9.1.1 USB DC Electrical Characteristics

This table lists the DC electrical characteristics for the USB interface.

**Table 30. USB DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | LVDD + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | LVDD – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $NV_{IN}$ symbol referenced in Table 1 and Table 2.

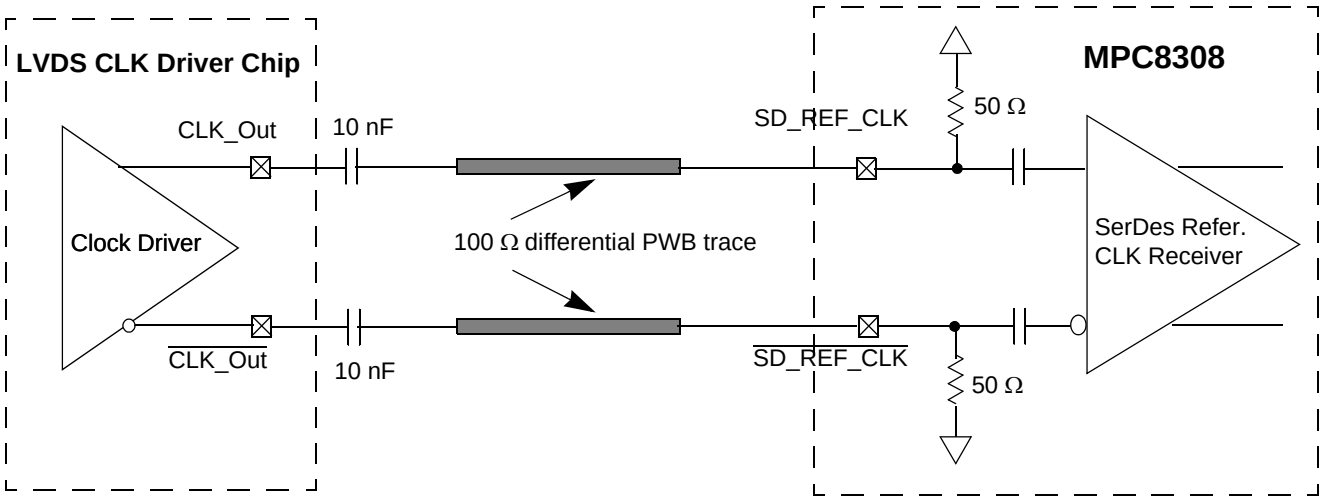


**Figure 21. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)**

Figure 22 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8308 SerDes reference clock input's DC requirement, AC-coupling has to be used.

This figure assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8308's SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

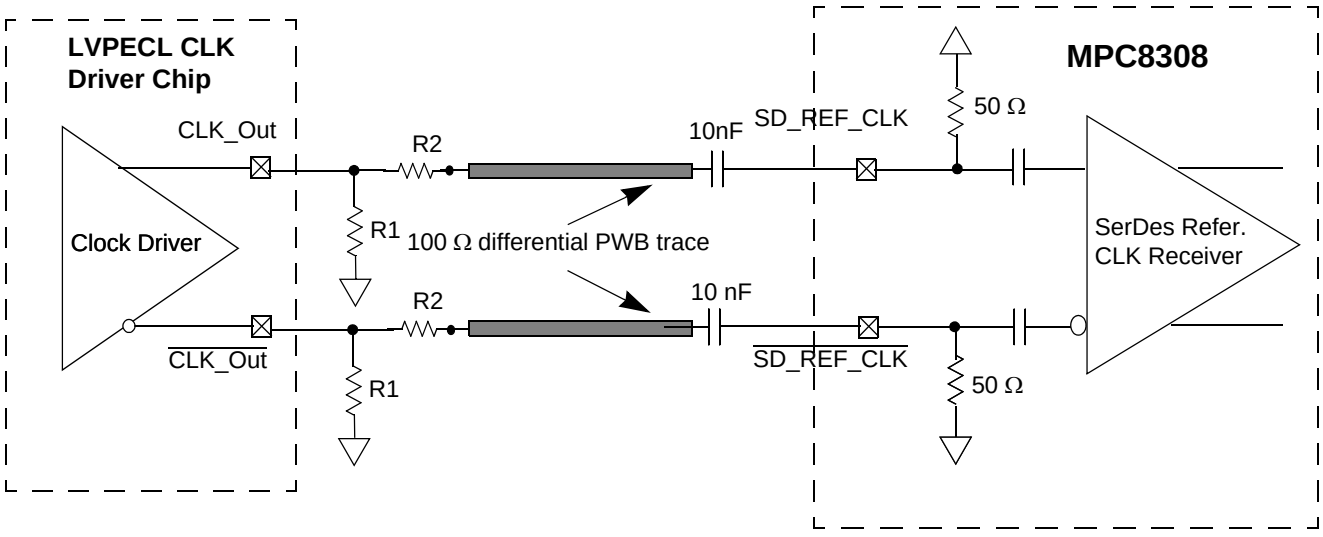


**Figure 22. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the device's SerDes reference clock input's DC requirement.

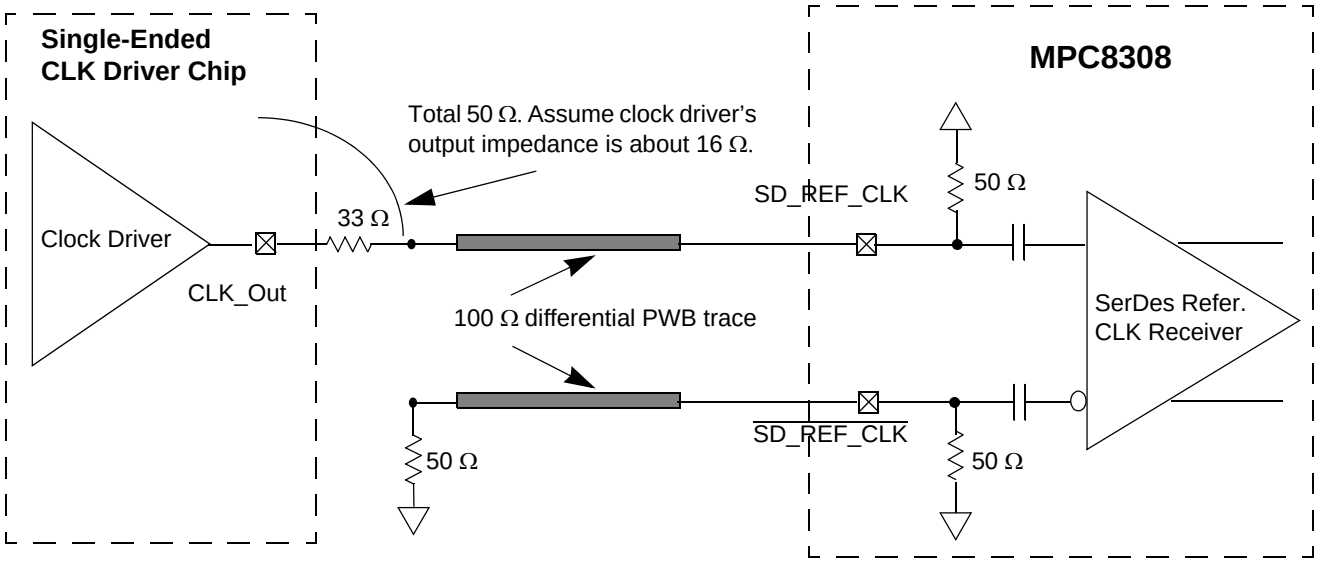


**Figure 23. Single-Ended Connection (Reference Only)**

## 10.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for PCI Express protocol.

**Table 32. SerDes Reference Clock AC Parameters**

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Rising Edge Rate | Rise Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling Edge Rate | Fall Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential Input High Voltage | $V_{IH}$ | +200 | — | mV | 2 |
| Differential Input Low Voltage | $V_{IL}$ | — | –200 | mV | 2 |

### 10.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

## 10.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

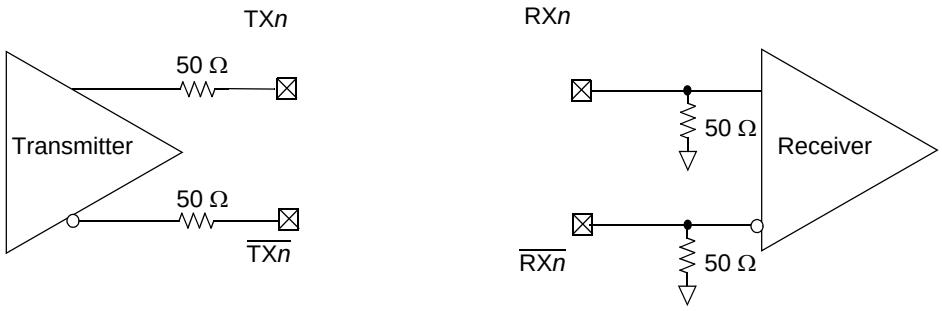


**Figure 26. SerDes Transmitter and Receiver Reference Circuits**

The DC and AC specification of SerDes data lanes are defined in Section 11, "PCI Express."

Note that external AC coupling capacitor is required for the PCI Express serial transmission protocol with the capacitor value defined in specification of PCI Express protocol section.

# 11 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

## 11.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 10.2, "SerDes Reference Clocks."

## 11.2 AC Requirements for PCI Express SerDes Clocks

This table lists the PCI Express SerDes clock AC requirements.

**Table 33. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time (for 125 MHz and 100 MHz) | 8 | 10 | — | ns | — |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles. | — | — | 100 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location. | –50 | — | 50 | ps | — |

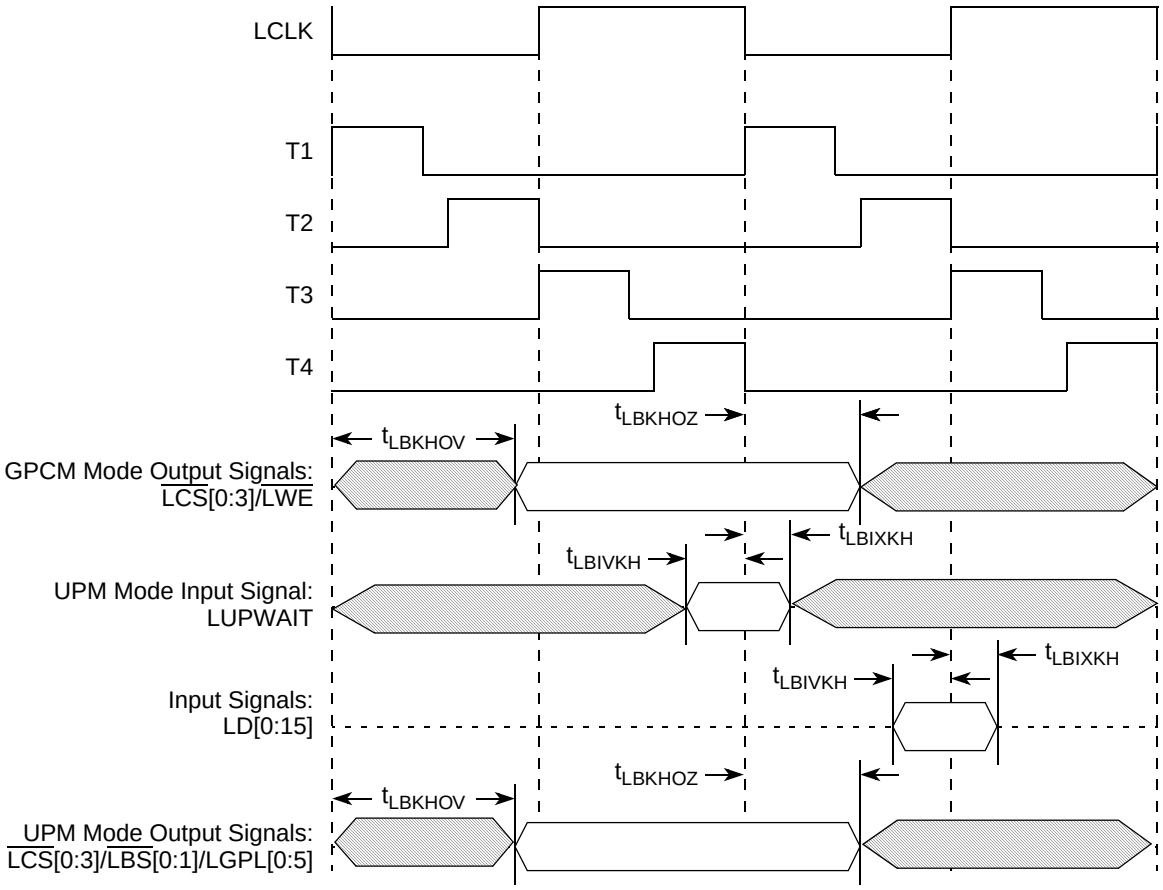


**Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4**

# 13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SD/MMC/SDIO) interface of the MPC8308.

The eSDHC controller always uses the falling edge of the SD_CLK in order to drive the SD_DAT[0:3]/CMD as outputs and rising edge to sample the SD_DAT[0:3], CMD, $\overline{\text{CD}}$ and WP as inputs. This behavior is true for both full and high speed modes.

## 13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device, compatible with SDHC specifications. The eSDHC $NV_{DD}$ range is between 3.0 V and 3.6 V.

**Table 38. eSDHC interface DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |

**Table 38. eSDHC interface DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |
| Input high voltage | $V_{IH}$ | — | 2.1 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |

## 13.2 eSDHC AC Timing Specifications (Full Speed Mode)

This section describes the AC electrical specifications for the eSDHC (SD/MMC) interface of the device. This table provides the eSDHC AC timing specifications for full speed mode as defined in Figure 35 and Figure 36.

**Table 39. eSDHC AC Timing Specifications for Full Speed Mode**

At recommended operating conditions $NV_{DD}$ = 3.3 V ± 300 mV.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| SD_CLK clock frequency—full speed mode | $f_{SFSCK}$ | 0 | 25 | MHz | — |
| SD_CLK clock cycle | $t_{SFSCK}$ | 40 | — | ns | — |
| SD_CLK clock frequency—identification mode | $f_{SIDCK}$ | 0 | 400 | kHz | — |
| SD_CLK clock low time | $t_{SFSCKL}$ | 15 | — | ns | 2 |
| SD_CLK clock high time | $t_{SFSCKH}$ | 15 | — | ns | 2 |
| SD_CLK clock rise and fall times | $t_{SFSCKR}$/ $t_{SFSCKF}$ | — | 5 | ns | 2 |
| Input setup times: SD_CMD, SD_DATx to SD_CLK | $t_{SFSIVKH}$ | 3 | — | ns | 2 |
| Input hold times: SD_CMD, SD_DATx to SD_CLK | $t_{SFSIXKH}$ | 2 | — | ns | 2 |
| Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid | $t_{SFSKHOV}$ | — | 3 | ns | 2 |
| Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid | $t_{SFSKHOX}$ | –3 | — | — | — |
| SD card input setup | $t_{ISU}$ | 5 | — | ns | 3 |
| SD card input hold | $t_{IH}$ | 5 | — | ns | 3 |
| SD card output valid | $t_{ODLY}$ | — | 14 | ns | 3 |
| SD card output hold | $t_{OH}$ | 0 | — | ns | 3 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

### 13.3.1 High Speed Output Path (Write)

This figure provides the data and command output timing diagram.

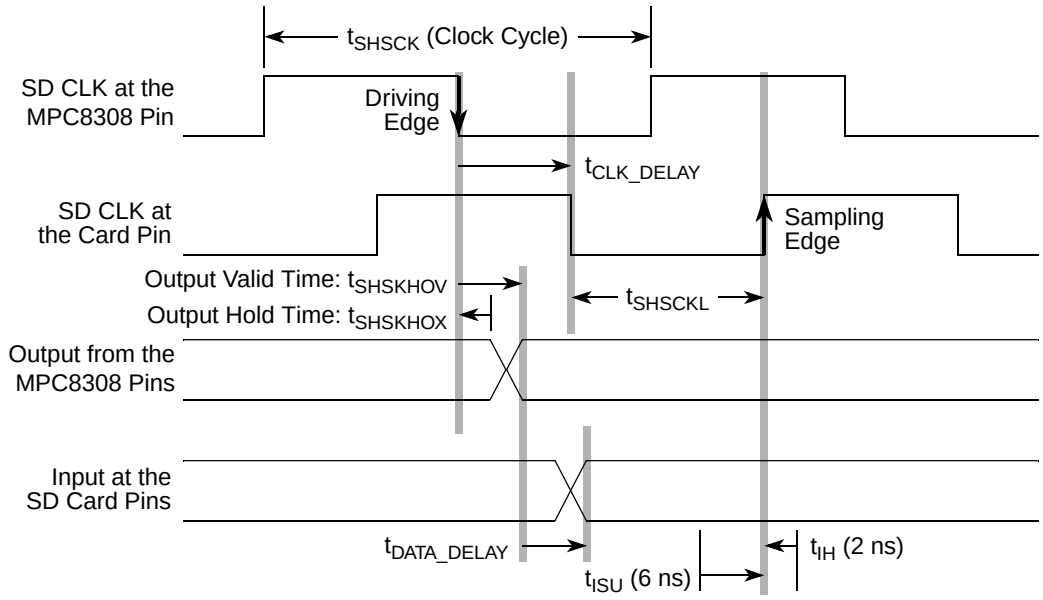


**Figure 38. High Speed Output Path**

### 13.3.2 High Speed Input Path (Read)

This figure provides the data and command input timing diagram.

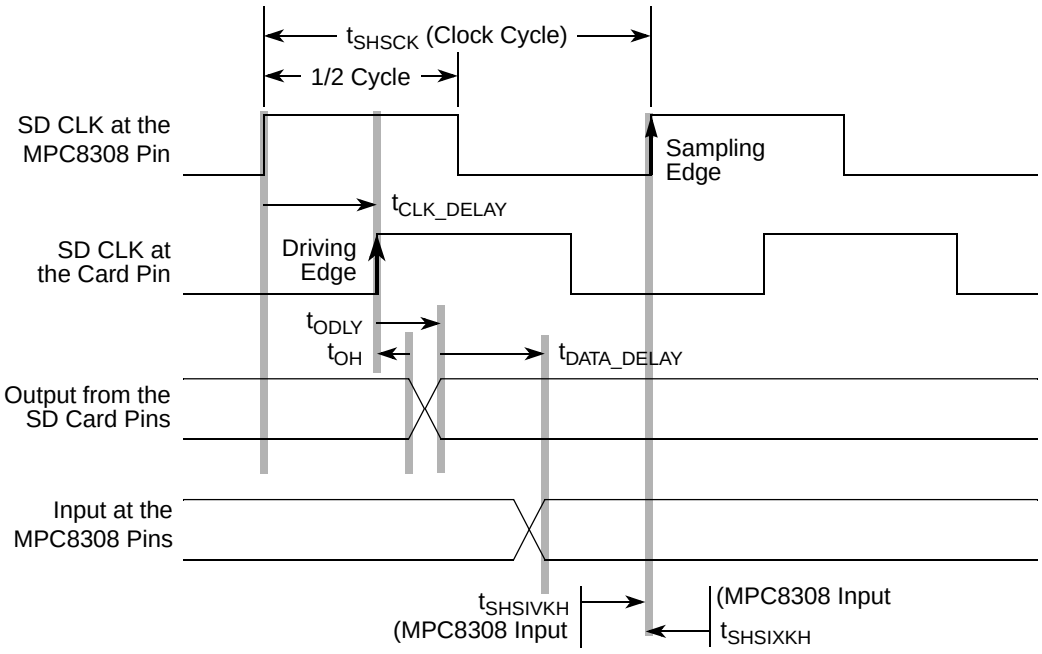


**Figure 39. High Speed Input Path**

2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

## 20.3 Pinout Listings

This table provides the pin-out listing for the MPC8308, MAPBGA package.

**Table 53. MPC8308 Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **DDR Memory Controller Interface** | | | | |
| MEMC_MDQ[0] | V6 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[1] | Y4 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[2] | AB3 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[3] | AA3 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[4] | AA2 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[5] | AA1 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[6] | W4 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[7] | Y2 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[8] | W3 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[9] | W1 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[10] | Y1 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[11] | W2 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[12] | U4 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[13] | U3 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[14] | V4 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[15] | U6 | I/O | $GV_{DDA}$ | — |
| MEMC_MDQ[16] | T3 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[17] | T2 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[18] | R4 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[19] | R3 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[20] | P4 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[21] | N6 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[22] | P2 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[23] | P1 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[24] | N4 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[25] | N3 | I/O | $GV_{DDB}$ | — |
| MEMC_MDQ[26] | N2 | I/O | $GV_{DDB}$ | — |

This table provides the operating frequencies for the device under recommended operating conditions (Table 2).

**Table 55. Operating Frequencies for MPC8308**

| Characteristic[1] | Maximum Operating Frequency | Unit |
|---|---|---|
| e300 core frequency (*core_clk*) | 400 | MHz |
| Coherent system bus frequency (*csb_clk*) | 133 | MHz |
| DDR2 memory bus frequency (MCK)[2] | 133 | MHz |
| Local bus frequency (LCLK*0*)[3] | 66 | MHz |

**Notes:**
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK0, and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCCR[CLKDIV]) which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

## 21.2 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

**Table 56. System PLL Ratio**

| RCWL[SPMF] | csb_clk: SYS_CLK_IN |
|---|---|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | 2 : 1 |
| 0011 | 3 : 1 |
| 0100 | 4 : 1 |
| 0101 | 5 : 1 |
| 0110–1111 | Reserved |

As described in Section 21, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (SYS_CLK_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN ratios.

**Table 57. CSB Frequency Options**

| SPMF<br>*csb_clk* :Input Clock Ratio | | Input Clock Frequency (MHz) | | |
|---|---|---|---|---|
| | | 25 | 33.33 | 66.67 |
| 0010 | 2:1 | | | 133 |
| 0100 | 4:1 | | 133 | |
| 0101 | 5:1 | 125 | 167 | |

## 21.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

**NOTE**

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

**Table 58. e300 Core PLL Configuration**

| RCWL[COREPLL] | | | *core_clk: csb_clk* Ratio[1] | VCO Divider (VCOD)[2] |
|---|---|---|---|---|
| **0–1** | **2–5** | **6** | | |
| ***nn*** | **0000** | 0 | PLL bypassed (PLL off, *csb_clk* clocks core directly) | PLL bypassed (PLL off, *csb_clk* clocks core directly) |
| **11** | ***nnnn*** | n | n/a | n/a |
| **00** | **0001** | 0 | 1:1 | 2 |
| **01** | **0001** | 0 | 1:1 | 4 |
| **10** | **0001** | 0 | 1:1 | 8 |
| **00** | **0001** | 1 | 1.5:1 | 2 |
| **01** | **0001** | 1 | 1.5:1 | 4 |
| **10** | **0001** | 1 | 1.5:1 | 8 |
| **00** | **0010** | 0 | 2:1 | 2 |
| **01** | **0010** | 0 | 2:1 | 4 |
| **10** | **0010** | 0 | 2:1 | 8 |
| **00** | **0010** | 1 | 2.5:1 | 2 |
| **01** | **0010** | 1 | 2.5:1 | 4 |
| **10** | **0010** | 1 | 2.5:1 | 8 |
| **00** | **0011** | 0 | 3:1 | 2 |
| **01** | **0011** | 0 | 3:1 | 4 |
| **10** | **0011** | 0 | 3:1 | 8 |

**Note:**

1 For any *core_clk:csb_clk* ratios, the *core_clk* must not exceed its maximum operating frequency of 400 MHz.

2 Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

# 22 Thermal

This section describes the thermal specifications of the device.