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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8308zqadd

The I/O power supply ramp-up slew rate should be slower than 4V/100 μs, this requirement is for ESD circuit. Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD}, LV_{DD}, and NV_{DD}) do not have any ordering requirements with respect to one another.

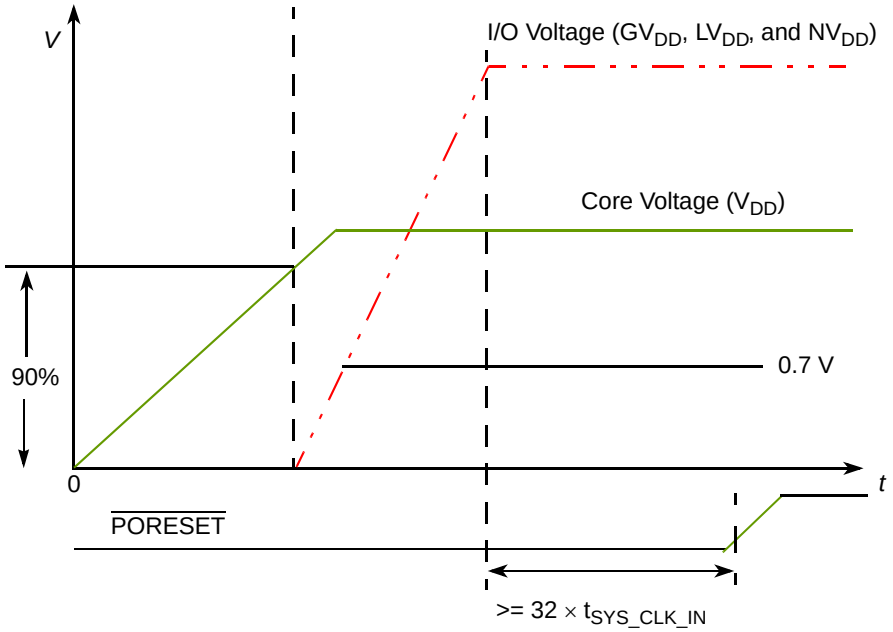

Figure 3. Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power for the device is shown in this table. Table 5 shows the estimated typical I/O power dissipation.

Table 4. MPC8308 Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	Typical[2]	Maximum [3]	Unit
266	133	530	900	mW
333	133	565	950	mW
400	133	600	1000	mW

Note:

1 The values do not include I/O supply power but do include core (V_{DD}) and PLL (AV_{DD1}, AV_{DD2}, $XCOREV_{DD}$, $XPADV_{DD}$, and $SDAV_{DD}$)

2 Typical power is based on best process, a voltage of V_{DD} = 1.0 V and ambient temperature of T_A = 25° C and an artificial smoker test.

3 Maximum power is estimated based on best process, a voltage of V_{DD} = 1.05 V, a junction temperature of T_J = 105° C

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/	Symbol	Min	Typ	Max	Unit	Notes
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1, 6
SYS_CLK_IN period	$t_{SYS\_CLK\_IN}$	15	—	41.67	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6		1.2	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system and core must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33 kHz (max rate).

Table 9. RTC_PIT_CLOCK AC Timing Specifications

Parameter/	Symbol	Min	Typ	Max	Unit	Notes
RTC_PIT_CLOCK frequency	$f_{RTC\_PIT\_CLOCK}$	1	32768	—	Hz	—
RTC_PIT_CLOCK rise and fall time	t_{RTCH}, t_{RTCL}	1.5	—	3	μs	—
RTC_PIT_CLOCK duty cycle	$t_{RTCHK}/t_{RTC\_PIT\_CLOCK}$	45	—	55	%	—

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the device.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

Table 10. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$		±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

This figure illustrates the DDR2 input timing diagram showing the t_{DISKEW} timing parameter.

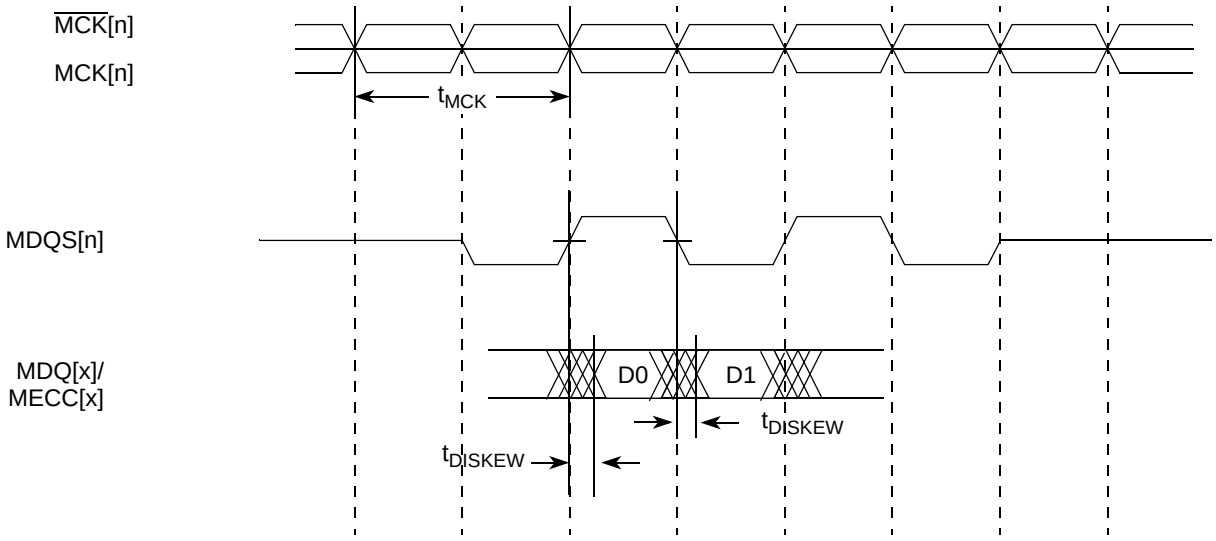

Figure 4. Timing Diagram for t_{DISKEW}

6.2.2 DDR2 SDRAM Output AC Timing Specifications

Table 18. DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}		—	ns	3
266 MHz		2.9			
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}		—	ns	3
266 MHz		2.33			
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}		—	ns	3
266 MHz		2.5			
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}		—	ns	3
266 MHz		3.15			
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ//MDM/MECC output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}		—	ps	5
266 MHz		900			
MDQ//MDM/MECC output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}		—	ps	5
266 MHz		1100			
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure shows the DDR2 SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

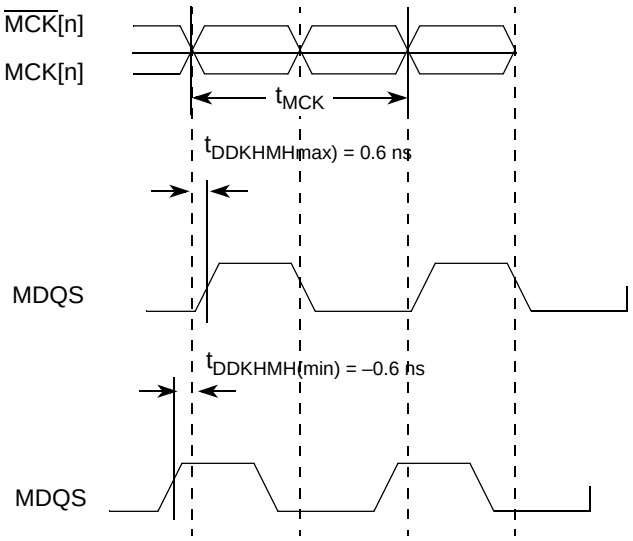

Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR2 SDRAM output timing diagram.

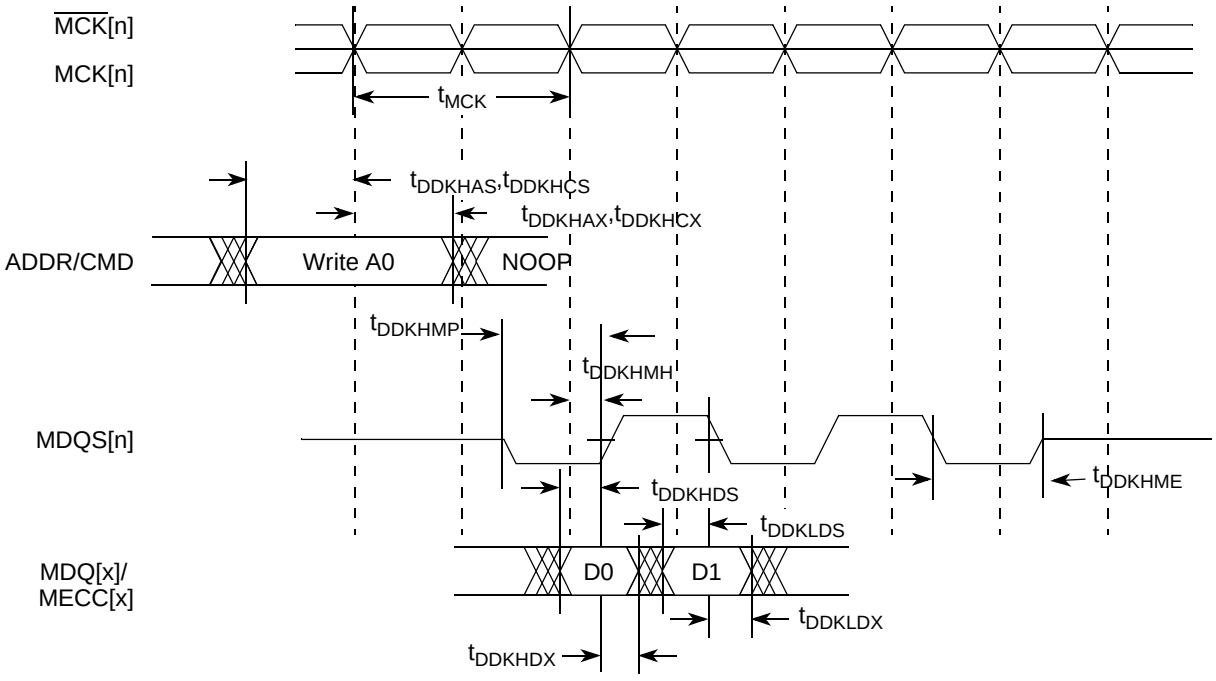

Figure 6. DDR2 SDRAM Output Timing Diagram

This figure shows the MII transmit AC timing diagram.

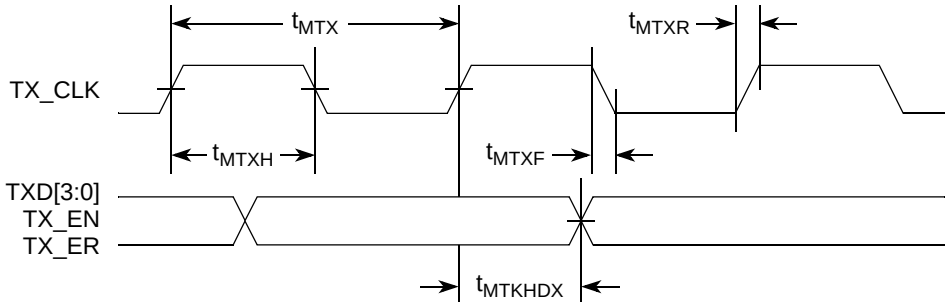

Figure 8. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

and RGMII are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. This table provides the DC electrical characteristics for MDIO and MDC.

Table 26. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NV_{DD}	—		3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DD} = Min	2.10	NV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	VSS	0.50	V
Input high voltage	V_{IH}	—		2.0	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	NV_{DD} = Max	V_{IN} [1] = 2.1 V	—	40	μA
Input low current	I_{IL}	NV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 27. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} is 3.3 V ± 0.3V

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

10 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

10.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 15 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX*n* and $\overline{\text{TX}n}$) or a receiver input (RX*n* and $\overline{\text{RX}n}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- **Single-Ended Swing**

  The transmitter output signals and the receiver input signals TX*n*, $\overline{\text{TX}n}$, RX*n*, and $\overline{\text{RX}n}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's single-ended swing.
- **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**)

  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.
- **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**)

  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.
- **Differential Peak Voltage, V_{DIFFp}**

  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, V_{DIFFp} = |A – B| Volts.
- **Differential Peak-to-Peak, $V_{DIFFp-p}$**

  Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.
- **Differential Waveform**

  The differential waveform is constructed by subtracting the inverting signal (for example, $\overline{\text{TX}n}$) from the non-inverting signal (for example, TX*n*) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 24 as an example for differential waveform.

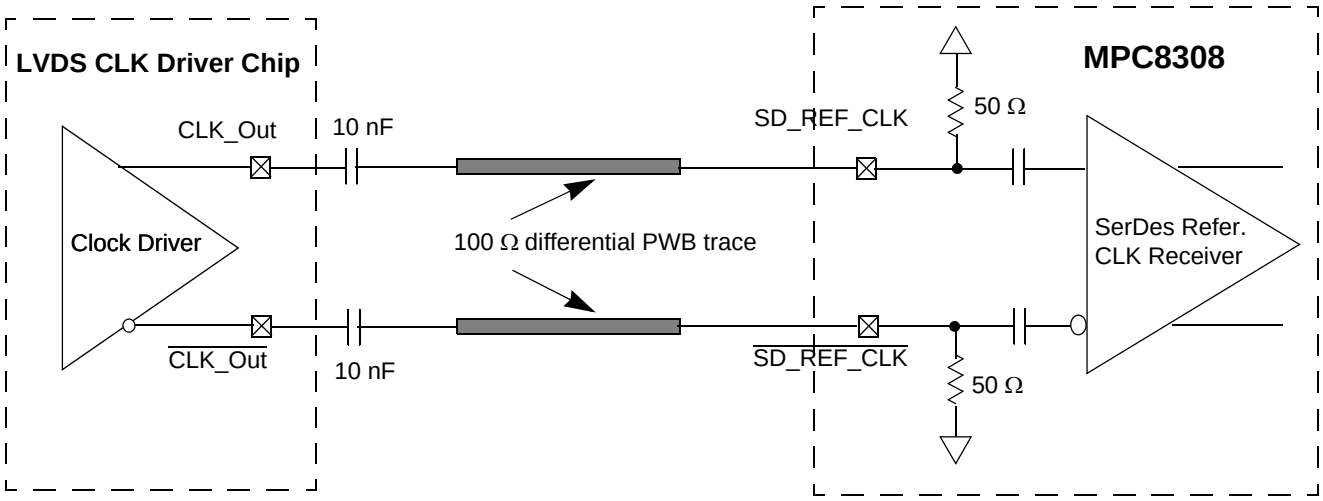

Figure 21. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 22 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8308 SerDes reference clock input's DC requirement, AC-coupling has to be used.

This figure assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8308's SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

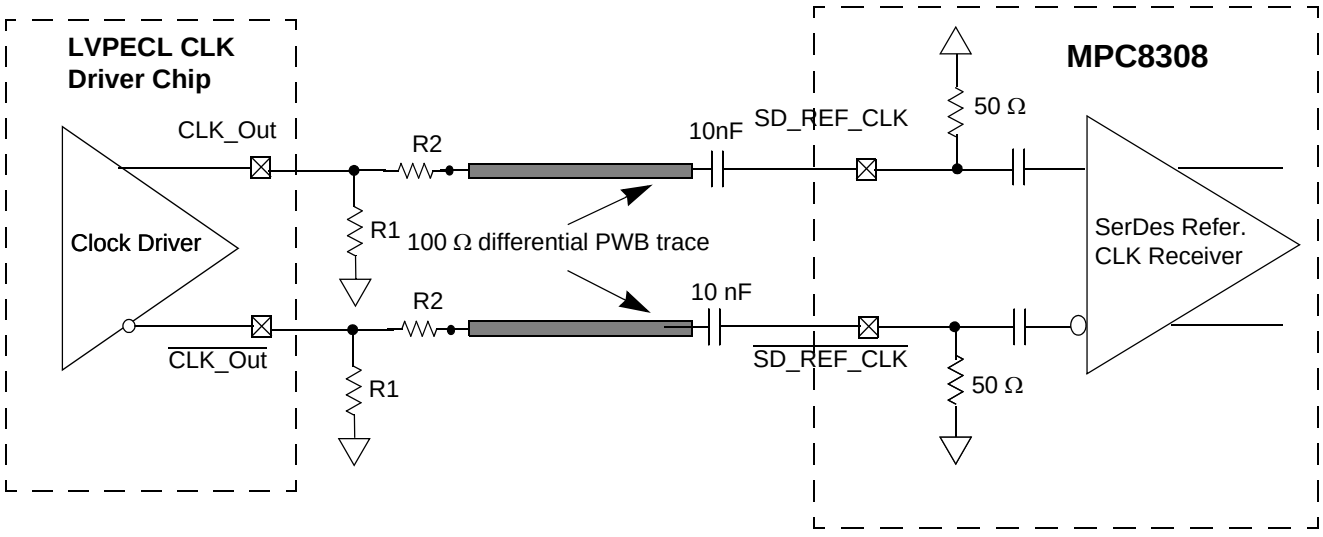

Figure 22. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

11.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

11.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer please use the *PCI Express Base Specification*, Rev. 1.0a.

11.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 34. Differential Transmitter (TX) Output Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Unit interval	UI	Each U_{PETX} is 400 ps ± 300 ppm. U_{PETX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	$V_{PEDPPTX} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.8	—	1.2	V	2
De-Emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	Ratio of the $V_{PEDPPTX}$ of the second and following bits after a transition divided by the $V_{PEDPPTX}$ of the first bit after a transition.	–3.0	–3.5	–4.0	dB	2
Minimum TX eye width	T_{TX-EYE}	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - U_{PEEWTX} = 0.3$ UI.	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPTX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.15	UI	2, 3
D+/D- TX output rise/fall time	$T_{TX-RISE}$, $T_{TX-FALL}$	—	0.125	—	—	UI	2, 5
RMS AC peak common mode output voltage	$V_{TX-CM-ACp}$	$V_{PEACPCMTX} = RMS(\|V_{TXD+} + V_{TXD-}\|/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$	—	—	20	mV	2

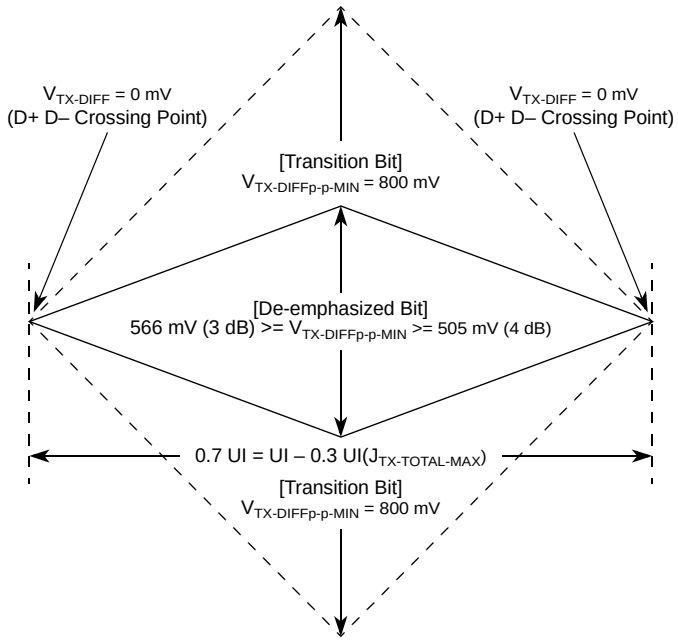

Figure 27. Minimum Transmitter Timing and Voltage Output Compliance Specifications

11.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 35. Differential Receiver (RX) Input Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Unit interval	UI	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{RX-DIFFp-p}$	$V_{PEDPPRX} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	—	1.200	V	2
Minimum receiver eye width	T_{RX-EYE}	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - U_{PEEWRX} = 0.6$ UI.	0.4	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPRX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.3	UI	2, 3, 7

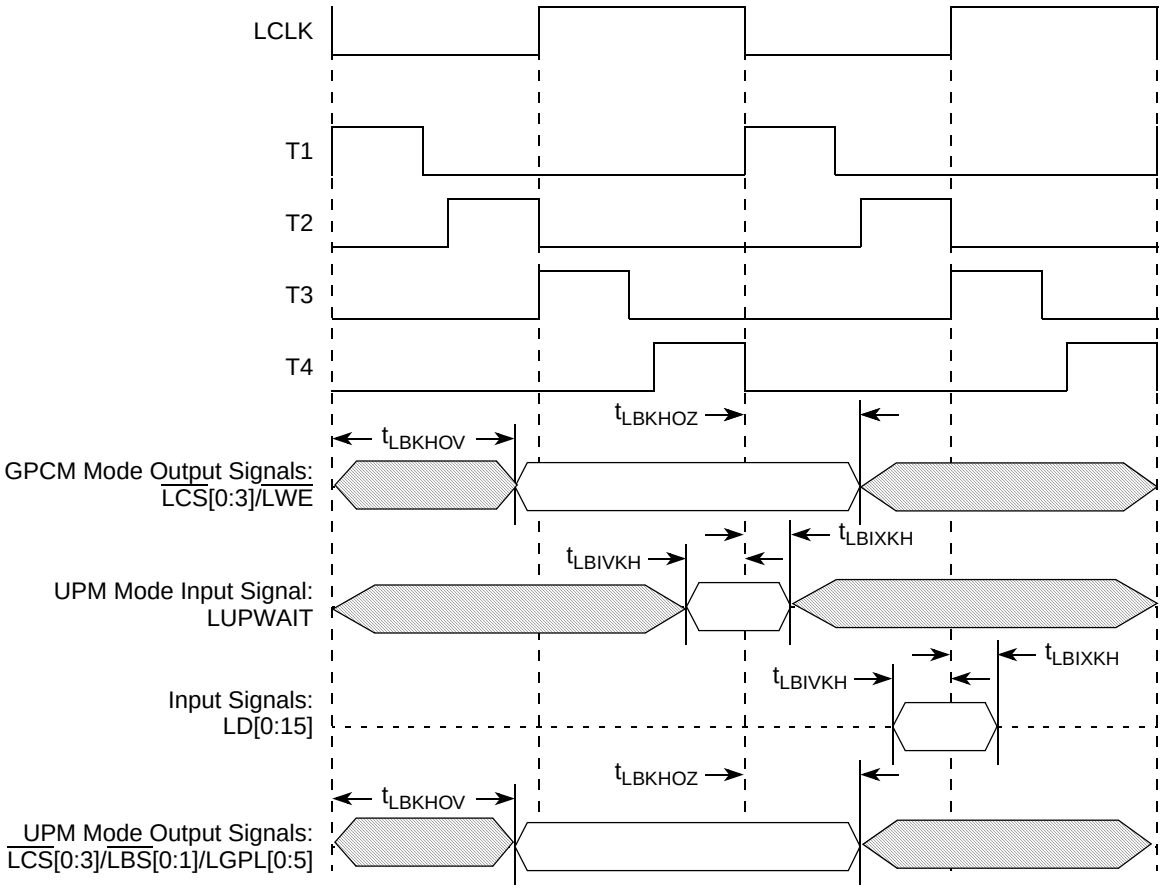

Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4

13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SD/MMC/SDIO) interface of the MPC8308.

The eSDHC controller always uses the falling edge of the SD_CLK in order to drive the SD_DAT[0:3]/CMD as outputs and rising edge to sample the SD_DAT[0:3], CMD, $\overline{\text{CD}}$ and WP as inputs. This behavior is true for both full and high speed modes.

13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device, compatible with SDHC specifications. The eSDHC NV_{DD} range is between 3.0 V and 3.6 V.

Table 38. eSDHC interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

This figure provides the eSDHC clock input timing diagram.

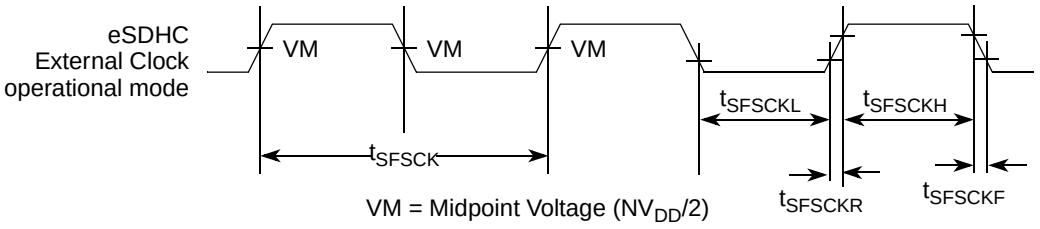

Figure 34. eSDHC Clock Input Timing Diagram

13.2.1 Full Speed Output Path (Write)

This figure provides the data and command output timing diagram.

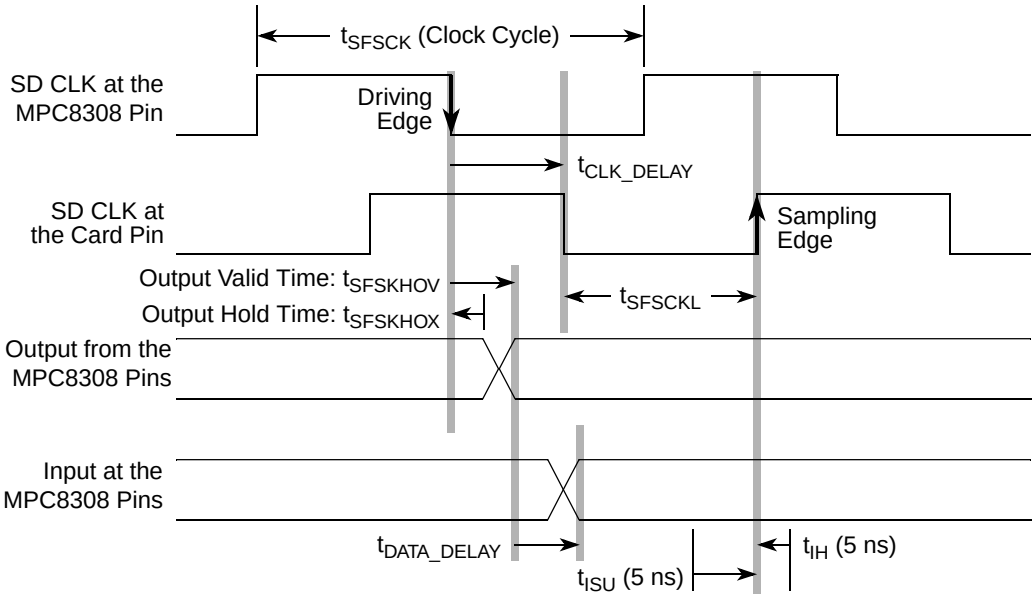

Figure 35. Full Speed Output Path

13.2.2 Full Speed Input Path (Read)

This figure provides the data and command input timing diagram.

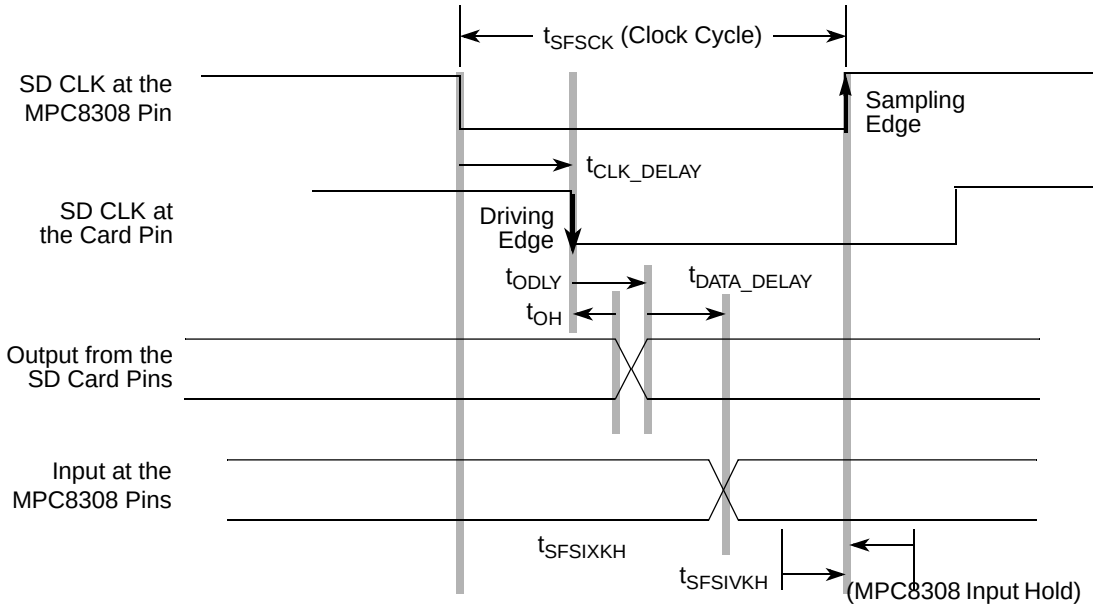

Figure 36. Full Speed Input Path

13.3 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications.

Table 40. eSDHC AC Timing Specifications for High Speed Mode

At recommended operating conditions NV_{DD} = 3.3 V ± 300 mV.

Parameter	Symbol [1]	Min	Max	Unit	Notes
SD_CLK clock frequency—high speed mode	f_{SHSCK}	0	50	MHz	3
SD_CLK clock cycle	t_{SHSCK}	20	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	kHz	—
SD_CLK clock low time	t_{SHSCKL}	7	—	ns	2
SD_CLK clock high time	t_{SHSCKH}	7	—	ns	2
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	2
Input setup times: SD_CMD, SD_DATx	$t_{SHSIVKH}$	3	—	ns	2
Input hold times: SD_CMD, SD_DATx	$t_{SHSIXKH}$	2	—	ns	2
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	3	—	ns	2
Output Hold time: SD_CLK to SD_CMD, SD_DATx invalid	$t_{SHSKHOX}$	–3	—	ns	2
SD Card Input Setup	t_{ISU}	6	—	ns	3
SD Card Input Hold	t_{IH}	2	—	ns	3

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{LCS}}$[3]	Y11	O	NV_{DDP_K}	4
$\overline{\text{LWE}}$[0] /$\overline{\text{LFWE}}$0/$\overline{\text{LBS}}$0	AB11	O	NV_{DDP_K}	—
$\overline{\text{LWE}}$[1]/$\overline{\text{LBS}}$1	AC11	O	NV_{DDP_K}	—
LBCTL	U11	O	NV_{DDP_K}	—
LGPL0/LFCLE	Y10	O	NV_{DDP_K}	—
LGPL1/LFALE	AA10	O	NV_{DDP_K}	—
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AB10	O	NV_{DDP_K}	4
LGPL3/$\overline{\text{LFWP}}$	AC10	O	NV_{DDP_K}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LFRB	AB9	I/O	NV_{DDP_K}	4
LGPL5	Y9	O	NV_{DDP_K}	—
LCLK0	AC12	O	NV_{DDP_K}	—
DUART				
UART_SOUT1/MSRCID0/ LSRCID0	C17	O	NV_{DDB}	—
UART_SIN1/MSRCID1/ LSRCID1	B18	I/O	NV_{DDB}	—
UART_SOUT2/MSRCID2/ LSRCID2	D17	O	NV_{DDB}	—
UART_SIN2/MSRCID3/ LSRCID3	D18	I/O	NV_{DDB}	—
PEX PHY				
TXA	C14	O	XPADVDD	—
$\overline{\text{TXA}}$	C15	O	XPADVDD	—
RXA	A13	I	XCOREVDD	—
$\overline{\text{RXA}}$	B13	I	XCOREVDD	—
SD_IMP_CAL_RX	A15	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	C12	I	XCOREVDD	—
SD_REF_CLK	D12	I	XCOREVDD	—
SD_PLL_TPD	F13	O	—	—
SD_IMP_CAL_TX	A11	I	XPADVDD	—
SD_PLL_TPA_ANA	F11	O	—	—
SDAVDD_0	G12	I	—	—
SDAVSS_0	F12	I	—	—
I^2C interface				
IIC_SDA1	C9	I/O	NV_{DDA}	2

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
USBDR_PCTL1	U20	O	NV_{DDH}	—
USBDR_STP	V21	O	NV_{DDH}	—
TSEC_TMR_CLK/ GPIO[8]	W23	I	NV_{DDH}	—
GTM1_TOUT3/ GPIO[9]	T18	O	NV_{DDH}	—
GTM1_TOUT4/ GPIO[10]	V20	O	NV_{DDH}	—
TSEC_TMR_TRIG1/ GPIO[11]	W21	I	NV_{DDH}	—
TSEC_TMR_TRIG2/ GPIO[12]	Y21	I	NV_{DDH}	—
TSEC_TMR_GCLK	L17	O	NV_{DDG}	—
TSEC_TMR_PP1	L18	O	NV_{DDG}	—
TSEC_TMR_PP2	L21	O	NV_{DDG}	—
TSEC_TMR_PP3/ GPIO[13]	L22	O	NV_{DDG}	—
TSEC_TMR_ALARM1	L23	O	NV_{DDG}	—
TSEC_TMR_ALARM2/ GPIO[14]	M23	O	NV_{DDG}	—
GPIO[7]	M22	IO	—	—
TSEC2_CRS/ GPIO[0]	M21	IO	NV_{DDG}	—
TSEC2_TMR_RX_ESFD/ GPIO[1]	M18	O	NV_{DDG}	—
TSEC2_TMR_TX_ESFD/ GPIO[2]	M20	O	NV_{DDG}	—
TSEC1_TMR_RX_ESFD/ GPIO[3]	N23	O	NV_{DDG}	—
TSEC1_TMR_TX_ESFD/ GPIO[4]	N21	O	NV_{DDG}	—
GTM1_TGATE3	N20	I	NV_{DDG}	—
GTM1_TIN4	N18	I	NV_{DDG}	—
GTM1_TGATE4/ GPIO[15]	P23	I	NV_{DDG}	—
GTM1_TIN3	P22	I	NV_{DDG}	—
GPIO[5]	N17	IO	NV_{DDH}	—
GPIO[6]	P21	IO	NV_{DDH}	—
Power and Ground Supplies				
AV_{DD1}	R6	I	—	—
AV_{DD2}	V10	I	—	—
NC, No Connection	B11, B16, D16	—	—	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	Y23, H8, H9, H10, H14, H15, H16, J8, J16, K8, K16, L8, L16, M8, M16, N8, N16, P8, P16, R8, R16, T8, T9, T10, T11, T12, T13, T14, T15, T16	I	—	—
VSS	A2, A21, B1, B19, B23, C4, C16, D6, D19, E3, F8, F15, F17, F23, G7, G8, G10, G15, G16, G17, G20, H2, H6, H7, H17, H23, J7, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, K15, L1, L7, L9, L10, L11, L12, L13, L14, L15, L20, M4, M9, M10, M11, M12, M13, M14, M15, N9, N10, N11, N12, N13, N14, N15, P6, P7, P9, P10, P11, P12, P13, P14, P15, R2, R7, R9, R10, R11, R12, R13, R14, R15, R22, T6, T7, U8, U17, U21, V2, V7, V9, V11, W20, Y8, Y15, AA4, AB1, AB6, AB12, AB19, AC2, AC9, AC23	I	—	—
NV_{DDA}	B7, B10, C7, D9, F9	I	—	—
NV_{DDB}	A16, A19, C18	I	—	—
NV_{DDC}	A23, B22, D23, E20, G18	I	—	—
NV_{DDF}	G22, J22, K17	I	—	—
NV_{DDG}	M17, N22	I	—	—
NV_{DDH}	P17, R20, T17, T23, W22, Y22	I	—	—
NV_{DDJ}	AB23, AA22	I	—	—
NV_{DDP_K}	U10, U14, Y5, Y18, AA11, AB8, AB16, AB22, AC4, AC13	I	—	—
GV_{DD}	A1, A6, B3, D1, F1, F6, G4, J1, J4, K7, N1, N7, T1, T4, U7, Y3, AC1	I	—	—
XPADVDD	D15, F10, F14	I	—	—
XPADVSS	A10, B15, D14, G13, G14, H12	I	—	—
XCOREVDD	A14, B12, C13	I	—	—
XCOREVSS	A12, B14, C11, D11, D13, G11, H11, H13	I	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. This pin has weak internal pull-up that is always enabled. 5. This pin must always be tied to VSS.
6. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
7. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a buffer released to high impedance is needed.
8. This pin has weak internal pull-down that is always enabled

21.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 58. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk: csb_clk* Ratio[1]	VCO Divider (VCOD)[2]
0–1	**2–5**	**6**		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	***nnnn***	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8

Note:

1 For any *core_clk:csb_clk* ratios, the *core_clk* must not exceed its maximum operating frequency of 400 MHz.

2 Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

22 Thermal

This section describes the thermal specifications of the device.

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the device

23.1 System Clocking

The device includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 21.2, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.3, “Core PLL Configuration.”

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} for core PLL and AV_{DD2} for the platform PLL). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low pass filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 54, one to each of the two AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs’ resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

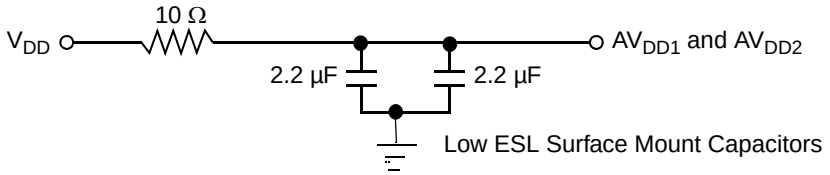

Figure 54. PLL Power Supply Filter Circuit

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