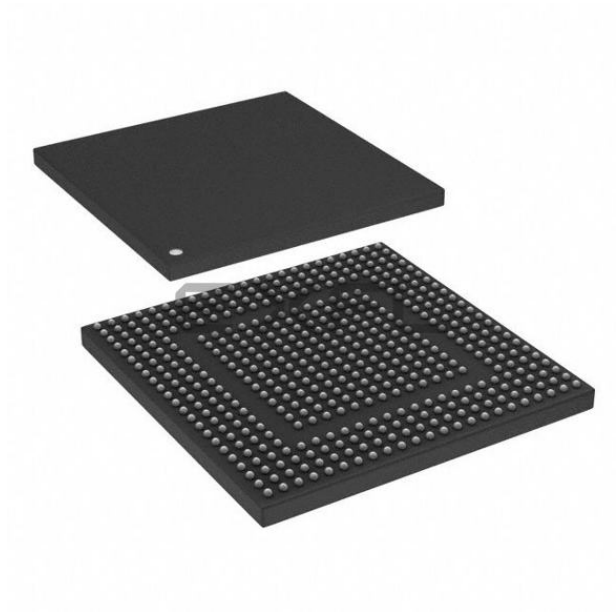

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Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8308zqafda

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit
SerDes internal digital power	$XCOREV_{DD}$	1.0 V ± 50 mV	V
SerDes internal digital power	$XCOREV_{SS}$	0.0	V
SerDes I/O digital power	$XPADV_{DD}$	1.0 V ± 50 mV	V
SerDes analog power for PLL	$SDAV_{DD}$	1.0 V ± 50 mV	V
SerDes analog power for PLL	$SDAV_{SS}$	0	V
SerDes I/O digital power	$XPADV_{SS}$	0	V
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V
Analog supply for e300 core APLL[2]	AV_{DD1}	1.0 V ± 50 mV	V
Analog supply for system APLL[2]	AV_{DD2}	1.0 V ± 50 mV	V
DDR2 DRAM I/O voltage	GV_{DD}	1.8 V ± 100 mV	V
Differential reference voltage for DDR controller	MV_{REF}	GVDD/2 ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$)	V
Standard I/O voltage (Local bus, DUART, system control and power management, eSDHC, USB, I^2C, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage)[3]	NV_{DD}	3.3 V ± 300 mV	V
eTSEC IO supply[4,5]	LV_{DD1}, LV_{DD2}	2.5 V ± 125 mV 3.3 V ± 300 mV	V
Analog and digital ground	V_{SS}	0.0	V
Operating temperature range[6]	T_A/T_J	Standard = 0 to 105 Extended = -40 to 105	°C

Notes:

1. GV_{DD}, NV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. This voltage is the input to the filter discussed in Section 23.2, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. NV_{DD} here refers to NV_{DDA}, NV_{DDB},NV_{DDG}, NV_{DDH}, NV_{DDJ} and NV_{DDP_K} from the ball map.
4. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
5. LV_{DD1} here refers to NV_{DDC} and LV_{DD2} refers to NV_{DDF} from the ball map.
6. Minimum temperature is specified with T_A; Maximum temperature is specified with T_J.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/	Symbol	Min	Typ	Max	Unit	Notes
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1, 6
SYS_CLK_IN period	$t_{SYS\_CLK\_IN}$	15	—	41.67	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6		1.2	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system and core must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33 kHz (max rate).

Table 9. RTC_PIT_CLOCK AC Timing Specifications

Parameter/	Symbol	Min	Typ	Max	Unit	Notes
RTC_PIT_CLOCK frequency	$f_{RTC\_PIT\_CLOCK}$	1	32768	—	Hz	—
RTC_PIT_CLOCK rise and fall time	t_{RTCH}, t_{RTCL}	1.5	—	3	μs	—
RTC_PIT_CLOCK duty cycle	$t_{RTCHK}/t_{RTC\_PIT\_CLOCK}$	45	—	55	%	—

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the device.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

Table 10. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$		±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ//MDM/MECC output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}		—	ps	5
266 MHz		900			
MDQ//MDM/MECC output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}		—	ps	5
266 MHz		1100			
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure shows the DDR2 SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

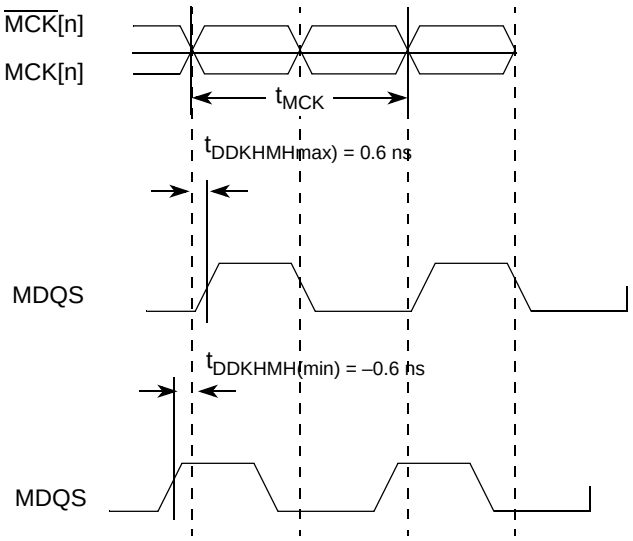


Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR2 SDRAM output timing diagram.

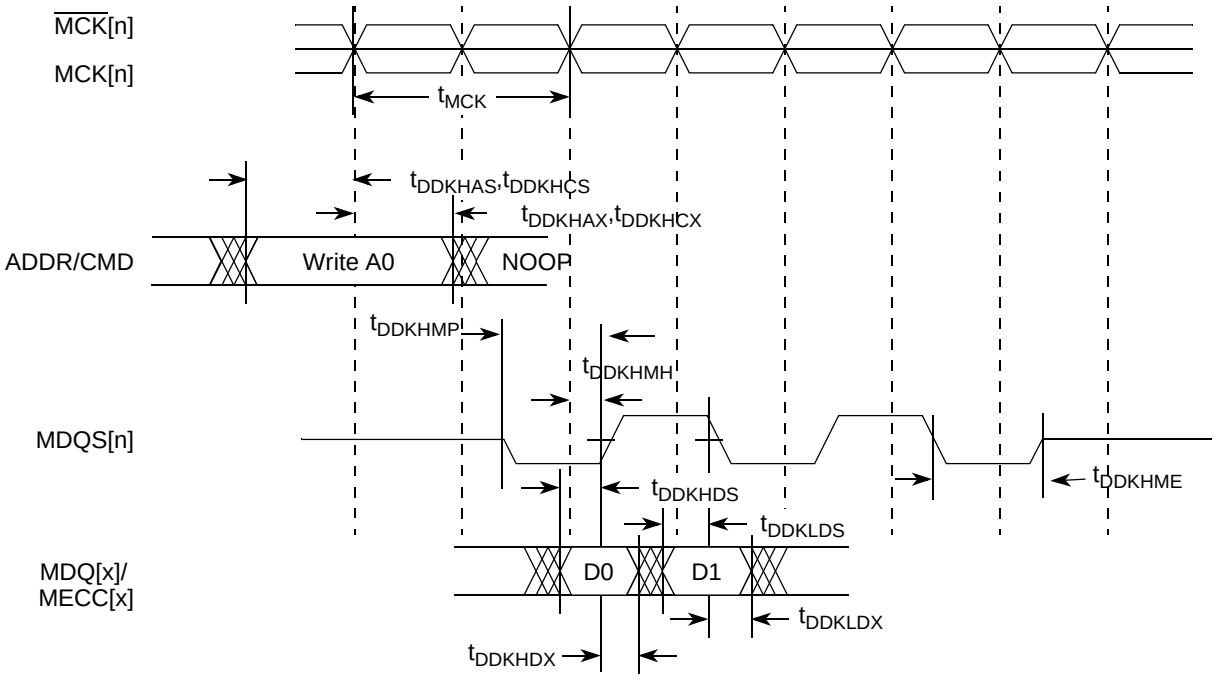


Figure 6. DDR2 SDRAM Output Timing Diagram

Table 22. RGMII DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD}= Min	VSS – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DD}		—	15	μA
Input low current	I_{IL}	V_{IN} [1] = VSS		–15	—	μA

Note:
1. V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 MII and RGMII AC Timing Specifications

The AC timing specifications for MII and RGMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

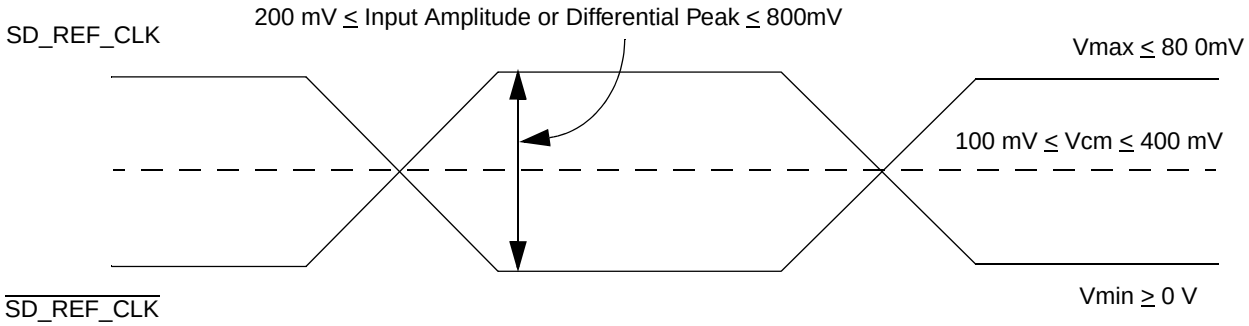


Figure 17. Differential Reference Clock Input DC Requirements (External DC-Coupled)

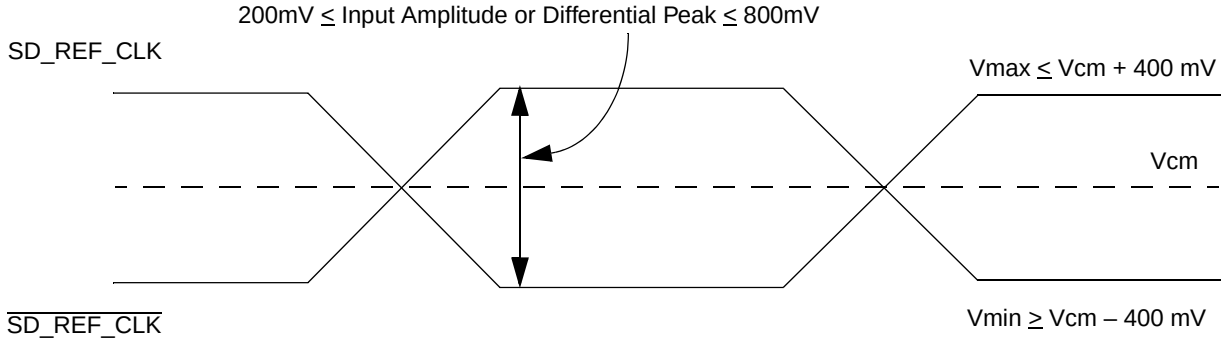


Figure 18. Differential Reference Clock Input DC Requirements (External AC-Coupled)

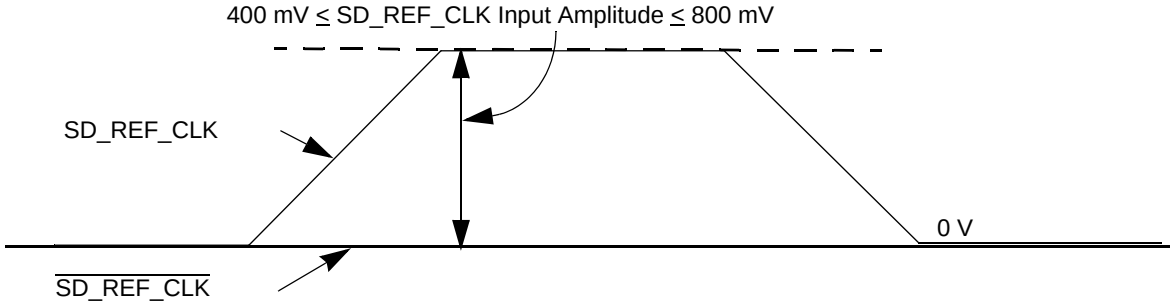


Figure 19. Single-Ended Reference Clock Input DC Requirements

10.2.3 Interfacing with Other Differential Signaling Levels

With on-chip termination to XCOREVSS, the differential reference clocks inputs are high-speed current steering logic (HCSL) compatible and DC coupled.

Many other low voltage differential type outputs like low-voltage differential signaling (LVDS) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100–400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

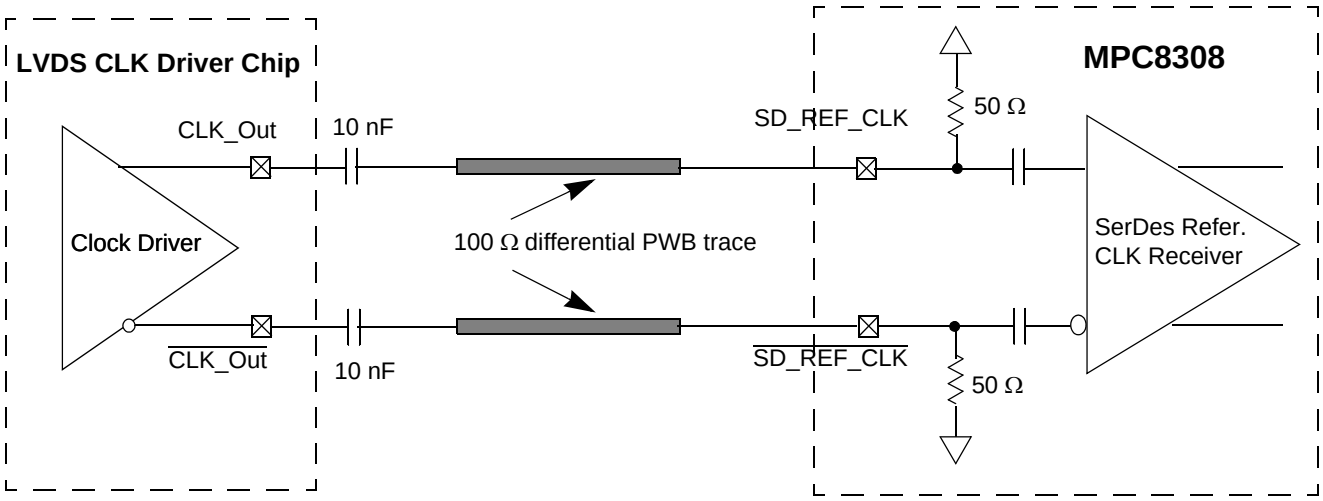


Figure 21. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 22 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8308 SerDes reference clock input's DC requirement, AC-coupling has to be used.

This figure assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8308's SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

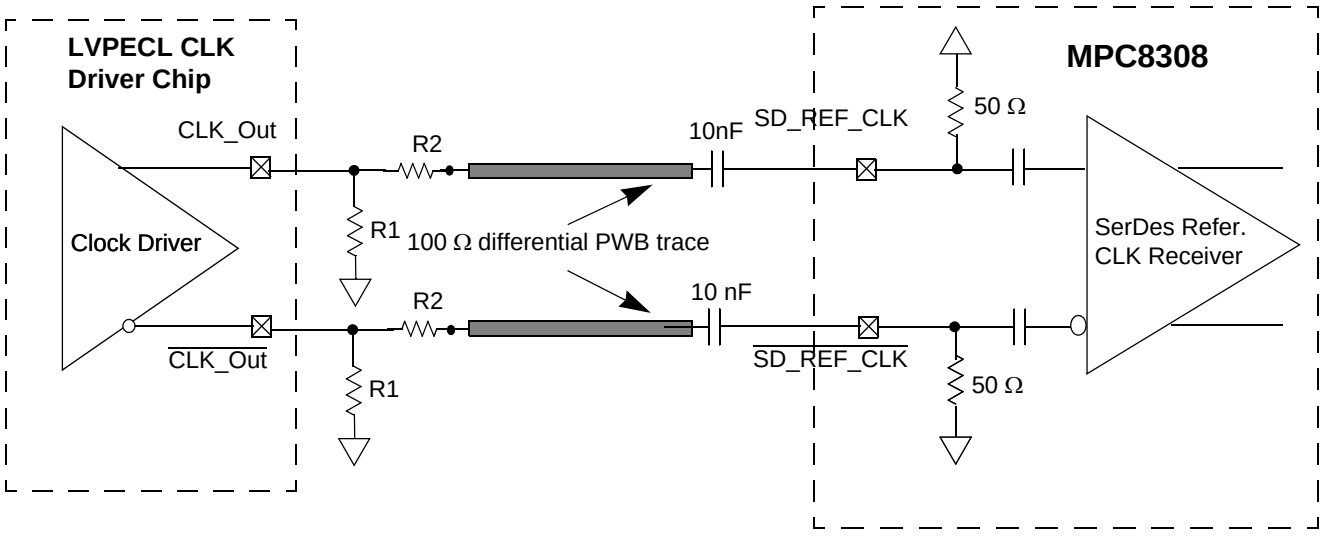


Figure 22. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Table 32. SerDes Reference Clock AC Parameters (continued)

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
Rising edge rate (SD_REF_CLK) to falling edge rate ($\overline{\text{SD\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing (Figure 24).
4. Matching applies to rising edge rate for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate (See Figure 25).

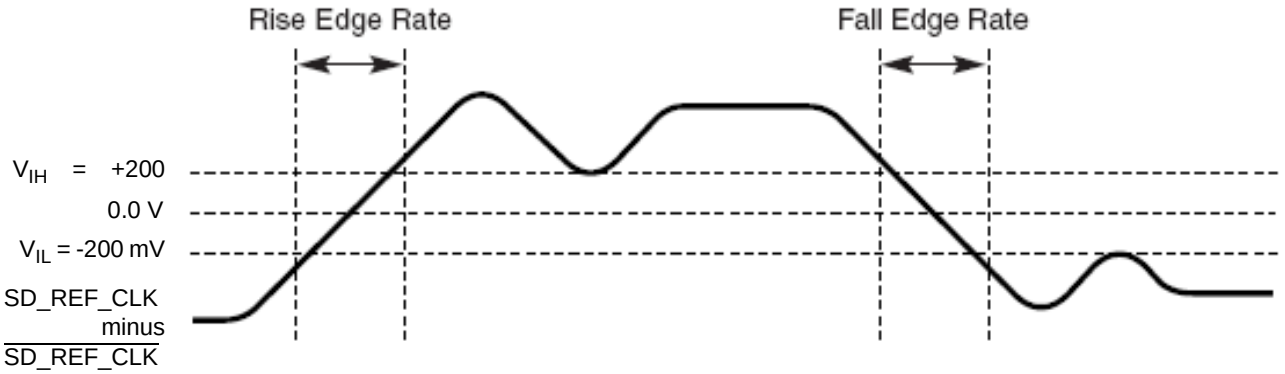


Figure 24. Differential Measurement Points for Rise and Fall Time

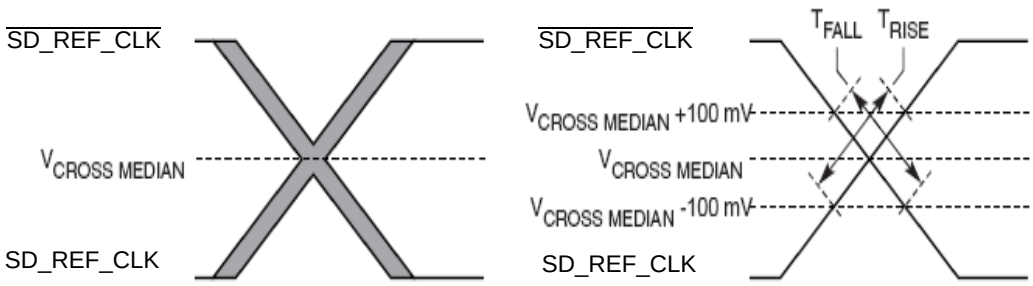


Figure 25. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. For detailed information, see the following sections:

- Section 11.2, “AC Requirements for PCI Express SerDes Clocks”

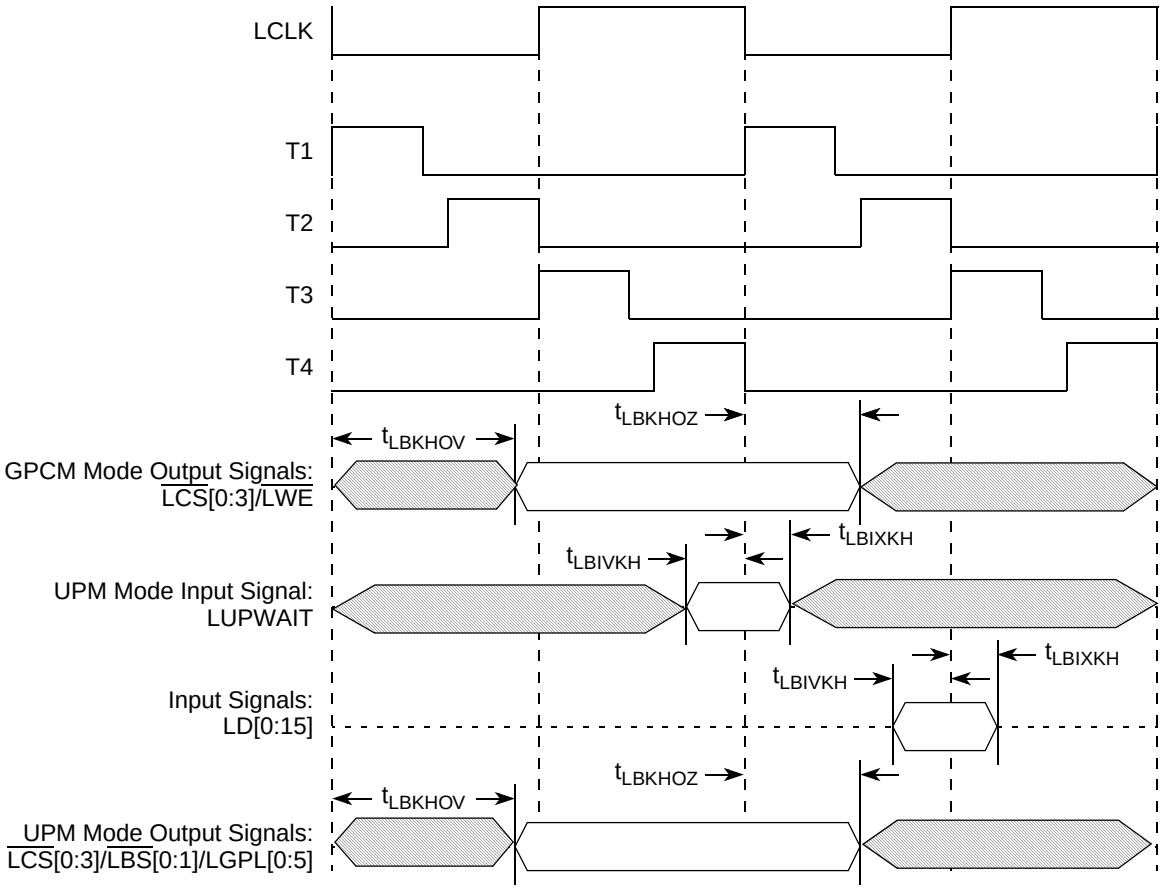


Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4

13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SD/MMC/SDIO) interface of the MPC8308.

The eSDHC controller always uses the falling edge of the SD_CLK in order to drive the SD_DAT[0:3]/CMD as outputs and rising edge to sample the SD_DAT[0:3], CMD, $\overline{\text{CD}}$ and WP as inputs. This behavior is true for both full and high speed modes.

13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device, compatible with SDHC specifications. The eSDHC NV_{DD} range is between 3.0 V and 3.6 V.

Table 38. eSDHC interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

This figure provides the $\overline{\text{TRST}}$ timing diagram.

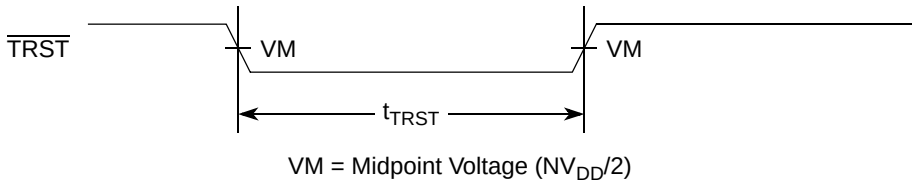


Figure 42. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

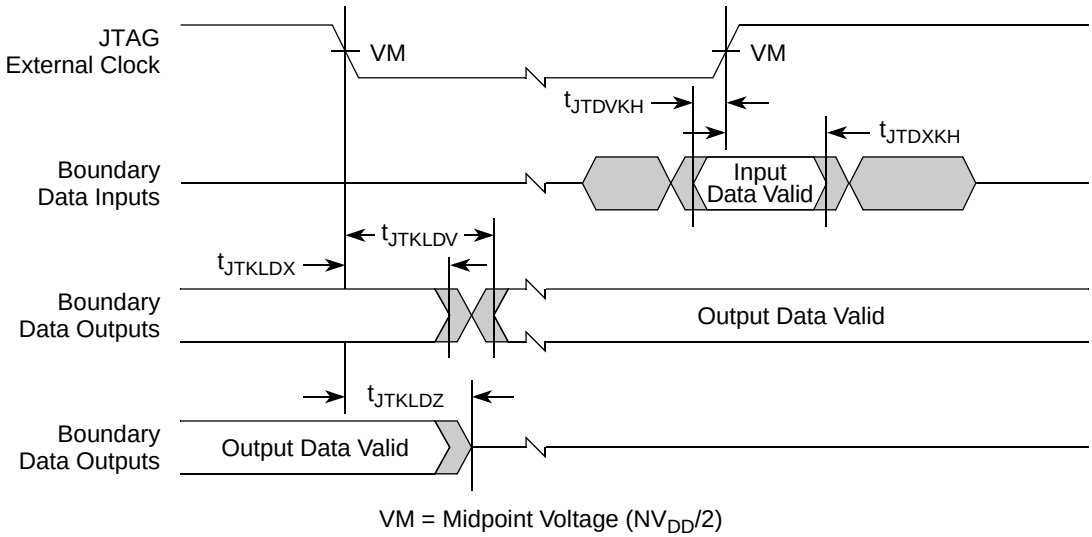


Figure 43. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.

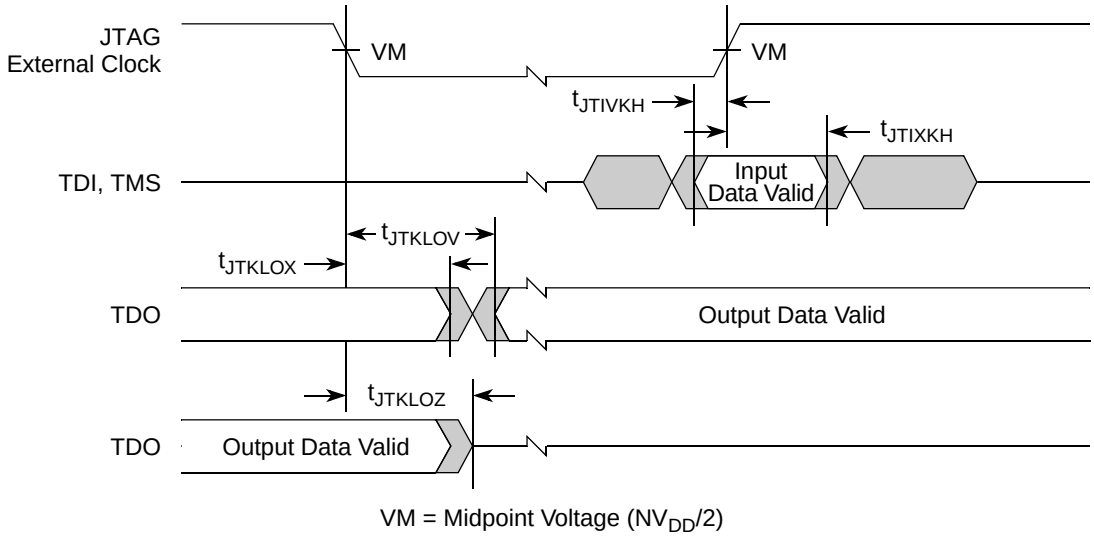


Figure 44. Test Access Port Timing Diagram

16 Timers

This section describes the DC and AC electrical specifications for the timers.

16.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8308 timers pins, including TIN, $\overline{\text{TOUT}}$, and $\overline{\text{TGATE}}$.

Table 45. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

16.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 46. Timers Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the Timers.

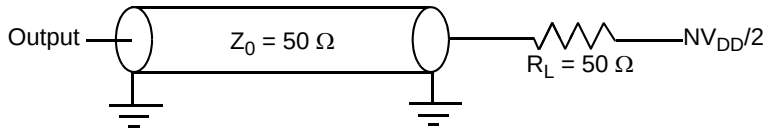
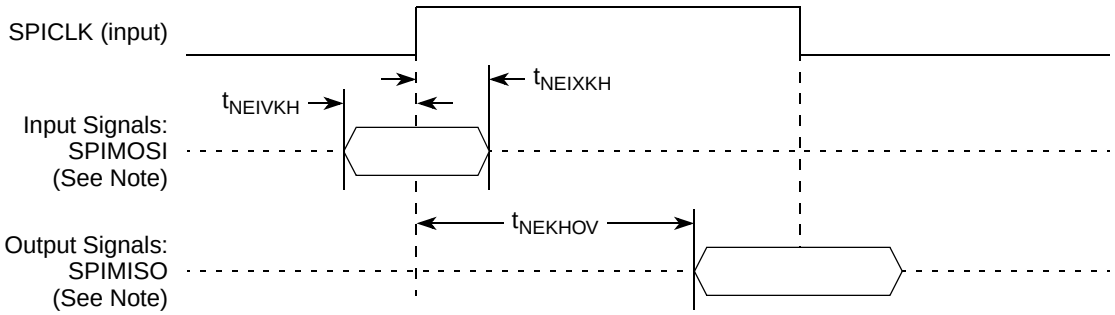


Figure 47. Timers AC Test Load

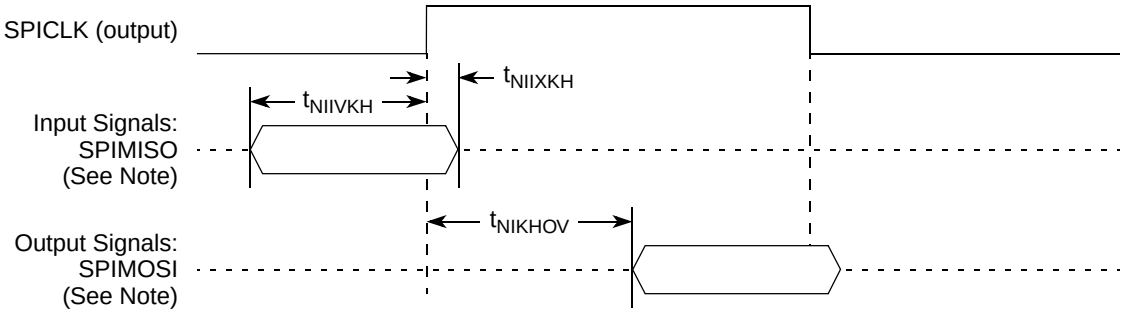
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 51. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8308 is available in a moulded array process ball grid array (MAPBGA). For information on the MAPBGA, see Section 20.1, "Package Parameters for the MPC8308 MAPBGA," and Section 20.2, "Mechanical Dimensions of the MPC8308 MAPBGA."

20.1 Package Parameters for the MPC8308 MAPBGA

The package parameters are as provided in the following list. The package type is 19 mm × 19 mm, 473 MAPBGA.

Package outline	19 mm × 19 mm
Interconnects	473
Pitch	0.80 mm
Module height (typical)	1.39 mm
Solder Balls	96.5 Sn/ 3.5Ag
Ball diameter (typical)	0.40 mm

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDQ[27]	M6	I/O	GV_{DDB}	—
MEMC_MDQ[28]	M2	I/O	GV_{DDB}	—
MEMC_MDQ[29]	M3	I/O	GV_{DDB}	—
MEMC_MDQ[30]	L2	I/O	GV_{DDB}	—
MEMC_MDQ[31]	L3	I/O	GV_{DDB}	—
MEMC_MDM[0]	AB2	O	GV_{DDA}	—
MEMC_MDM[1]	V3	O	GV_{DDA}	—
MEMC_MDM[2]	P3	O	GV_{DDB}	—
MEMC_MDM[3]	M7	O	GV_{DDB}	—
MEMC_MDM[8]	K2	O	GV_{DDB}	—
MEMC_MDQS[0]	AC3	I/O	GV_{DDA}	—
MEMC_MDQS[1]	V1	I/O	GV_{DDA}	—
MEMC_MDQS[2]	R1	I/O	GV_{DDB}	—
MEMC_MDQS[3]	M1	I/O	GV_{DDB}	—
MEMC_MDQS[8]	K1	I/O	GV_{DDB}	—
MEMC_MBA[0]	C3	O	GV_{DDB}	—
MEMC_MBA[1]	B2	O	GV_{DDB}	—
MEMC_MBA[2]	H4	O	GV_{DDB}	—
MEMC_MA0	C2	O	GV_{DDB}	—
MEMC_MA1	D2	O	GV_{DDB}	—
MEMC_MA2	D3	O	GV_{DDB}	—
MEMC_MA3	D4	O	GV_{DDB}	—
MEMC_MA4	E4	O	GV_{DDB}	—
MEMC_MA5	F4	O	GV_{DDB}	—
MEMC_MA6	E2	O	GV_{DDB}	—
MEMC_MA7	E1	O	GV_{DDB}	—
MEMC_MA8	F2	O	GV_{DDB}	—
MEMC_MA9	F3	O	GV_{DDB}	—
MEMC_MA10	C1	O	GV_{DDB}	—
MEMC_MA11	F7	O	GV_{DDB}	—
MEMC_MA12	G2	O	GV_{DDB}	—
MEMC_MA13	G3	O	GV_{DDB}	—
$\overline{\text{MEMC\_MWE}}$	D5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MRAS}}$	B4	O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

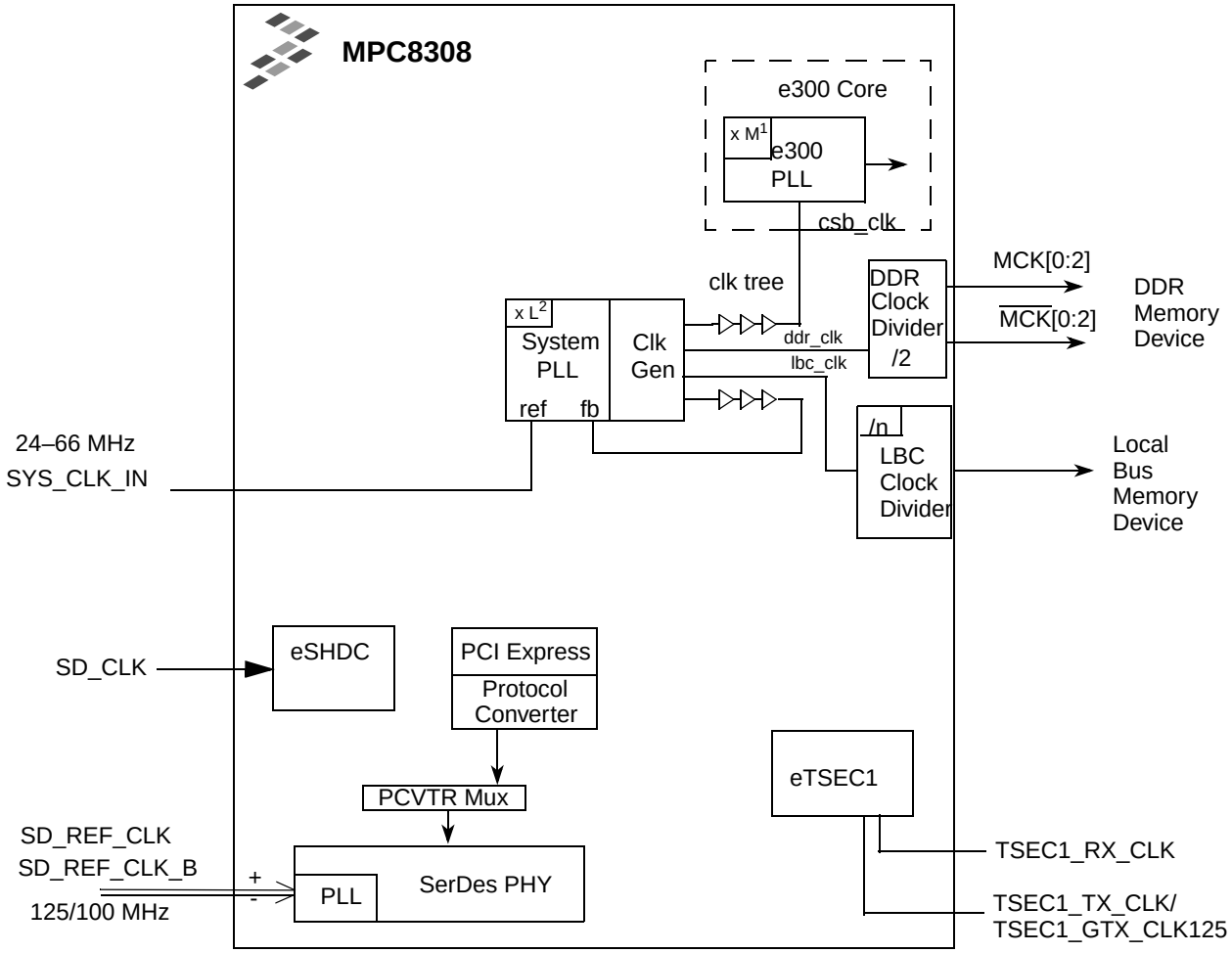
Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{LCS}}$[3]	Y11	O	NV_{DDP_K}	4
$\overline{\text{LWE}}$[0] /$\overline{\text{LFWE}}$0/$\overline{\text{LBS}}$0	AB11	O	NV_{DDP_K}	—
$\overline{\text{LWE}}$[1]/$\overline{\text{LBS}}$1	AC11	O	NV_{DDP_K}	—
LBCTL	U11	O	NV_{DDP_K}	—
LGPL0/LFCLE	Y10	O	NV_{DDP_K}	—
LGPL1/LFALE	AA10	O	NV_{DDP_K}	—
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AB10	O	NV_{DDP_K}	4
LGPL3/$\overline{\text{LFWP}}$	AC10	O	NV_{DDP_K}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LFRB	AB9	I/O	NV_{DDP_K}	4
LGPL5	Y9	O	NV_{DDP_K}	—
LCLK0	AC12	O	NV_{DDP_K}	—
DUART				
UART_SOUT1/MSRCID0/ LSRCID0	C17	O	NV_{DDB}	—
UART_SIN1/MSRCID1/ LSRCID1	B18	I/O	NV_{DDB}	—
UART_SOUT2/MSRCID2/ LSRCID2	D17	O	NV_{DDB}	—
UART_SIN2/MSRCID3/ LSRCID3	D18	I/O	NV_{DDB}	—
PEX PHY				
TXA	C14	O	XPADVDD	—
$\overline{\text{TXA}}$	C15	O	XPADVDD	—
RXA	A13	I	XCOREVDD	—
$\overline{\text{RXA}}$	B13	I	XCOREVDD	—
SD_IMP_CAL_RX	A15	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	C12	I	XCOREVDD	—
SD_REF_CLK	D12	I	XCOREVDD	—
SD_PLL_TPD	F13	O	—	—
SD_IMP_CAL_TX	A11	I	XPADVDD	—
SD_PLL_TPA_ANA	F11	O	—	—
SDAVDD_0	G12	I	—	—
SDAVSS_0	F12	I	—	—
I^2C interface				
IIC_SDA1	C9	I/O	NV_{DDA}	2

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPICLK	AA5	I/O	NV_{DDP_K}	—
SPISEL	AB4	I	NV_{DDP_K}	—
GPIO/ETSEC2				
GPIO[0]/TSEC2_COL	G21	I/O	NV_{DDF}	—
GPIO[1]/TSEC2_TX_ER	K23	I/O	NV_{DDF}	—
GPIO[2]/TSEC2_GTX_CLK	H18	I/O	NV_{DDF}	—
GPIO[3]/TSEC2_RX_CLK	G23	I/O	NV_{DDF}	—
GPIO[4]/TSEC2_RX_DV	J18	I/O	NV_{DDF}	—
GPIO[5]/TSEC2_RXD3	J20	I/O	NV_{DDF}	—
GPIO[6]/TSEC2_RXD2	H22	I/O	NV_{DDF}	—
GPIO[7]/TSEC2_RXD1	H21	I/O	NV_{DDF}	—
GPIO[8]/TSEC2_RXD0	H20	I/O	NV_{DDF}	—
GPIO[9]/TSEC2_RX_ER	J21	I/O	NV_{DDF}	—
GPIO[10]/TSEC2_TX_CLK/ TSEC2_GTX_CLK125	J23	I/O	NV_{DDF}	—
GPIO[11]/TSEC2_TXD3	K22	I/O	NV_{DDF}	—
GPIO[12]/TSEC2_TXD2	K20	I/O	NV_{DDF}	—
GPIO[13]/TSEC2_TXD1	K18	I/O	NV_{DDF}	—
GPIO[14]/TSEC2_TXD0	J17	I/O	NV_{DDF}	—
GPIO[15]/TSEC2_TX_EN	K21	I/O	NV_{DDF}	—
USB/IEEE1588/GTM				
USBDR_PWR_FAULT	P20	I	NV_{DDH}	—
USBDR_CLK	R23	I	NV_{DDH}	—
USBDR_DIR	R21	I	NV_{DDH}	—
USBDR_NXT	P18	I	NV_{DDH}	—
USBDR_TXDRXD0	T22	I/O	NV_{DDH}	—
USBDR_TXDRXD1	T21	I/O	NV_{DDH}	—
USBDR_TXDRXD2	U23	I/O	NV_{DDH}	—
USBDR_TXDRXD3	U22	I/O	NV_{DDH}	—
USBDR_TXDRXD4	T20	I/O	NV_{DDH}	—
USBDR_TXDRXD5	R18	I/O	NV_{DDH}	—
USBDR_TXDRXD6	V23	I/O	NV_{DDH}	—
USBDR_TXDRXD7	V22	I/O	NV_{DDH}	—
USBDR_PCTL0	R17	O	NV_{DDH}	—

21 Clocking

This figure shows the internal distribution of clocks within the device.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4, 5 and 6. Value is decided by RCWLR[SPMF].

Figure 53. MPC8308 Clock Subsystem

The following external clock sources are utilized on the MPC8308:

- System clock (SYS_CLK_IN)
- Ethernet Clock (TSEC1_RX_CLK/TSEC1_TX_CLK/TSEC1_GTX_CLK125 for eTSEC)
- SerDes PHY clock
- eSHDC clock (SD_CLK)

  For more information, see the SerDes chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

All clock inputs can be supplied using an external canned oscillator, a clock generation chip, or some other source that provides a standard CMOS square wave input.

This table provides the operating frequencies for the device under recommended operating conditions (Table 2).

Table 55. Operating Frequencies for MPC8308

Characteristic[1]	Maximum Operating Frequency	Unit
e300 core frequency (*core_clk*)	400	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
DDR2 memory bus frequency (MCK)[2]	133	MHz
Local bus frequency (LCLK*0*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK0, and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCCR[CLKDIV]) which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

21.2 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

Table 56. System PLL Ratio

RCWL[SPMF]	csb_clk: SYS_CLK_IN
0000	Reserved
0001	Reserved
0010	2 : 1
0011	3 : 1
0100	4 : 1
0101	5 : 1
0110–1111	Reserved

As described in Section 21, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (SYS_CLK_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN ratios.

Table 57. CSB Frequency Options

SPMF *csb_clk* :Input Clock Ratio		Input Clock Frequency (MHz)		
		25	33.33	66.67
0010	2:1			133
0100	4:1		133	
0101	5:1	125	167	

22.1 Thermal Characteristics

This table provides the package thermal characteristics for the 473, 19 × 19 mm MAPBGA.

Table 59. Package Thermal Characteristics for MAPBGA

Characteristic	Board Type	Symbol	Value	Unit	Note
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	42	°C/W	1, 2
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	27	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	35	°C/W	1, 3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W	1, 3
Junction to Board	—	$R_{\theta JB}$	17	°C/W	4
Junction to Case	—	$R_{\theta JC}$	9	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

22.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

22.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-t-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the device

23.1 System Clocking

The device includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 21.2, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.3, “Core PLL Configuration.”

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} for core PLL and AV_{DD2} for the platform PLL). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low pass filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 54, one to each of the two AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs’ resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

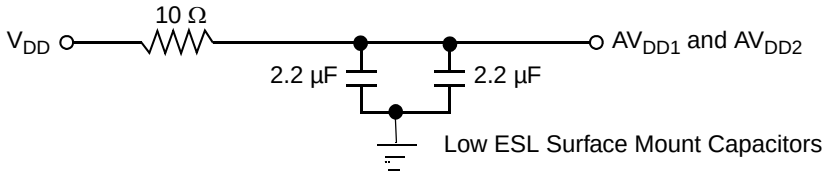


Figure 54. PLL Power Supply Filter Circuit

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