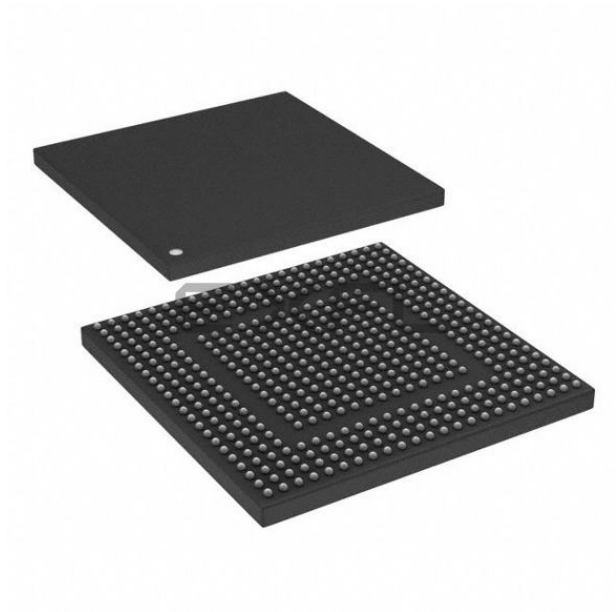

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Understanding Embedded - Microprocessors

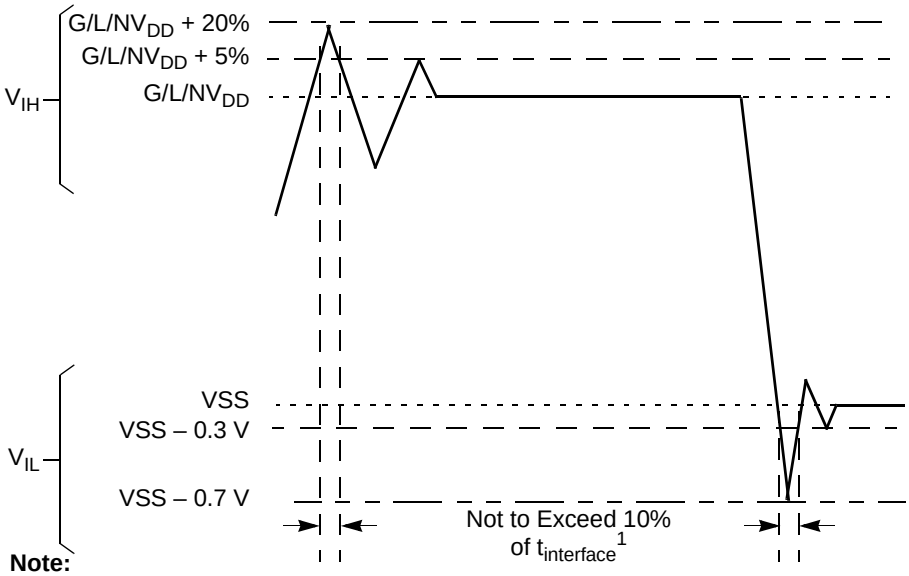
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8308zqagd

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GVDD/NVDD/LVDD

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NV_{DD} = 3.3 V
DDR2 signals[1]	18	GV_{DD} = 1.8 V
DUART, system control, I^2C, JTAG, eSDHC, GPIO,SPI, USB	42	NV_{DD} = 3.3 V
eTSEC signals	42	LV_{DD} = 2.5/3.3 V

[1] Output Impedance can also be adjusted through configurable options in DDR Control Driver Register (DDRCDR). For more information, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

2.1.4 Power Sequencing

It is required to apply the core supply voltage (V_{DD}) before the I/O supply voltages (GV_{DD}, LV_{DD}, and NV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. The core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3.

If this recommendation is not observed and I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. To overcome side effects of this condition, the application environment may require tuning of external pull-up or pull-down resistors on particular signals to lesser values.

This figure shows the DDR2 SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

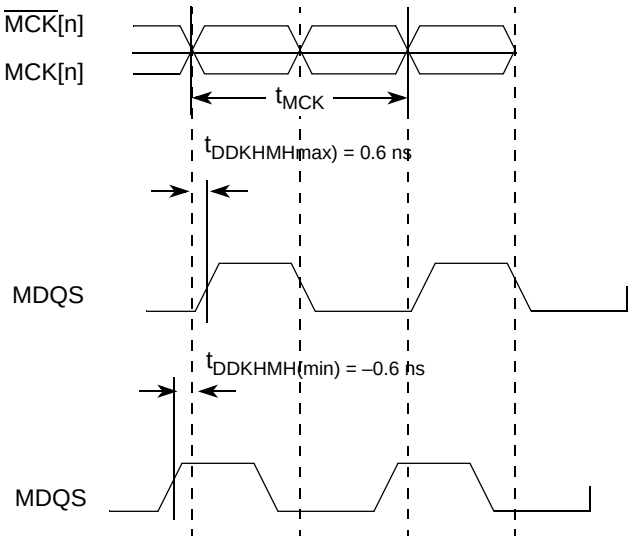


Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR2 SDRAM output timing diagram.

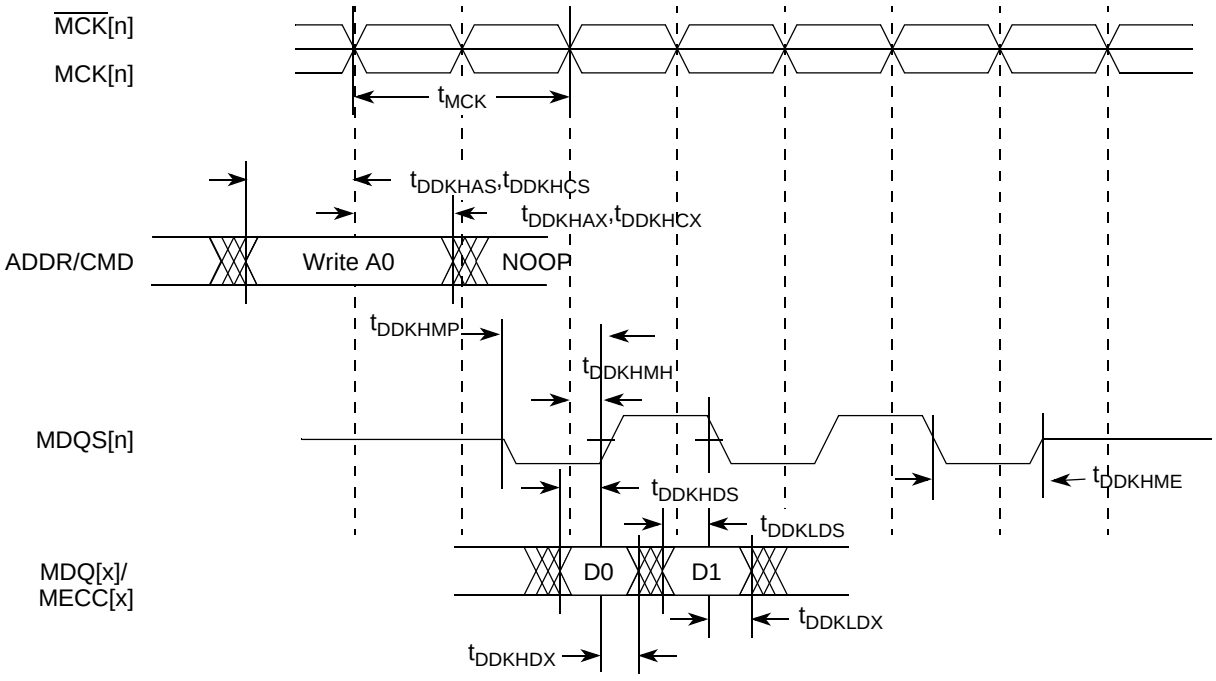


Figure 6. DDR2 SDRAM Output Timing Diagram

Table 25. RGMII AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of t_{RGT} represents the RGMII receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $0.5*LV_{DD}$
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

This figure shows the RGMII AC timing and multiplexing diagrams.

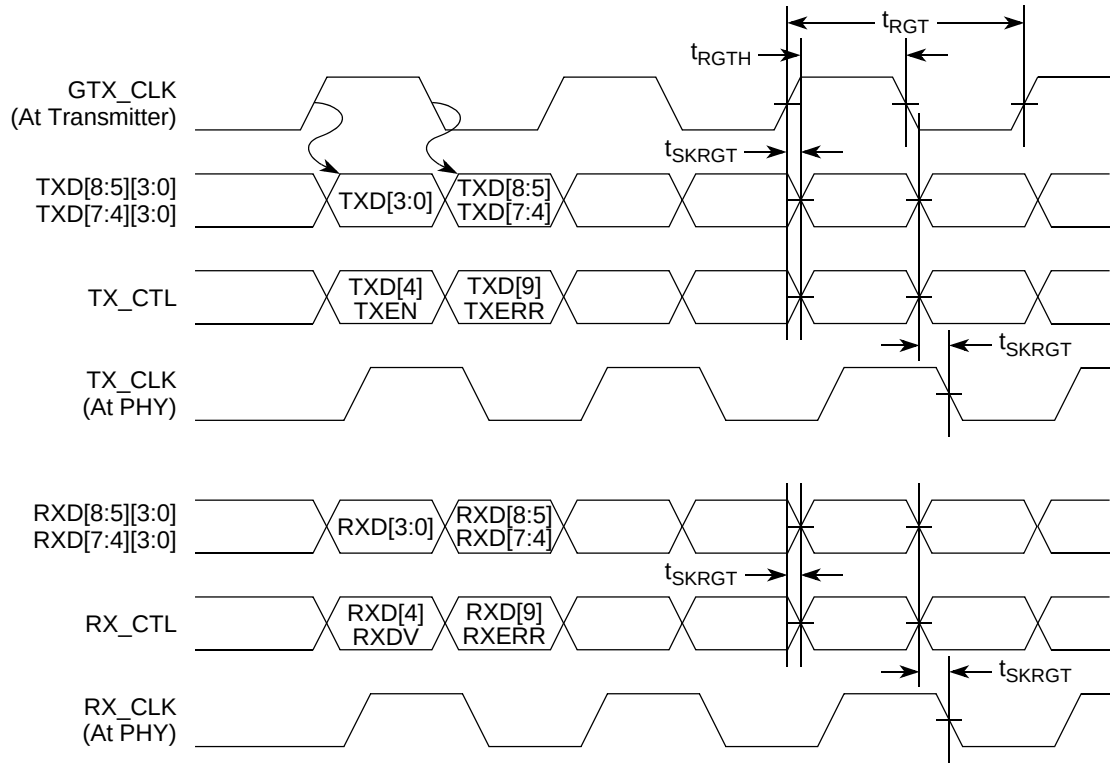


Figure 11. RGMII AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII

and RGMII are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. This table provides the DC electrical characteristics for MDIO and MDC.

Table 26. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NV_{DD}	—		3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DD} = Min	2.10	NV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	VSS	0.50	V
Input high voltage	V_{IH}	—		2.0	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	NV_{DD} = Max	V_{IN} [1] = 2.1 V	—	40	μA
Input low current	I_{IL}	NV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 27. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} is 3.3 V ± 0.3V

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

Table 28. GPIO DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NVDD$	—	± 5	μA

8.4.2 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

Table 29. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	—
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Note:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9 USB

9.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

9.1.1 USB DC Electrical Characteristics

This table lists the DC electrical characteristics for the USB interface.

Table 30. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LVDD + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	LVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

Table 34. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
AC coupling capacitor	C_{TX}	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. An external capacitor of 100nF is recommended.	75	—	200	nF	—
Crosslink random timeout	$T_{crosslink}$	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port.	0	—	1	ms	7

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 29 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 27.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 29). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 29 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.

11.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 27 is specified using the passive compliance/test measurement load (Figure 29) in place of any real PCI Express interconnect + RX component. There are two eye diagrams that must be met for the transmitter. Both diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending on whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI be calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

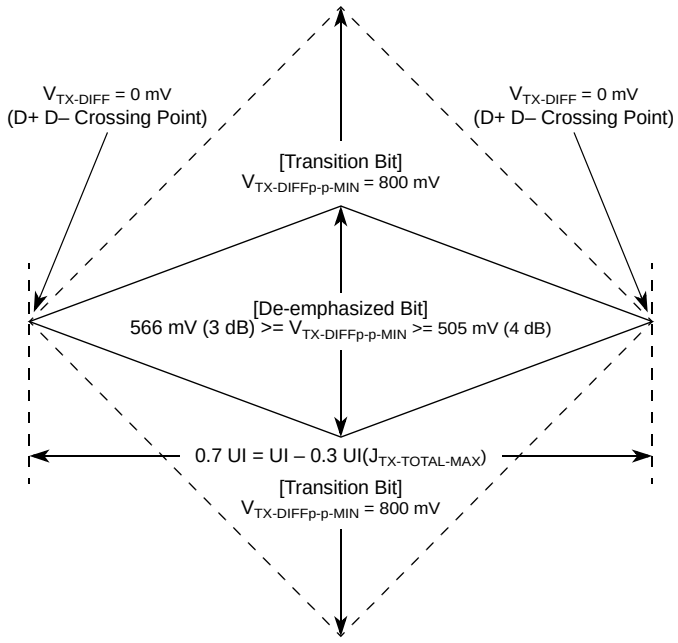


Figure 27. Minimum Transmitter Timing and Voltage Output Compliance Specifications

11.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 35. Differential Receiver (RX) Input Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Note
Unit interval	UI	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{RX-DIFFp-p}$	$V_{PEDPPRX} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	—	1.200	V	2
Minimum receiver eye width	T_{RX-EYE}	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - U_{PEEWRX} = 0.6$ UI.	0.4	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPRX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.3	UI	2, 3, 7

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 29). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

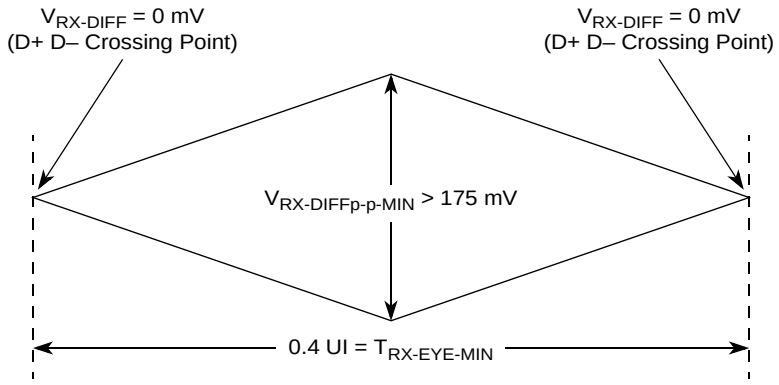


Figure 28. Minimum Receiver Eye Timing and Voltage Compliance Specification

11.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 29.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

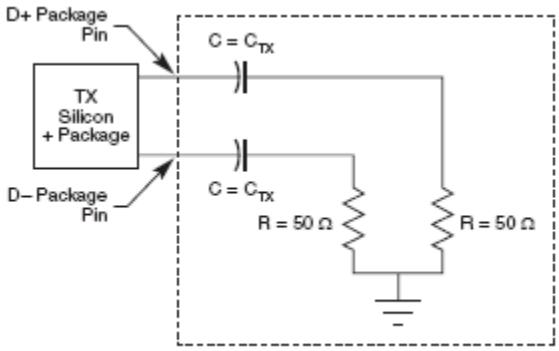


Figure 29. Compliance Test/Measurement Load

12 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

This figure provides the eSDHC clock input timing diagram.

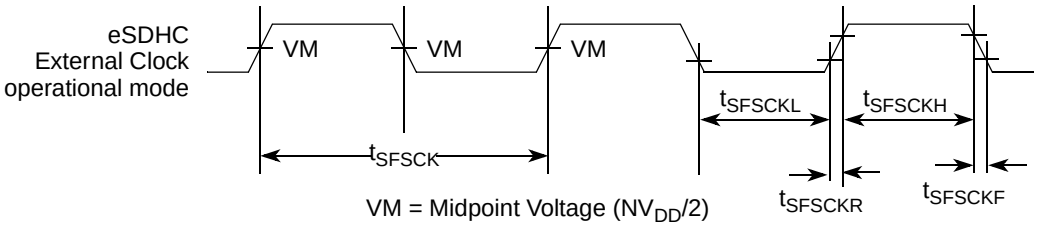


Figure 34. eSDHC Clock Input Timing Diagram

13.2.1 Full Speed Output Path (Write)

This figure provides the data and command output timing diagram.

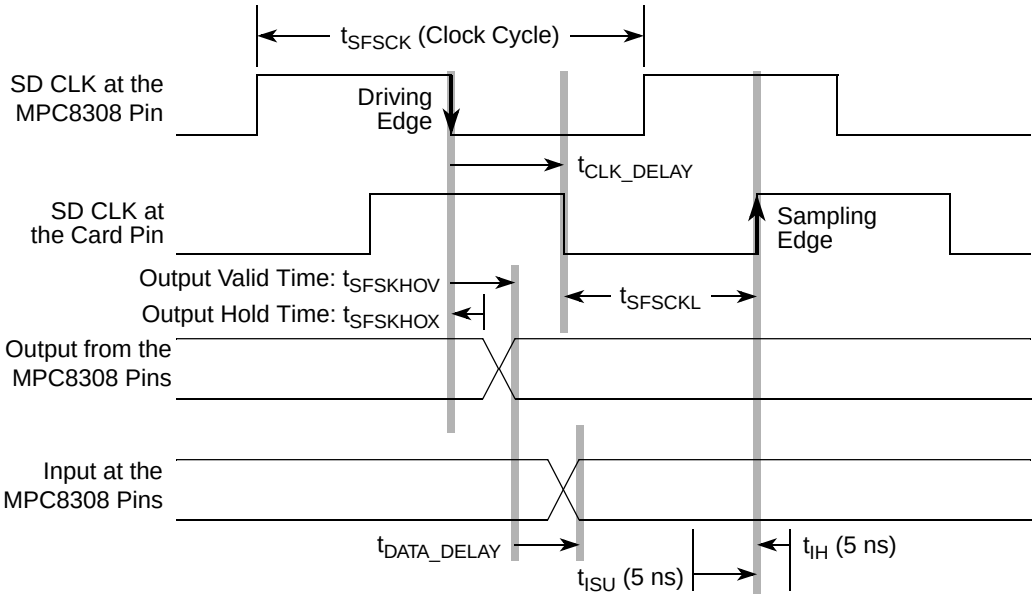


Figure 35. Full Speed Output Path

13.3.1 High Speed Output Path (Write)

This figure provides the data and command output timing diagram.

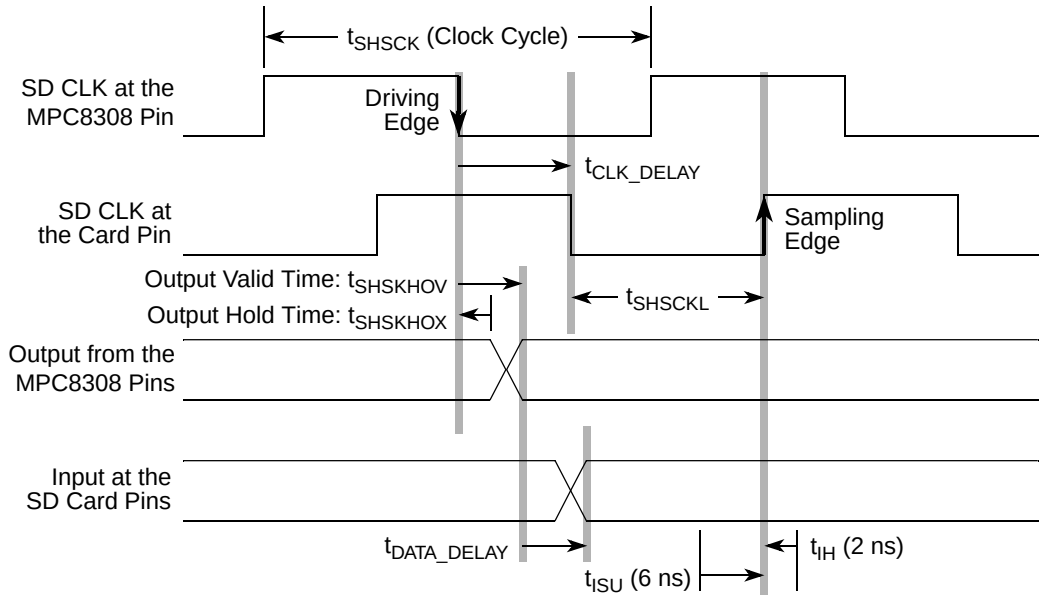


Figure 38. High Speed Output Path

13.3.2 High Speed Input Path (Read)

This figure provides the data and command input timing diagram.

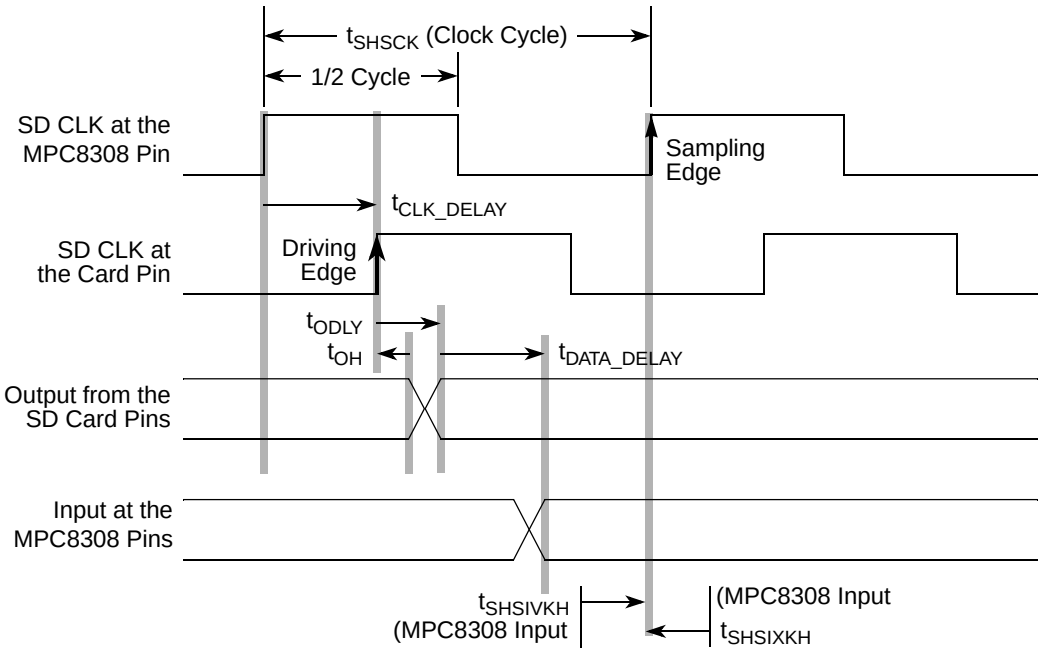


Figure 39. High Speed Input Path

15 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

15.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 43. I²C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times NV_{DD}$	$NV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times NV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times NV_{DD}$	V	1
High level output voltage	V_{OH}	$0.8 \times NV_{DD}$	$NV_{DD} + 0.3$	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current, ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	μA	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. For information on the digital filter used, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

15.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface.

Table 44. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	μs
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns

Table 44. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The device does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

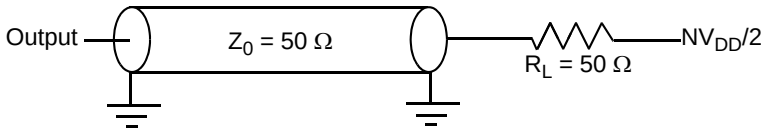


Figure 45. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

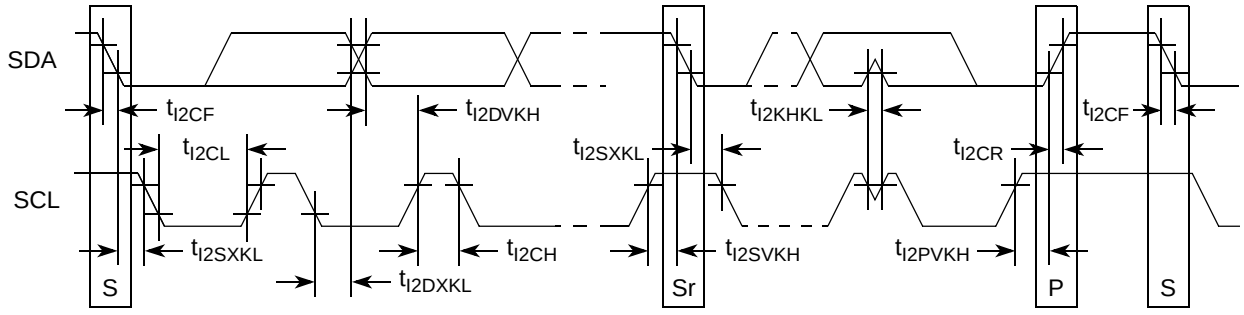


Figure 46. I²C Bus AC Timing Diagram

16 Timers

This section describes the DC and AC electrical specifications for the timers.

16.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8308 timers pins, including TIN, $\overline{\text{TOUT}}$, and $\overline{\text{TGATE}}$.

Table 45. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

16.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 46. Timers Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the Timers.

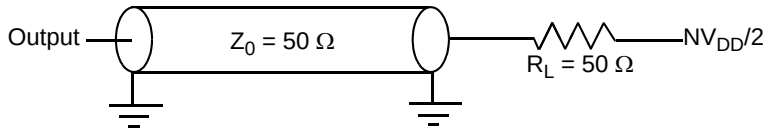


Figure 47. Timers AC Test Load

2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

20.3 Pinout Listings

This table provides the pin-out listing for the MPC8308, MAPBGA package.

Table 53. MPC8308 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	V6	I/O	GV_{DDA}	—
MEMC_MDQ[1]	Y4	I/O	GV_{DDA}	—
MEMC_MDQ[2]	AB3	I/O	GV_{DDA}	—
MEMC_MDQ[3]	AA3	I/O	GV_{DDA}	—
MEMC_MDQ[4]	AA2	I/O	GV_{DDA}	—
MEMC_MDQ[5]	AA1	I/O	GV_{DDA}	—
MEMC_MDQ[6]	W4	I/O	GV_{DDA}	—
MEMC_MDQ[7]	Y2	I/O	GV_{DDA}	—
MEMC_MDQ[8]	W3	I/O	GV_{DDA}	—
MEMC_MDQ[9]	W1	I/O	GV_{DDA}	—
MEMC_MDQ[10]	Y1	I/O	GV_{DDA}	—
MEMC_MDQ[11]	W2	I/O	GV_{DDA}	—
MEMC_MDQ[12]	U4	I/O	GV_{DDA}	—
MEMC_MDQ[13]	U3	I/O	GV_{DDA}	—
MEMC_MDQ[14]	V4	I/O	GV_{DDA}	—
MEMC_MDQ[15]	U6	I/O	GV_{DDA}	—
MEMC_MDQ[16]	T3	I/O	GV_{DDB}	—
MEMC_MDQ[17]	T2	I/O	GV_{DDB}	—
MEMC_MDQ[18]	R4	I/O	GV_{DDB}	—
MEMC_MDQ[19]	R3	I/O	GV_{DDB}	—
MEMC_MDQ[20]	P4	I/O	GV_{DDB}	—
MEMC_MDQ[21]	N6	I/O	GV_{DDB}	—
MEMC_MDQ[22]	P2	I/O	GV_{DDB}	—
MEMC_MDQ[23]	P1	I/O	GV_{DDB}	—
MEMC_MDQ[24]	N4	I/O	GV_{DDB}	—
MEMC_MDQ[25]	N3	I/O	GV_{DDB}	—
MEMC_MDQ[26]	N2	I/O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MEMC\_MCAS}}$	C5	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCS}}$[0]	B6	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCS}}$[1]	C6	O	GV_{DDB}	—
MEMC_MCKE	H3	O	GV_{DDB}	3
MEMC_MCK [0]	A3	O	GV_{DDB}	—
MEMC_MCK [1]	U2	O	GV_{DDB}	—
MEMC_MCK [2]	G1	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [0]	A4	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [1]	U1	O	GV_{DDB}	—
$\overline{\text{MEMC\_MCK}}$ [2]	H1	O	GV_{DDB}	—
MEMC_MODT[0]	A5	O	GV_{DDB}	—
MEMC_MODT[1]	B5	O	GV_{DDB}	—
MEMC_MECC[0]	L4	I/O	GV_{DDB}	—
MEMC_MECC[1]	L6	I/O	GV_{DDB}	—
MEMC_MECC[2]	K4	I/O	GV_{DDB}	—
MEMC_MECC[3]	K3	I/O	GV_{DDB}	—
MEMC_MECC[4]	J2	I/O	GV_{DDB}	—
MEMC_MECC[5]	K6	I/O	GV_{DDB}	—
MEMC_MECC[6]	J3	I/O	GV_{DDB}	—
MEMC_MECC[7]	J6	I/O	GV_{DDB}	—
MV_{REF}	G6	I	GV_{DDB}	—
Local Bus Controller Interface				
LD0	U18	I/O	NV_{DDP_K}	8
LD1	V18	I/O	NV_{DDP_K}	8
LD2	U16	I/O	NV_{DDP_K}	8
LD3	Y20	I/O	NV_{DDP_K}	8
LD4	AA21	I/O	NV_{DDP_K}	8
LD5	AC22	I/O	NV_{DDP_K}	8
LD6	V17	I/O	NV_{DDP_K}	8
LD7	AB21	I/O	NV_{DDP_K}	8
LD8	Y19	I/O	NV_{DDP_K}	8
LD9	AA20	I/O	NV_{DDP_K}	8
LD10	Y17	I/O	NV_{DDP_K}	8

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LD11	AC21	I/O	NV_{DDP_K}	8
LD12	AB20	I/O	NV_{DDP_K}	8
LD13	V16	I/O	NV_{DDP_K}	8
LD14	AA19	I/O	NV_{DDP_K}	8
LD15	AC17	I/O	NV_{DDP_K}	8
LA0	AC20	O	NV_{DDP_K}	—
LA1	Y16	O	NV_{DDP_K}	—
LA2	U15	O	NV_{DDP_K}	—
LA3	V15	O	NV_{DDP_K}	—
LA4	AA18	O	NV_{DDP_K}	—
LA5	AA17	O	NV_{DDP_K}	—
LA6	AC19	O	NV_{DDP_K}	—
LA7	AA16	O	NV_{DDP_K}	—
LA8	AB18	O	NV_{DDP_K}	—
LA9	AC18	O	NV_{DDP_K}	—
LA10	V14	O	NV_{DDP_K}	—
LA11	AB17	O	NV_{DDP_K}	—
LA12	AA15	O	NV_{DDP_K}	—
LA13	AC16	O	NV_{DDP_K}	—
LA14	Y14	O	NV_{DDP_K}	—
LA15	AC15	O	NV_{DDP_K}	—
LA16	U13	O	NV_{DDP_K}	—
LA17	V13	O	NV_{DDP_K}	—
LA18	Y13	O	NV_{DDP_K}	—
LA19	AB15	O	NV_{DDP_K}	—
LA20	AA14	O	NV_{DDP_K}	—
LA21	AB14	O	NV_{DDP_K}	—
LA22	U12	O	NV_{DDP_K}	—
LA23	V12	O	NV_{DDP_K}	—
LA24	Y12	O	NV_{DDP_K}	—
LA25	AC14	O	NV_{DDP_K}	—
$\overline{\text{LCS}}$[0]	AA13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[1]	AB13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[2]	AA12	O	NV_{DDP_K}	4

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
IIC_SCL1	A9	I/O	NV_{DDA}	2
IIC_SDA2/$\overline{\text{CKSTOP\_OUT}}$	D10	I/O	NV_{DDA}	2
IIC_SCL2/$\overline{\text{CKSTOP\_IN}}$	C10	I/O	NV_{DDA}	2
Interrupts				
IRQ[0]/$\overline{\text{MCP\_IN}}$	A17	I	NV_{DDB}	—
IRQ[1]/$\overline{\text{MCP\_OUT}}$	F16	I/O	NV_{DDB}	—
IRQ[2] /$\overline{\text{CKSTOP\_OUT}}$	B17	I/O	NV_{DDB}	—
IRQ[3] /$\overline{\text{CKSTOP\_IN}}$	A18	I	NV_{DDB}	—
JTAG				
TCK	Y7	I	NV_{DDP_K}	—
TDI	U9	I	NV_{DDP_K}	4
TDO	AC5	O	NV_{DDP_K}	3
TMS	AA6	I	NV_{DDP_K}	4
$\overline{\text{TRST}}$	V8	I	NV_{DDP_K}	4
TEST				
TEST_MODE	AC6	I	NV_{DDP_K}	5
System Control				
$\overline{\text{HRESET}}$	AA9	I/O	NV_{DDP_K}	1
$\overline{\text{PORESET}}$	AA8	I	NV_{DDP_K}	—
$\overline{\text{SRESET}}$	AB7	I/O	NV_{DDP_K}	—
Clocks				
SYS_CLK_IN	AC8	I	NV_{DDP_K}	—
RTC_PIT_CLOCK	AA23	I	NV_{DDJ}	—
MISC				
QUIESCE	AA7	O	NV_{DDP_K}	—
THERM0	AC7	I	NV_{DDP_K}	6
ETSEC1				
TSEC1_COL	B20	I	NV_{DDC}	—
TSEC1_CRS	B21	I	NV_{DDC}	—
TSEC1_GTX_CLK	F18	O	NV_{DDC}	3
TSEC1_RX_CLK	A22	I	NV_{DDC}	—
TSEC1_RX_DV	D21	I	NV_{DDC}	—
TSEC1_RXD[3]	C22	I	NV_{DDC}	—
TSEC1_RXD[2]	C21	I	NV_{DDC}	—

Table 53. MPC8308 Pinout Listing (continued)

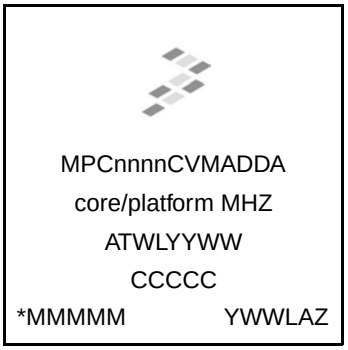
Signal	Package Pin Number	Pin Type	Power Supply	Note
SPICLK	AA5	I/O	NV_{DDP_K}	—
SPISEL	AB4	I	NV_{DDP_K}	—
GPIO/ETSEC2				
GPIO[0]/TSEC2_COL	G21	I/O	NV_{DDF}	—
GPIO[1]/TSEC2_TX_ER	K23	I/O	NV_{DDF}	—
GPIO[2]/TSEC2_GTX_CLK	H18	I/O	NV_{DDF}	—
GPIO[3]/TSEC2_RX_CLK	G23	I/O	NV_{DDF}	—
GPIO[4]/TSEC2_RX_DV	J18	I/O	NV_{DDF}	—
GPIO[5]/TSEC2_RXD3	J20	I/O	NV_{DDF}	—
GPIO[6]/TSEC2_RXD2	H22	I/O	NV_{DDF}	—
GPIO[7]/TSEC2_RXD1	H21	I/O	NV_{DDF}	—
GPIO[8]/TSEC2_RXD0	H20	I/O	NV_{DDF}	—
GPIO[9]/TSEC2_RX_ER	J21	I/O	NV_{DDF}	—
GPIO[10]/TSEC2_TX_CLK/ TSEC2_GTX_CLK125	J23	I/O	NV_{DDF}	—
GPIO[11]/TSEC2_TXD3	K22	I/O	NV_{DDF}	—
GPIO[12]/TSEC2_TXD2	K20	I/O	NV_{DDF}	—
GPIO[13]/TSEC2_TXD1	K18	I/O	NV_{DDF}	—
GPIO[14]/TSEC2_TXD0	J17	I/O	NV_{DDF}	—
GPIO[15]/TSEC2_TX_EN	K21	I/O	NV_{DDF}	—
USB/IEEE1588/GTM				
USBDR_PWR_FAULT	P20	I	NV_{DDH}	—
USBDR_CLK	R23	I	NV_{DDH}	—
USBDR_DIR	R21	I	NV_{DDH}	—
USBDR_NXT	P18	I	NV_{DDH}	—
USBDR_TXDRXD0	T22	I/O	NV_{DDH}	—
USBDR_TXDRXD1	T21	I/O	NV_{DDH}	—
USBDR_TXDRXD2	U23	I/O	NV_{DDH}	—
USBDR_TXDRXD3	U22	I/O	NV_{DDH}	—
USBDR_TXDRXD4	T20	I/O	NV_{DDH}	—
USBDR_TXDRXD5	R18	I/O	NV_{DDH}	—
USBDR_TXDRXD6	V23	I/O	NV_{DDH}	—
USBDR_TXDRXD7	V22	I/O	NV_{DDH}	—
USBDR_PCTL0	R17	O	NV_{DDH}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
USBDR_PCTL1	U20	O	NV_{DDH}	—
USBDR_STP	V21	O	NV_{DDH}	—
TSEC_TMR_CLK/ GPIO[8]	W23	I	NV_{DDH}	—
GTM1_TOUT3/ GPIO[9]	T18	O	NV_{DDH}	—
GTM1_TOUT4/ GPIO[10]	V20	O	NV_{DDH}	—
TSEC_TMR_TRIG1/ GPIO[11]	W21	I	NV_{DDH}	—
TSEC_TMR_TRIG2/ GPIO[12]	Y21	I	NV_{DDH}	—
TSEC_TMR_GCLK	L17	O	NV_{DDG}	—
TSEC_TMR_PP1	L18	O	NV_{DDG}	—
TSEC_TMR_PP2	L21	O	NV_{DDG}	—
TSEC_TMR_PP3/ GPIO[13]	L22	O	NV_{DDG}	—
TSEC_TMR_ALARM1	L23	O	NV_{DDG}	—
TSEC_TMR_ALARM2/ GPIO[14]	M23	O	NV_{DDG}	—
GPIO[7]	M22	IO	—	—
TSEC2_CRS/ GPIO[0]	M21	IO	NV_{DDG}	—
TSEC2_TMR_RX_ESFD/ GPIO[1]	M18	O	NV_{DDG}	—
TSEC2_TMR_TX_ESFD/ GPIO[2]	M20	O	NV_{DDG}	—
TSEC1_TMR_RX_ESFD/ GPIO[3]	N23	O	NV_{DDG}	—
TSEC1_TMR_TX_ESFD/ GPIO[4]	N21	O	NV_{DDG}	—
GTM1_TGATE3	N20	I	NV_{DDG}	—
GTM1_TIN4	N18	I	NV_{DDG}	—
GTM1_TGATE4/ GPIO[15]	P23	I	NV_{DDG}	—
GTM1_TIN3	P22	I	NV_{DDG}	—
GPIO[5]	N17	IO	NV_{DDH}	—
GPIO[6]	P21	IO	NV_{DDH}	—
Power and Ground Supplies				
AV_{DD1}	R6	I	—	—
AV_{DD2}	V10	I	—	—
NC, No Connection	B11, B16, D16	—	—	—

24.2 Part Marking

Parts are marked as in the example shown in this figure.



PBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 56. Freescale Part Marking for PBGA Devices

This table lists the SVR settings.

Table 62. SVR Settings

Device	Package	SVR
MPC8308	MAPBGA	0x8101 _0110

Note: PVR = 8085_0020 for the device.