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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3846axe-175

It also contains a separate, very low-power internal low-speed oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in real-time clock (RTC) applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C38 family supports a wide supply operating range from 1.71 V to 5.5 V. This allows operation from regulated supplies such as 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, or 5.0 V \pm 10%, or directly from a wide range of battery types.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1- μ A sleep mode with RTC. In the second mode, the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the “Power System” section on page 29 of this data sheet.

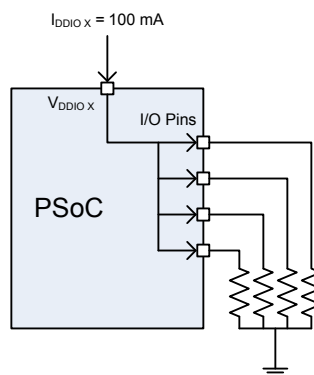
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for ‘printf’ style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces you can debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data trace memory for debug. Details of the programming, test, and debugging interfaces are discussed in the “Programming, Debug Interfaces, Resources” section on page 60 of this data sheet.

2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-4 show the pins that are powered by each VDDIO.

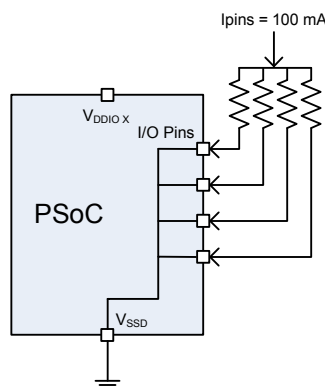
Each VDDIO may source up to 100 mA^[8] total to its associated I/O pins, as shown in Figure 2-1.

Figure 2-1. VDDIO Current Limit



Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA^[8] total, as shown in Figure 2-2.

Figure 2-2. I/O Pins Current Limit

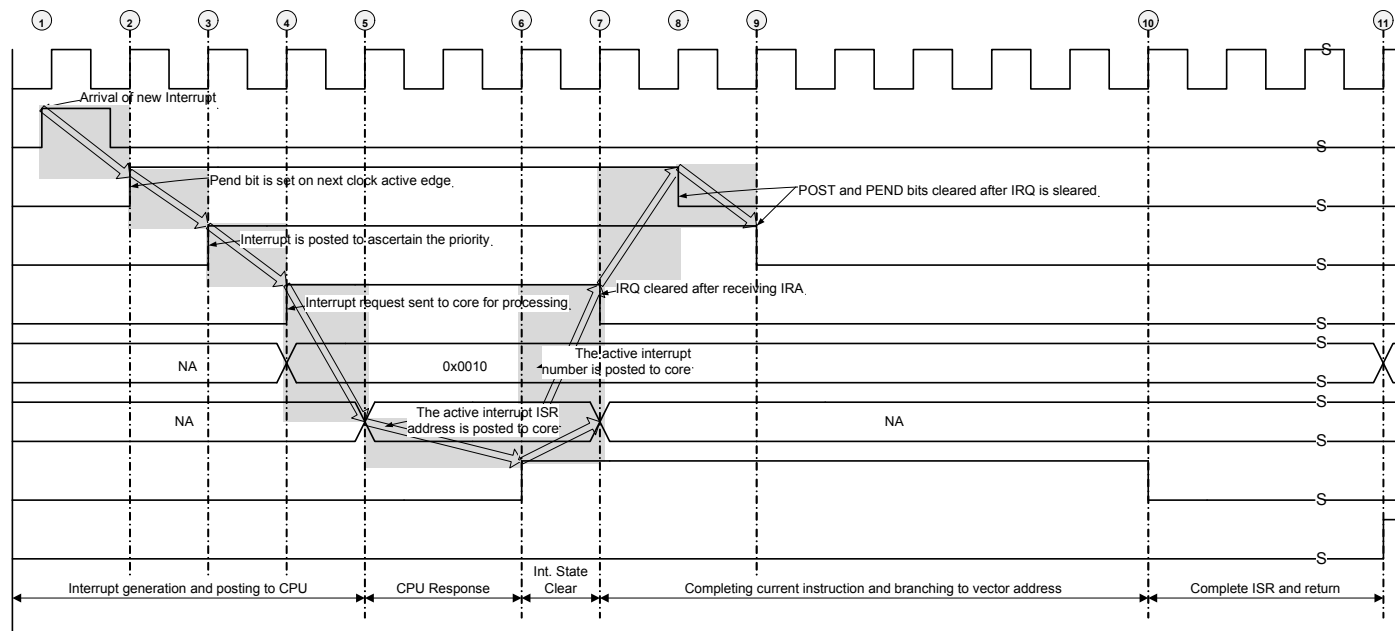


For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA^[8] total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.

Note

8. The 100 mA source/sink current per Vddio is valid only for temperature range of -40°C to $+85^{\circ}\text{C}$. For extended temperature range of -40°C to $+125^{\circ}\text{C}$, the maximum source or sink current per Vddio is 40 mA.

Figure 4-2. Interrupt Processing Timing Diagram



Notes

- 1: Interrupt triggered asynchronous to the clock
- 2: The PEND bit is set on next active clock edge to indicate the interrupt arrival
- 3: POST bit is set following the PEND bit
- 4: Interrupt request and the interrupt number sent to CPU core after evaluation priority (Takes 3 clocks)
- 5: ISR address is posted to CPU core for branching
- 6: CPU acknowledges the interrupt request
- 7: ISR address is read by CPU for branching
- 8, 9: PEND and POST bits are cleared respectively after receiving the IRA from core
- 10: IRA bit is cleared after completing the current instruction and starting the instruction execution from ISR location (Takes 7 cycles)
- 11: IRC is set to indicate the completion of ISR, Active int. status is restored with previous status

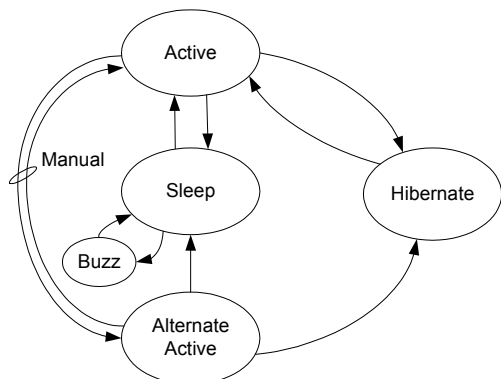
The total interrupt latency (ISR execution)

= POST + PEND + IRQ + IRA + Completing current instruction and branching

= 1+1+1+2+7 cycles

= 12 cycles

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode reduces power consumption when a resume time of 15 μ s is acceptable. The wake time is used to ensure that the regulator outputs are stable enough to directly enter active mode.

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external I/O interrupt. The resume time from hibernate mode is less than 100 μ s.

To achieve an extremely low current, the hibernate regulator has limited capacity. This limits the frequency of any signal present on the input pins - no GPIO should toggle at a rate greater than 10 kHz while in hibernate mode. If pins must be toggled at a high rate while in a low power mode, use sleep mode instead.

6.2.1.5 Wakeup Events

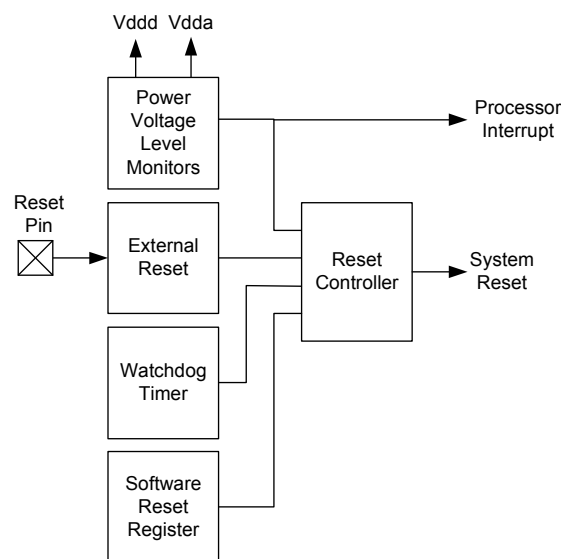
Wakeup events are configurable and can come from an interrupt or device reset. A wakeup event restores the system to active mode. Firmware enabled interrupt sources include internally generated interrupts, power supervisor, central timewheel, and I/O interrupts. Internal interrupt sources can come from a variety of peripherals, such as analog comparators and UDBs. The central timewheel provides periodic interrupts to allow the system to wake up, poll peripherals, or perform real-time functions. Reset event sources include the external reset I/O pin (XRES), WDT, and precision reset (PRES).

6.3 Reset

CY8C38 has multiple internal and external reset sources available. The reset sources are:

- **Power source monitoring** – The analog and digital power voltages, VDDA, VDDD, VCCA, and VCCD are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- **External** – The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to VDDIO1. VDDD, VDDA, and VDDIO1 must all have voltage applied before the part comes out of reset.
- **Watchdog timer** – A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- **Software** – The device can be reset under program control.

Figure 6-6. Resets



The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to

Figure 6-8. SIO Input/Output Block Diagram

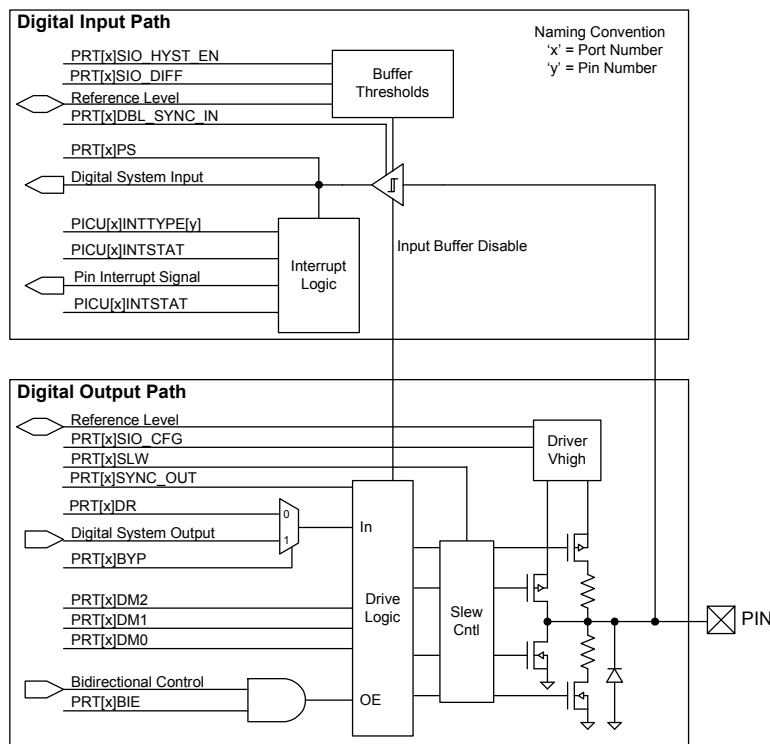
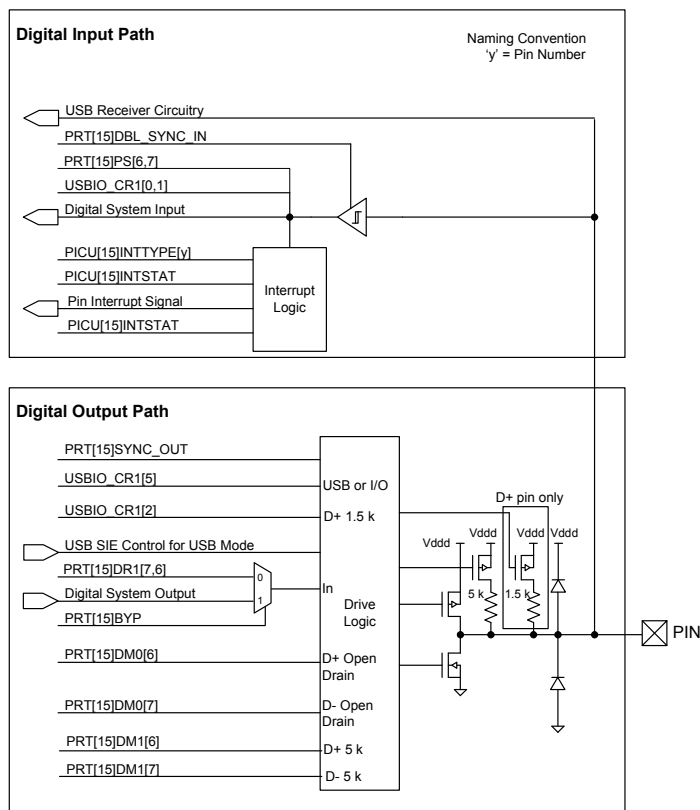


Figure 6-9. USBIO Block Diagram



6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-5. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-10 depicts a simplified pin view based on each of the eight drive modes. Table 6-5 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-10. Drive Mode

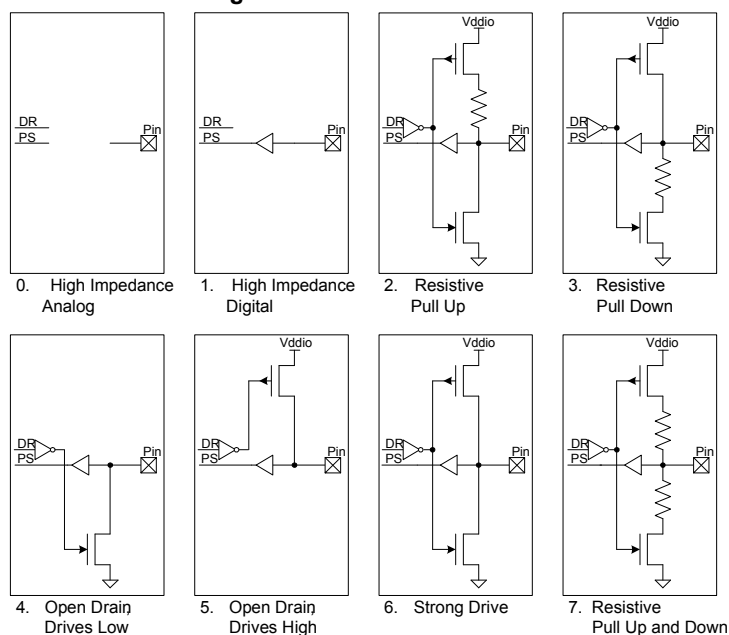


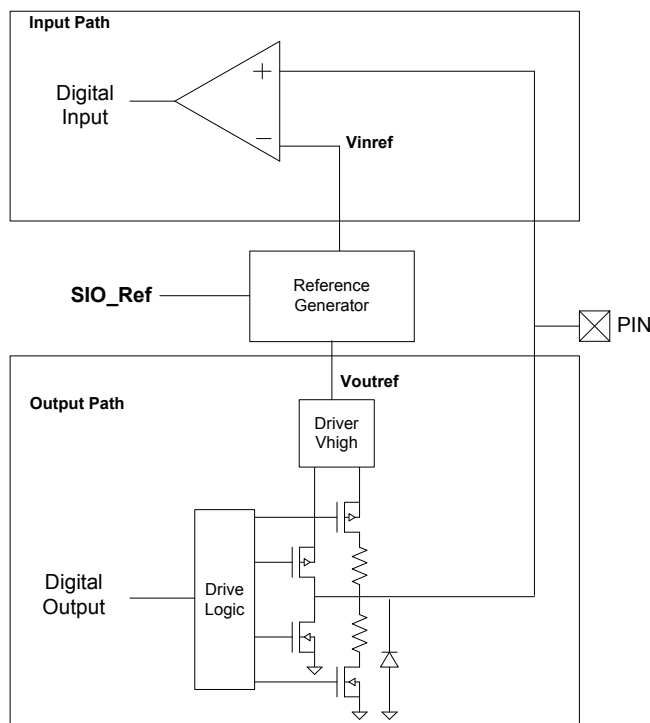
Table 6-5. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedance analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up ^[14]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down ^[14]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down ^[14]	1	1	1	Res High (5K)	Res Low (5K)

Note

¹⁴. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

Figure 6-11. SIO Reference for Input and Output



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the [Adjustable Input Level](#) section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold. The digital input path in [Figure 6-8](#) on page 35 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I2C bus may cause transient states on the SIO pins. The overall I2C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating V_{DD} .

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where $V_{DDIO} \leq V_{IN} \leq 5.5$ V.
- The GPIO pins must be limited to 100 μ A using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply where $V_{DDIO} \leq V_{IN} \leq V_{DDA}$.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I²C where different devices are running from different supply voltages. In the I²C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I²C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated VDDIO supply pin. The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See [Figure 6-10](#) for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in [Pinouts](#) on page 5. The special features are:

- Digital
 - 4- to 25-MHz crystal oscillator
 - 32.768-kHz crystal oscillator
 - Wake from sleep on I²C address match. Any pin can be used for I²C if wake from sleep is not required.
 - JTAG interface pins
 - SWD interface pins
 - SWV interface pins
 - External reset
- Analog
 - Opamp inputs and outputs
 - High current IDAC outputs
 - External reference inputs

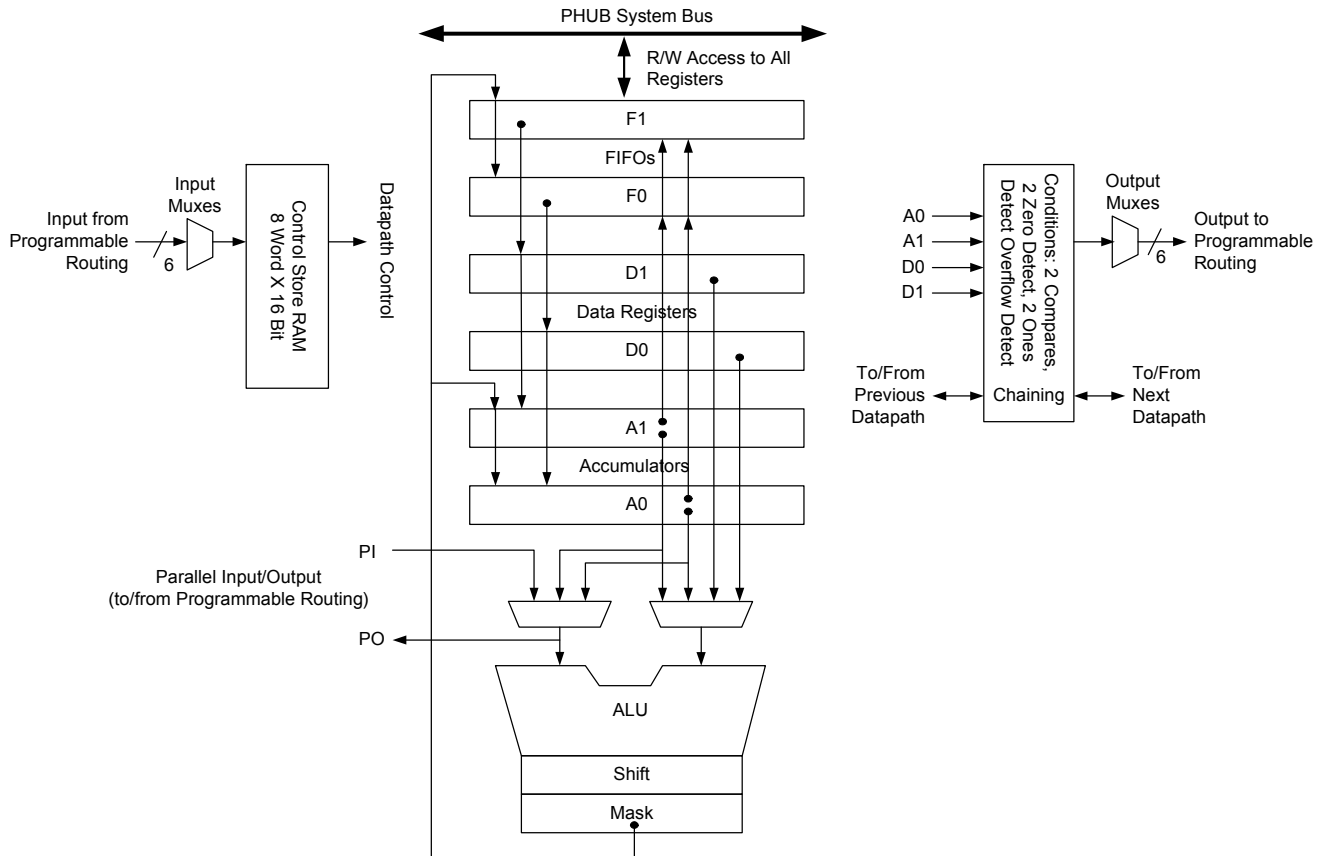
6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Datapath Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

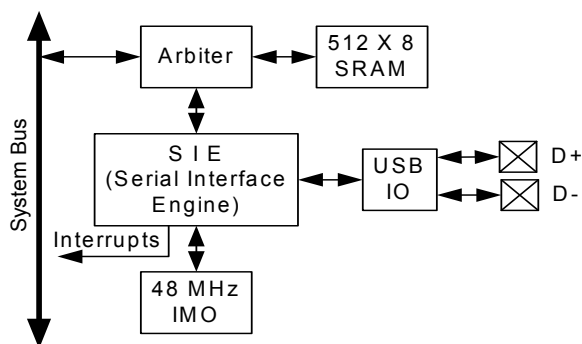
7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the “I/O System and Routing” section on page 33.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
 - ▢ Manual memory management with no DMA access
 - ▢ Manual memory management with manual DMA access
 - ▢ Automatic memory management with automatic DMA access
- Internal 3.3-V regulator for transceiver
- Internal 48-MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB reset, suspend, and resume operations
- Bus-powered and self-powered modes

Figure 7-16. USB



7.7 Timers, Counters, and PWMs

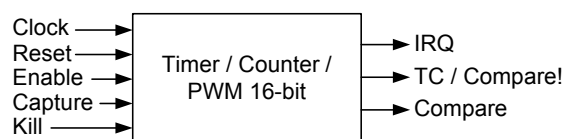
The timer/counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in UDBs as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The timer/counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-17. Timer/Counter/PWM



7.8 I²C

The I²C peripheral provides a synchronous two wire interface designed to interface the PSoC device with a two wire I²C serial communication bus. It is compatible^[16] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O may be implemented with GPIO or SIO in open-drain modes. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master).^[17] In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through DSI routing and allows direct connections to any GPIO or SIO pins.

I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup

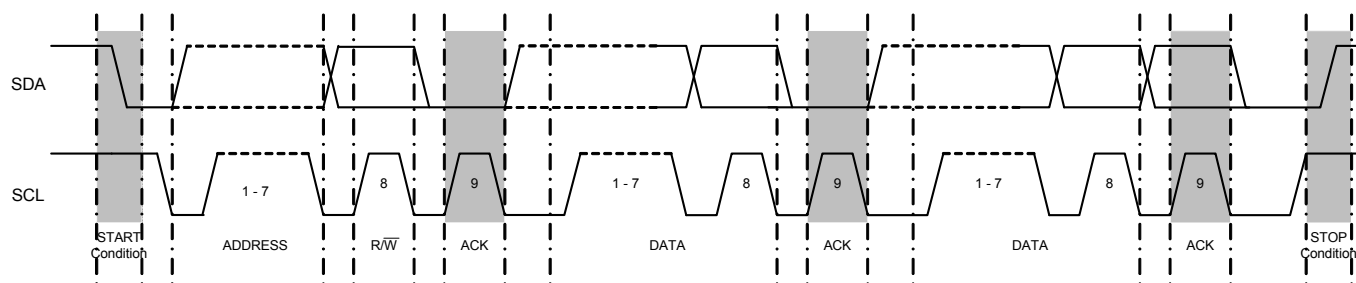
functionality is required, I²C pin connections are limited to the two special sets of SIO pins.

I²C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in Figure 7-18. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

Figure 7-18. I²C Complete Transfer Timing



Notes

16. The I²C peripheral is non-compliant with the NXP I²C specification in the following areas: analog glitch filter, I/O V_{OL}/I_{OL}, I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 74 for details.
17. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in CY8C38, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

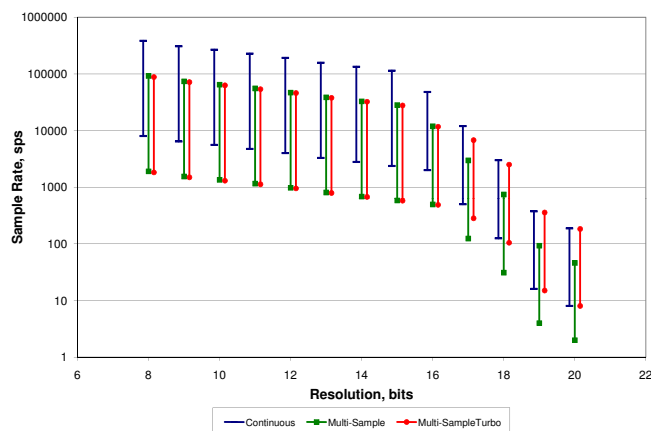
8.2 Delta-sigma ADC

The CY8C38 device contains one delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for both audio signal processing and measurement applications. The converter's nominal operation is 16 bits at 48 ksp/s. The ADC can be configured to output 20-bit resolution at data rates of up to 187 sps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1. Delta-sigma ADC Performance

Bits	Maximum Sample Rate (sps)	SINAD (dB)
20	187	—
16	48 k	83
12	192 k	66
8	384 k	43

Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V

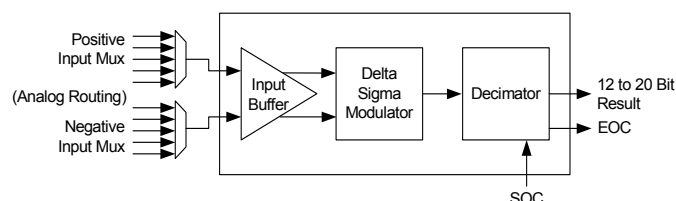


8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic

block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.3.2 LUT

The CY8C38 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

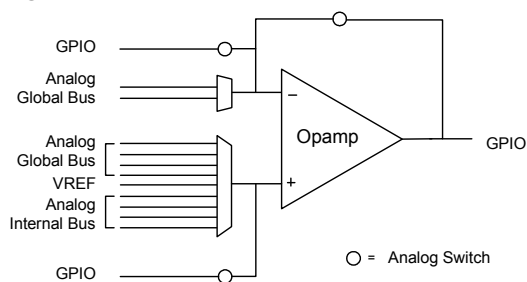
Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	FALSE ('0')
0001b	A AND B
0010b	A AND (NOT B)
0011b	A
0100b	(NOT A) AND B
0101b	B
0110b	A XOR B
0111b	A OR B
1000b	A NOR B
1001b	A XNOR B
1010b	NOT B
1011b	A OR (NOT B)
1100b	NOT A
1101b	(NOT A) OR B
1110b	A NAND B
1111b	TRUE ('1')

8.4 Opamps

The CY8C38 family of devices contain up to four general purpose opamps in a device.

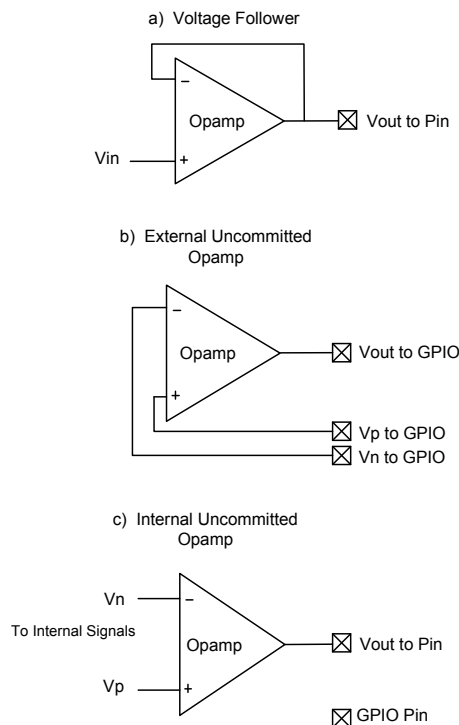
Figure 8-6. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-7. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-7. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

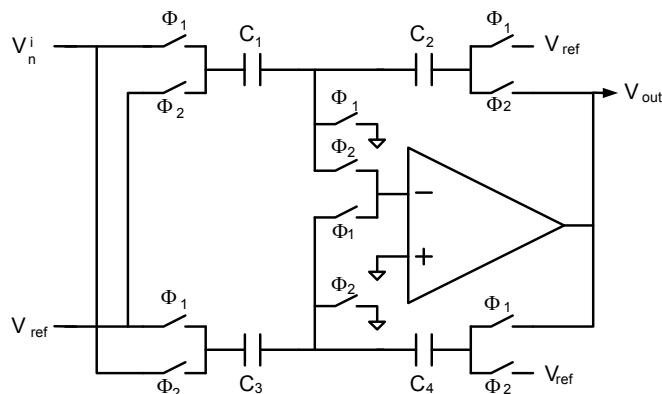
The CY8C38 family of devices contains up to four switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

Figure 8-13. Sample and Hold Topology
(Φ_1 and Φ_2 are opposite phases of a clock)



8.11.1 Down Mixer

The SC/CT block can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.11.2 First Order Modulator – SC Mode

A first order modulator is constructed by placing the SC/CT block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors.

The main application for this modulator is for a low-frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement.

9. Programming, Debug Interfaces, Resources

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. Three interfaces are available: JTAG, SWD, and SWV. JTAG and SWD support all programming and debug features of the device. JTAG also supports standard JTAG scan chains for board level test and chaining multiple JTAG devices to a single JTAG connection.

For more information on PSoC 3 Programming, refer to the [PSoC® 3 Device Programming Specifications](#).

Complete Debug on Chip (DoC) functionality enables full device debugging in the final system using the standard production

device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC JTAG, SWD, and SWV interfaces are fully compatible with industry standard third party tools.

All DOC circuits are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenables them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables DOC. Disabling DOC features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because you cannot access the device later. Because all programming, debug, and test interfaces are disabled when device security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

Table 9-1. Debug Configurations

Debug and Trace Configuration	GPIO Pins Used
All debug and trace disabled	0
JTAG	4 or 5
SWD	2
SWV	1
SWD + SWV	3

9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

PSoC 3 has certain timing requirements to be met for entering programming mode through the JTAG interface. Due to these timing requirements, not all standard JTAG programmers, or standard JTAG file formats such as SVF or STAPL, can support PSoC 3 programming. The list of programmers that support PSoC 3 programming is available at <http://www.cypress.com/go/programming>.

The JTAG clock frequency can be up to 14 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as GPIO instead.

9.3 Debug Features

Using the JTAG or SWD interface, the CY8C38 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Eight program address breakpoints
- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C38 compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The CY8C38 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device

erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see "Flash Security" on page 21). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out through the SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

11.2 Device Level Specifications

Specifications are valid for $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 11-2. DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled	1.8	—	5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled	1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled	1.8	—	$V_{DDA}^{[22]}$	V
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled	1.71	1.8	1.89	V
$V_{DDIO}^{[23]}$	I/O supply voltage relative to V_{SSIO}		1.71	—	$V_{DDA}^{[22]}$	V
V_{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled	1.71	1.8	1.89	V
V_{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled	1.71	1.8	1.89	V

Notes

22. $V_{DDX} = 3.3$ V.

23. Based on device specifications (not production tested).

Figure 11-8. SIO Output High Voltage and Current, Unregulated Mode

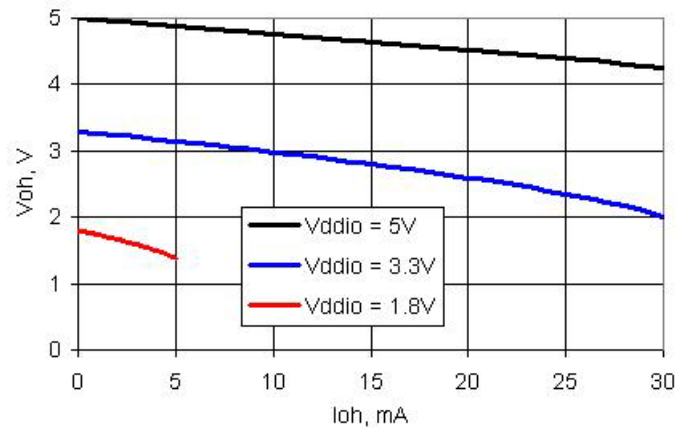


Figure 11-9. SIO Output Low Voltage and Current, Unregulated Mode

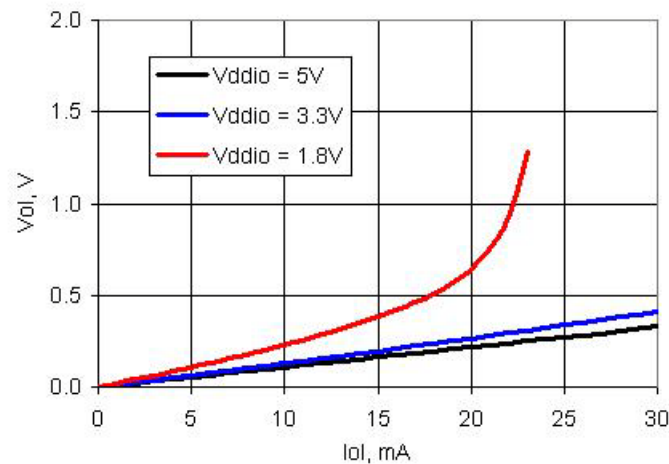
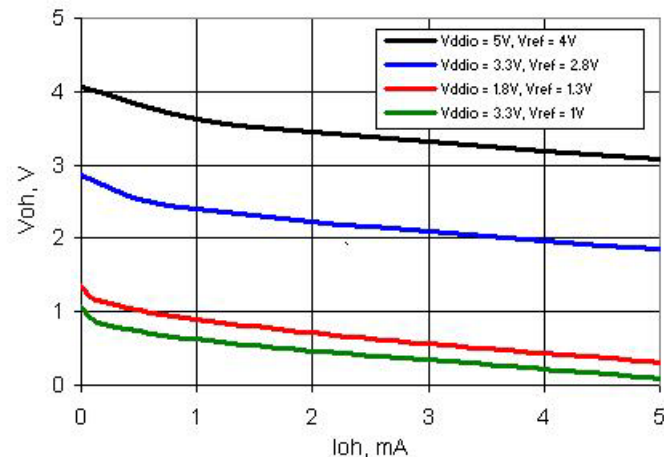


Figure 11-10. SIO Output High Voltage and Current, Regulated Mode



11.5.10 Programmable Gain Amplifier

The PGA is created using a SC/CT Analog Block, see the PGA component data sheet in PSoC Creator for full AC/DC specifications, and APIs and example code.

Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-36. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{in}	Input voltage range	Power mode = minimum	V _{ssa}	–	V _{dda}	V
V _{os}	Input offset voltage	Power mode = high, gain = 1	–	–	10	mV
	Gain Error ^[30]	Non inverting mode, reference = V _{ssa}				
Ge1	Gain = 1	R _{in} of 40K, -40°C ≤ T _a ≤ 85°C and T _j ≤ 100°C	–	–	±0.15	%
		R _{in} of 40K, -40°C ≤ T _a ≤ 125°C and T _j ≤ 150°C	–	–	±0.15	%
Ge16	Gain = 16	R _{in} of 40K, -40°C ≤ T _a ≤ 85°C and T _j ≤ 100°C	–	–	±2.5	%
		R _{in} of 40K, -40°C ≤ T _a ≤ 125°C and T _j ≤ 150°C	–	–	±4	%
Ge50	Gain = 50	R _{in} of 40K, -40°C ≤ T _a ≤ 85°C and T _j ≤ 100°C	–	–	±5	%
		R _{in} of 40K, -40°C ≤ T _a ≤ 125°C and T _j ≤ 150°C	–	–	±6	%
TCV _{os}	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
V _{onl}	DC output nonlinearity	Gain = 1	–	–	±0.01	% of FSR
C _{in}	Input capacitance		–	–	7	pF
V _{oh}	Output voltage swing	Power mode = high, gain = 1, R _{load} = 100 kΩ to V _{DDA} / 2	V _{DDA} – 0.15	–	–	V
V _{ol}	Output voltage swing	Power mode = high, gain = 1, R _{load} = 100 kΩ to V _{DDA} / 2	–	–	V _{SSA} + 0.15	V
V _{src}	Output voltage under load	I _{load} = 250 µA, V _{dda} ≥ 2.7V, power mode = high	–	–	300	mV
I _{dd}	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

11.5.12 LCD Direct Drive

Table 11-39. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 Mhz, Vddio = Vdda = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	μA
I_{CC_SEG}	Current per segment driver	Strong drive mode	–	260	–	μA
V_{BIAS}	LCD bias range (V_{BIAS} refers to the main output voltage(V_0) of LCD DAC)	$V_{DDA} \geq 3 V$ and $V_{DDA} \geq V_{BIAS}$	2	–	5	V
	LCD bias step size	$V_{DDA} \geq 3 V$ and $V_{DDA} \geq V_{BIAS}$	–	$9.1 \times V_{DDA}$	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I_{OUT}	Output drive current per segment driver)	Vddio = 5.5V, strong drive mode	355	–	710	μA

Table 11-40. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LCD}	LCD frame rate		10	50	150	Hz

11.7 Memory

Specifications are valid for $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-55. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	Vddd pin	1.71	-	5.5	V

Table 11-56. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Twrite	Block write time (erase + program)	$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$	-	-	15	ms
		$-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 140^{\circ}\text{C}$	-	-	15	ms
Terase	Block erase time	$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$	-	-	10	ms
		$-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 140^{\circ}\text{C}$	-	-	10	ms
	Block program time	$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$	-	-	5	ms
		$-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 140^{\circ}\text{C}$	-	-	5	ms
			-	-	5	ms
Tbulk	Bulk erase time (16 KB to 64 KB) ^[53]	$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$	-	-	35	ms
		$-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 140^{\circ}\text{C}$	-	-	35	ms
	Sector erase time (8 KB to 16 KB) ^[53]	$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$	-	-	15	ms
		$-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 140^{\circ}\text{C}$	-	-	15	ms
	Total device program time (including JTAG, etc.)	No overhead ^[54]	-	-	5	seconds
	Flash data retention time ^[55]	Average ambient temp. $T_A \leq 55^{\circ}\text{C}$, 100 K erase/program cycles	20	—	—	years
		Retention period measured from last erase cycle after 100k progra/erase cycles at $T_A \leq 85^{\circ}\text{C}$	10	—	—	

Notes

53. ECC not included.

54. See PSoC® 3 Device Programming Specifications for a description of a low-overhead method of programming PSoC 3 flash. (Please take care of Foot note numbers)

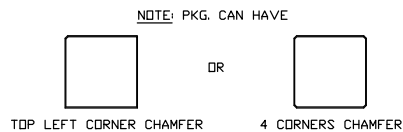
55. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the -40°C to $+125^{\circ}\text{C}$ ambient temperature range. Contact customer care@cypress.com.



The technical drawing illustrates a square microchip package with the following specifications:

- Top View Dimensions:**
 - Total width: 16.00 ± 0.25
 - Inner width: 14.00 ± 0.05
 - Pin pitch (horizontal): 0.39 ± 0.05
 - Pin pitch (vertical): 0.39 ± 0.05
 - Lead thickness: 0.08
 - Lead height at corners: 0.75
 - Seating plane offset: 0.25
 - Bottom lead length: 0.50
 - Right-side lead length: 0.51
 - Right-side pin pitch: 0.22 ± 0.05
 - Right-side lead angle: 0.50° TYP.
- Side View Dimensions:**
 - Package height: 1.60 MAX.
 - Lead thickness: 0.08
 - Lead height: 0.20 MAX.
 - Lead angle: $12^\circ \pm 1^\circ$ (BX)
 - Bottom lead length: 1.40 ± 0.05
- Labels:**
 - SEATING PLANE
 - SFF DETAIL A

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



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17. Revision History

Description Title: PSoC® 3: CY8C38 Automotive Family Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 001-54683				
Rev.	ECN	Submission Date	Orig. of Change	Description of Change
**	2742918	07/23/09	VIVG / PYRS	New data sheet for PSoC 3 Automotive
*A	2750090	08/10/09	SHEA	Minor ECN to correct title on first page
*B	2800070	01/05/10	SECA	Added Tio_init parameter and updated Tstartup values. Updated PGA and UGB AC Specs table and changed gain error condition in PGA DC table. Added PCB Layout and PCB Schematic figures. Updated Figure 1-1 and Figure 8-1 . Removed 12-Bit Del-Sig ADC table.
*C	2921624	04/26/2010	MKEA	Updated Active Mode Idd values in Table 11-2 Updated Boost AC and DC specifications Updated solder paste reflow temperature (Table 11-3) Moved Filo spec from ILO DC to ILO AC table Updated Figure 7-14, Interrupt and DMA processing Added Bytes column in Tables 4-1 and 4-5 Updated Figure 6-3, Power mode transitions Updated JTAG and SWD specifications Updated Interrupt Vector table Updated Sales links Updated PCB Schematic Updated Vbias spec Added UDBs subsection under 11.6 Digital Peripherals Updated Iout parameter in LCD Direct Drive DC Specs table Added footnote in PLL AC Specification table Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table Updated Icc parameter in LCD Direct Drive DC Specs table Updated Tstartup parameter in AC Specifications table Updated LVD in Tables 6-2 and 6-3 In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9 Added PLL intermediate frequency row with footnote in PLL AC Specs table Added bullets on CapSense in page 1; added CapSense column in Section Updated Figure 2-6 (PCB Layout) Updated Tstartup values in Table 11-3 Updated IMO frequency Updated section 5.2 and Table 11-2 to correct suggestion of execution from Flash Updated Vref specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Tresp, high and low power modes, in Table 11-24. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table 72. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Updated SNR condition in Table 11-20
*D	3490311	01/11/2012	GIR	Updated Figure 6-7 .
*E	3648803	06/18/2012	WKA / MKEA	No changes. EROS update. Updated 100-Pin TQFP package outline spec 51-85048 from *E to *G revision.
*F	3732521	09/03/2012	MKEA	Updated package diagram 51-85061 to *F revision.
*G	3994809	05/08/2013	KPAT	Updated all tables in Electrical Specifications . Updated Ordering Information (Updated part numbers, JTAG ID). Removed all references of Vboost across the document.