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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3846axe-176

It also contains a separate, very low-power internal low-speed oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in real-time clock (RTC) applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C38 family supports a wide supply operating range from 1.71 V to 5.5 V. This allows operation from regulated supplies such as 1.8 V ± 5%, 2.5 V ±10%, 3.3 V ± 10%, or 5.0 V ± 10%, or directly from a wide range of battery types.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1-µA sleep mode with RTC. In the second mode, the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 29 of this data sheet.

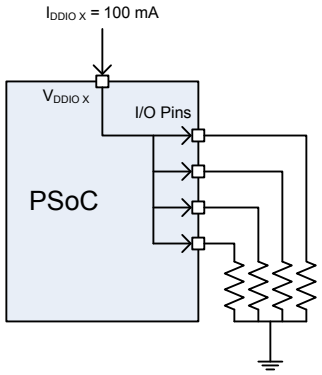
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for 'printf' style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces you can debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 60 of this data sheet.

2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-4 show the pins that are powered by each VDDIO.

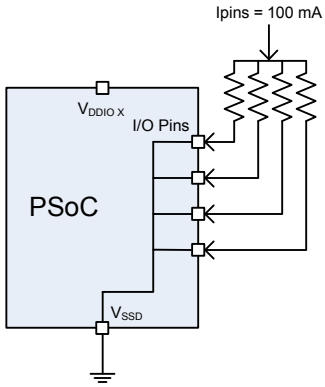
Each VDDIO may source up to 100 mA [8] total to its associated I/O pins, as shown in Figure 2-1.

Figure 2-1. VDDIO Current Limit



Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA [8] total, as shown in Figure 2-2.

Figure 2-2. I/O Pins Current Limit



For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA [8] total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.

Note
8. The 100 mA source/ sink current per Vddio is valid only for temperature range of –40 °C to +85 °C. For extended temperature range of –40 °C to +125 °C, the maximum source or sink current per Vddio is 40 mA.

Figure 2-4. 100-pin TQFP Part Pinout

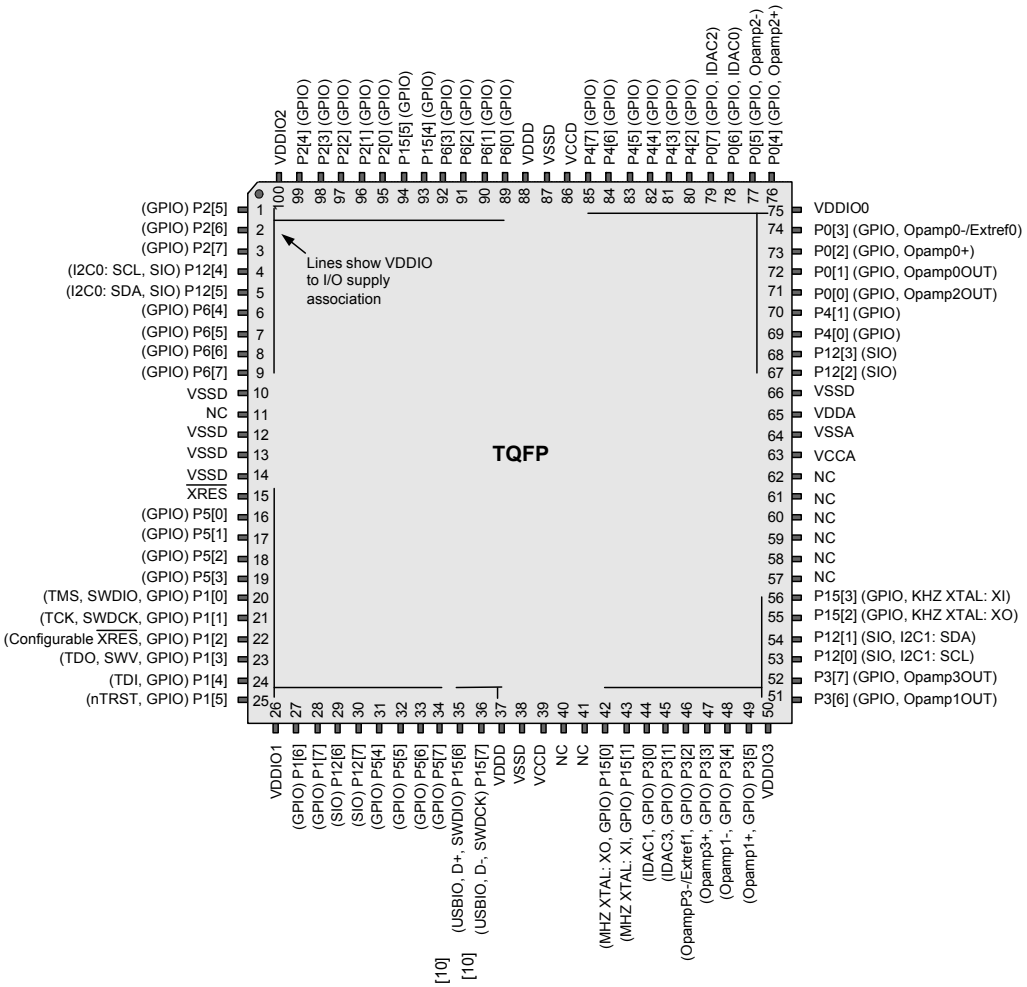


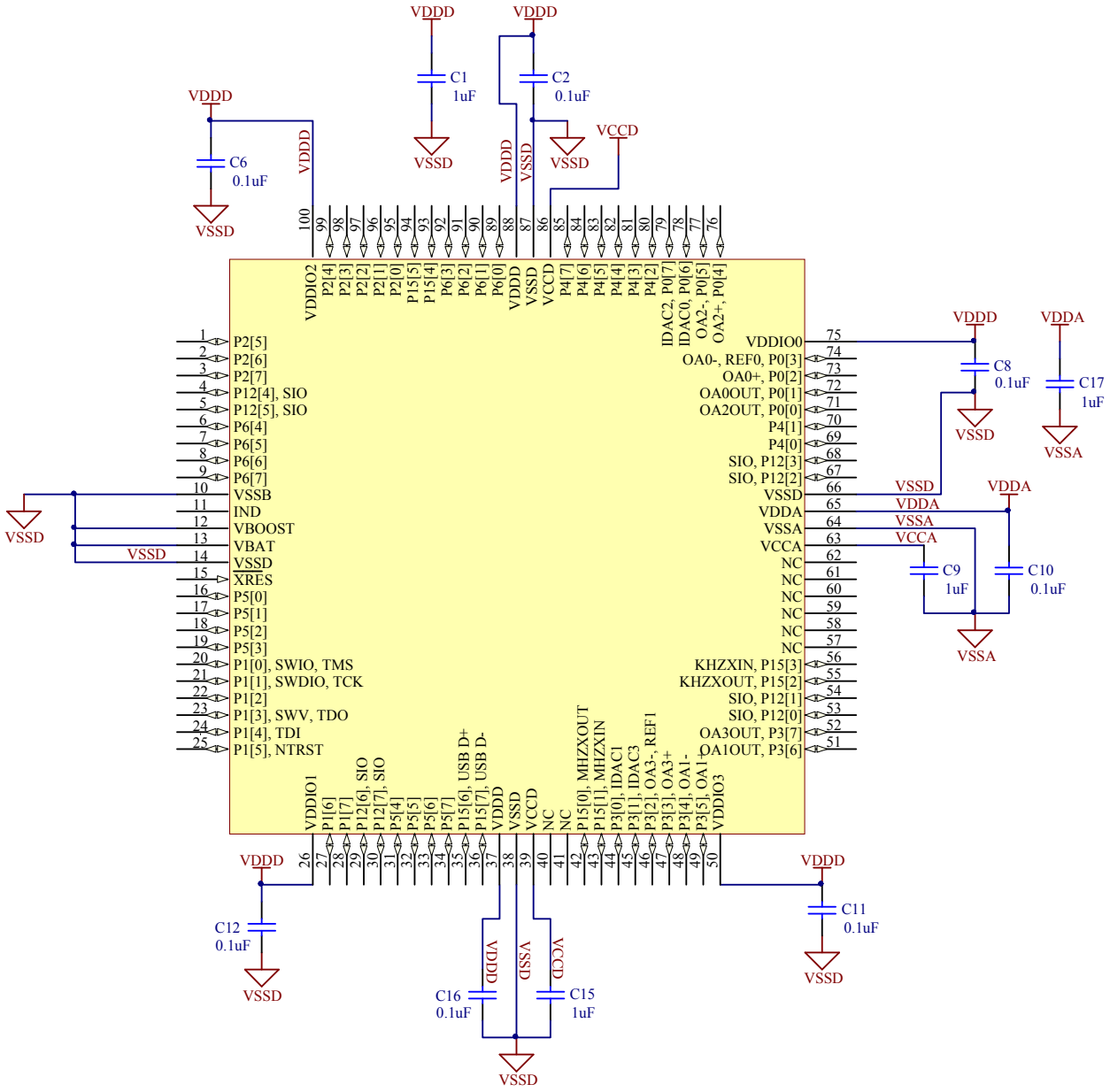
Figure 2-5 and Figure 2-6 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-5 and Power System on page 29. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled Vssd must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note, AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

Note
10. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 2-5. Example Schematic for 100-pin TQFP Part with Power Connections



Note The two Vccd pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6 on page 9.

■ Program branching instructions

4.3.1 Instruction Set Summary

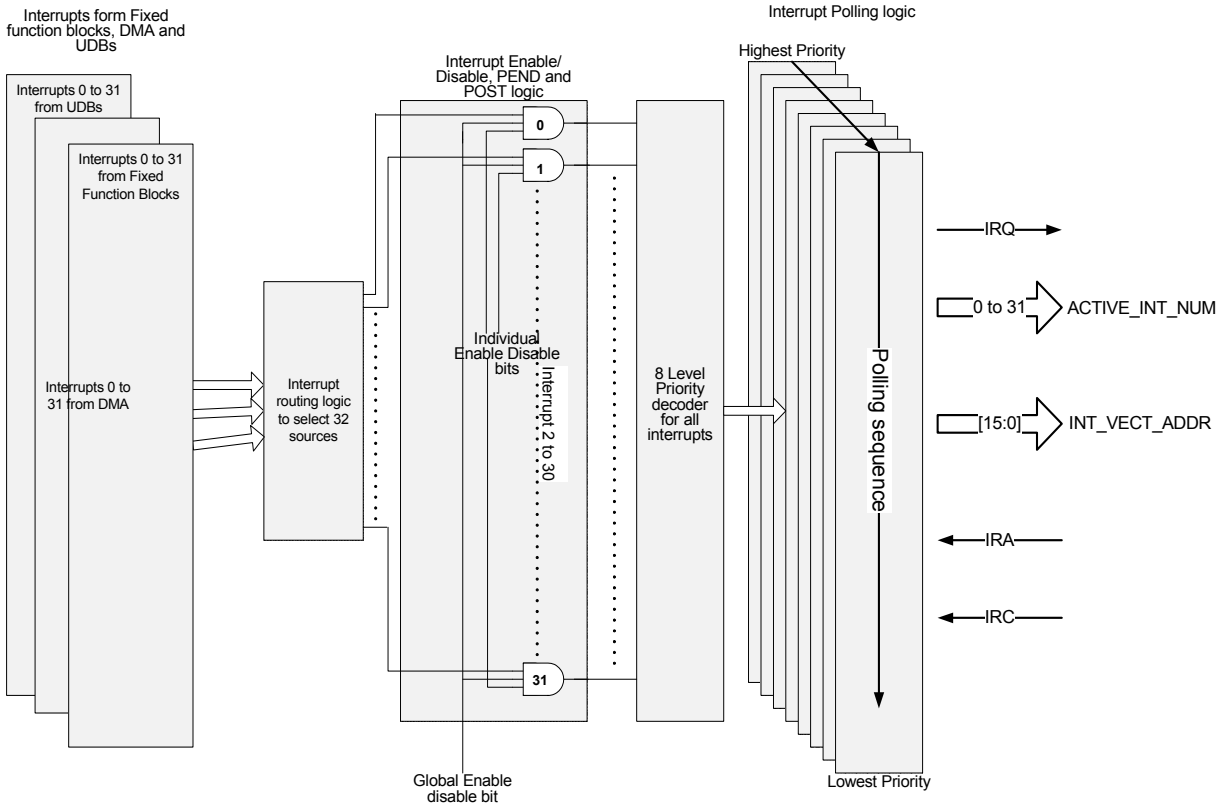
4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. Table 4-1 lists the different arithmetic instructions.

Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

Figure 4-3. Interrupt Structure



When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I^2C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	DFB Int	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-5. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-10 depicts a simplified pin view based on each of the eight drive modes. Table 6-5 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-10. Drive Mode

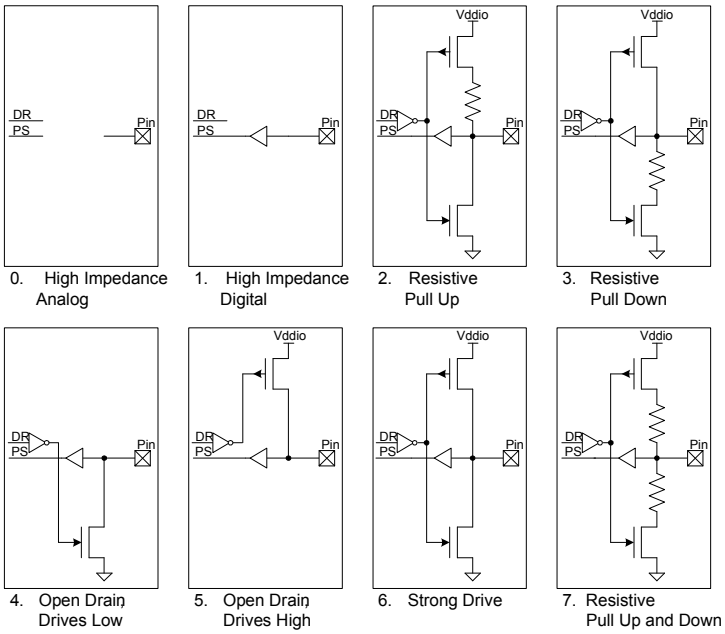


Table 6-5. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedance analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up[14]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down[14]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down[14]	1	1	1	Res High (5K)	Res Low (5K)

Note
14. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

8.3.2 LUT

The CY8C38 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

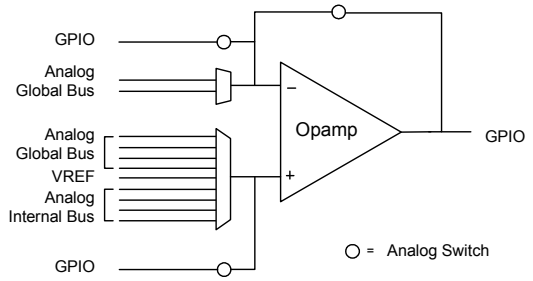
Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** (‘0’)
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** (‘1’)

8.4 Opamps

The CY8C38 family of devices contain up to four general purpose opamps in a device.

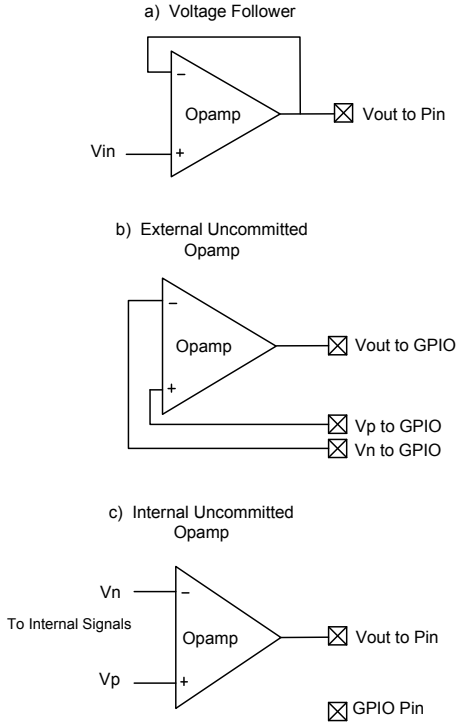
Figure 8-6. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-7. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-7. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

The CY8C38 family of devices contains up to four switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

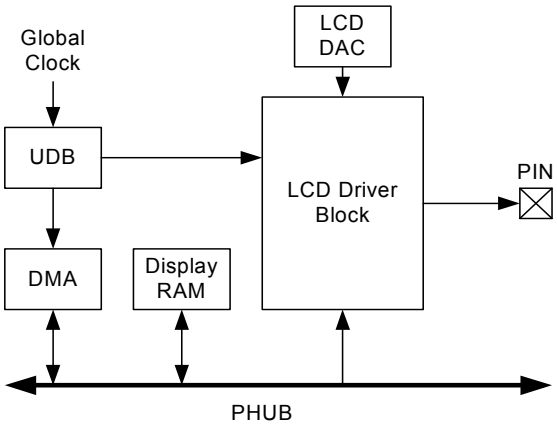
The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-10. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers through the DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.8 Temp Sensor

Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Idd[24, 25]	**Active Mode, VDD = 1.71 V - 5.5 V**					
	Execute from CPU instruction buffer, see Flash Program Memory on page 21					
	CPU at 3 MHz	T = –40 °C	–	1.3	2.9	mA
		T = 25 °C	–	1.6	3.2	mA
		T = 85 °C	–	4.8	7.5	mA
		T = 125 °C	–	4.9	7.7	mA
	CPU at 6 MHz	T = –40 °C	–	2.1	3.7	mA
		T = 25 °C	–	2.3	3.9	mA
		T = 85 °C	–	5.6	8.5	mA
		T = 125 °C	–	5.8	8.7	mA
	CPU at 12 MHz	T = –40 °C	–	3.5	5.2	mA
		T = 25 °C	–	3.8	5.5	mA
		T = 85 °C	–	7.1	9.8	mA
		T = 125 °C	–	9.0	10	mA
	CPU at 24 MHz	T = –40 °C	–	6.3	8.1	mA
		T = 25 °C	–	6.6	8.3	mA
		T = 85 °C	–	10	13	mA
		T = 125 °C	–	12	14	mA
	CPU at 48 MHz	T = –40 °C	–	11.5	13.5	mA
		T = 25 °C	–	12	14	mA
		T = 85 °C	–	15.5	18.5	mA
		T = 125 °C	–	16.5	19	mA
	CPU at 62 MHz	T = –40 °C	–	16	18	mA
		T = 25 °C	–	16	18	mA
		T = 85 °C	–	19.5	23	mA
		T = 125 °C	–	20	24	mA

Notes
24. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective data sheets, available in PSoC Creator, the integrated design environment. To compute total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device data sheet and component data sheets.
25. Total current for all power domains: digital (I_{DDD}), analog (I_{DDA}), and I/Os ($I_{DDIO0, 1, 2, 3}$). All I/Os floating.

11.4 Inputs and Outputs

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.4.1 GPIO

Table 11-6. GPIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vih	Input voltage high threshold	CMOS Input, PRT[x]CTL = 0	0.7 × Vddio	-	-	V
Vil	Input voltage low threshold	CMOS Input, PRT[x]CTL = 0	-	-	0.3 × Vddio	V
Vih	Input voltage high threshold	LVTTL Input, PRT[x]CTL = 1,Vddio < 2.7 V	0.7 x Vddio	-	-	V
Vih	Input voltage high threshold	LVTTL Input, PRT[x]CTL = 1, Vddio ≥ 2.7V	2.0	-	-	V
Vil	Input voltage low threshold	LVTTL Input, PRT[x]CTL = 1,Vddio < 2.7 V	-	-	0.3 x Vddio	V
Vil	Input voltage low threshold	LVTTL Input, PRT[x]CTL = 1, Vddio ≥ 2.7V	-	-	0.8	V
Voh	Output voltage high	Ioh = 4 mA at 3.3 Vddio	Vddio - 0.6	-	-	V
		Ioh = 1 mA at 1.8 Vddio	Vddio - 0.5	-	-	V
Vol	Output voltage low	Iol = 6 mA at 3.3 Vddio	–	–	0.6	V
		Iol = 3 mA at 1.8 Vddio	–	–	0.6	V
		Iol = 3 mA at 3.3 Vddio	–	–	0.4	V
Rpullup	Pull up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull down resistor		3.5	5.6	8.5	kΩ
Iil	Input leakage current (absolute value)[31]	25°C, Vddio = 3.0 V	-	-	2	nA
C_{IN}	Input capacitance[31]	GPIOs not shared with opamp outputs, MHz ECO or kHzECO	–	4	7	pF
		GPIOs shared with MHz ECO or kHzECO[32]	–	5	7	pF
		GPIOs shared with opamp outputs	–	–	18	pF
Vh	Input voltage hysteresis (Schmitt-Trigger)[31]		-	40	-	mV
Idiode	Current through protection diode to Vddio and Vssio		-	-	100	µA
Rglobal	Resistance pin to analog global bus	25°C, Vddio = 3.0 V	–	320	–	Ω
Rmux	Resistance pin to analog mux bus	25°C, Vddio = 3.0 V	–	220	–	Ω

Notes
31. Based on device characterization (Not production tested).
32. For information on designing with PSoC 3 oscillators, refer to the application note, AN54439 - PSoC® 3 and PSoC 5 External Oscillator.

11.4.3 USBIO

Table 11-10. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull up resistance	With idle bus	0.900	-	1.575	kΩ
Rusba	USB D+ pull up resistance	While receiving traffic	1.425	-	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to Vss, internal pull up enabled	2.8	-	3.6	V
Volusb	Static output low	15 kΩ ±5% to Vss, internal pull up enabled	-	-	0.3	V
Vihgpio	Input voltage high, GPIO mode	$V_{DDD} \geq 3$ V	2	–	–	V
Vilgpio	Input voltage low, GPIO mode	$V_{DDD} \geq 3$ V	–	–	0.8	V
Vohgpio	Output voltage high, GPIO mode	Ioh = 4 mA, Vddio ≥ 3 V	2.4	-	-	V
Volgpio	Output voltage low, GPIO mode	Iol = 4 mA, Vddio ≥ 3 V	-	-	0.3	V
Vdi	Differential input sensitivity	|(D+)-(D-)|	-	-	0.2	V
Vcm	Differential input common mode range		0.8	-	2.5	V
Vse	Single ended receiver threshold		0.8	-	2	V
Rps2	PS/2 pull up resistance	In PS/2 mode, with PS/2 pull up enabled	3	-	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (-1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	28	-	44	Ω
		Including Rext, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	28	-	46	Ω
Cin	USB transceiver input capacitance		-	-	20	pF
Iil [35]	Input leakage current (absolute value)	25°C, Vddio = 3.0 V	-	-	2	nA

Note
35. Based on device characterization (not production tested).

11.5.3 Voltage Reference

Table 11-24. Voltage Reference Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vref [39]	Precision reference	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	1.021 (-0.3%)	1.024	1.027 (+0.3%)	V
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	1.018 (–0.6%)	1.024	1.030 (+0.6%)	V
	After typical PCB assembly, post reflow	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance.				
		–40 °C		±0.5		%
		25 °C		±0.2		%
		85 °C		±0.2		%
	Temperature drift[40]	Box method	–	–	30	ppm/°C
	Long term drift		–	100	–	ppm/khr
	Thermal cycling drift (stability)[40, 41]		–	100	–	ppm

Figure 11-30. Voltage Reference vs. Temperature and V_{CCA}

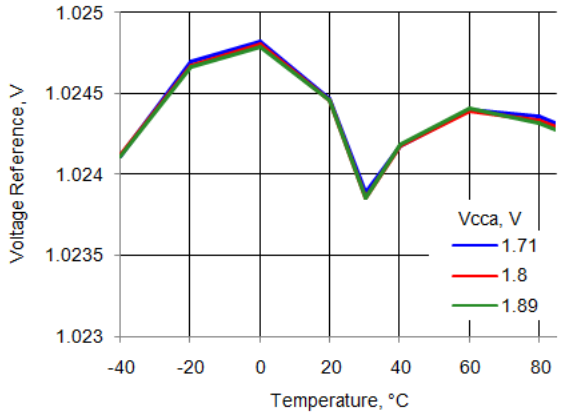
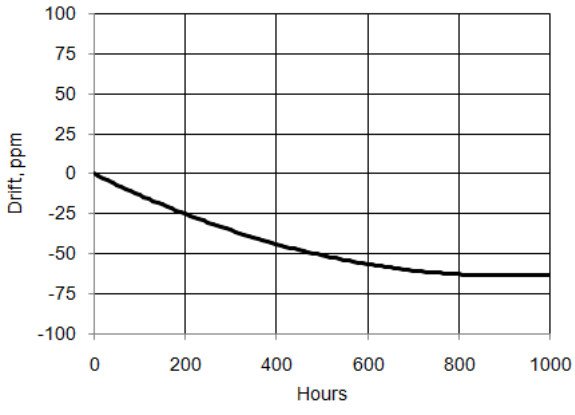


Figure 11-31. Voltage Reference Long-Term Drift



Notes
39. V_{REF} is measured after packaging, and thus accounts for substrate and die attach stresses.
40. Based on device characterization (Not production tested).
41. After eight full cycles between –40 °C and 100 °C.

Figure 11-39. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

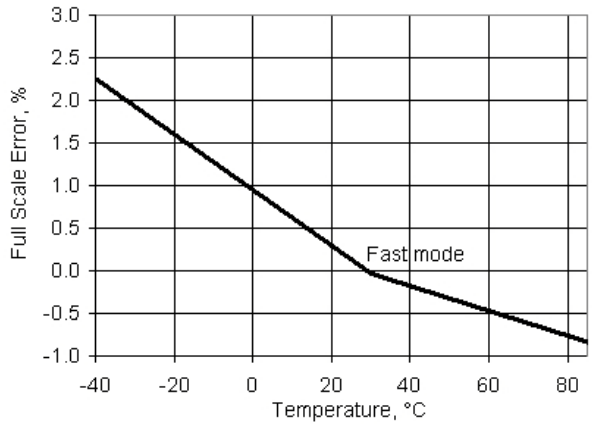


Figure 11-40. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

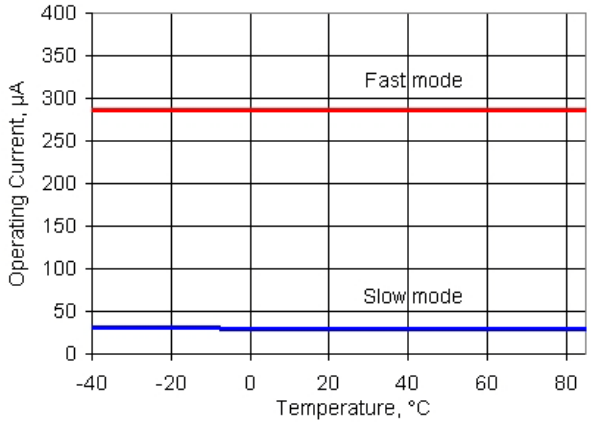


Figure 11-41. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

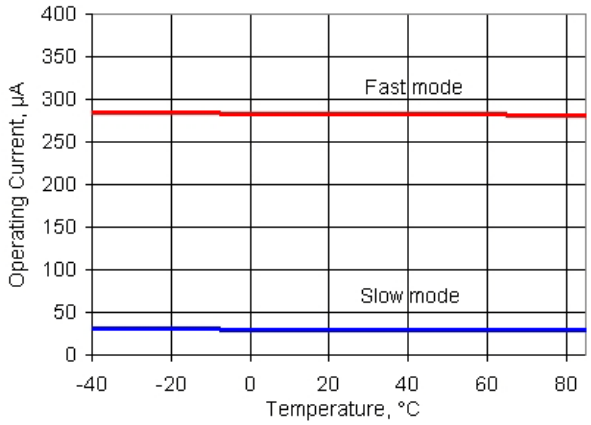
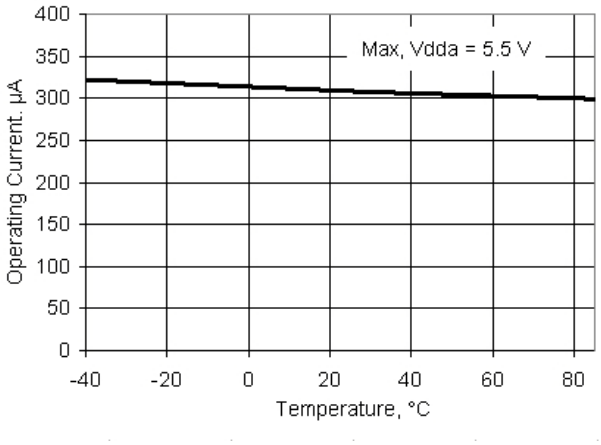


Figure 11-53. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode



11.5.10 Programmable Gain Amplifier

The PGA is created using a SC/CT Analog Block, see the PGA component data sheet in PSoC Creator for full AC/DC specifications, and APIs and example code.

Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-36. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vin	Input voltage range	Power mode = minimum	Vssa	–	Vdda	V
Vos	Input offset voltage	Power mode = high, gain = 1	–	–	10	mV
	Gain Error[30]	Non inverting mode, reference = Vssa				
Ge1	Gain = 1	Rin of 40K, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	–	–	±0.15	%
		Rin of 40K, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	–	–	±0.15	%
Ge16	Gain = 16	Rin of 40K, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	–	–	±2.5	%
		Rin of 40K, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	–	–	±4	%
Ge50	Gain = 50	Rin of 40K, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	–	–	±5	%
		Rin of 40K, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	–	–	±6	%
TCVos	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Vonl	DC output nonlinearity	Gain = 1	–	–	±0.01	% of FSR
Cin	Input capacitance		–	–	7	pF
Voh	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	V_{DDA} – 0.15	–	–	V
Vol	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	–	–	V_{SSA} + 0.15	V
Vsrc	Output voltage under load	Iload = 250 µA, Vdda ≥ 2.7V, power mode = high	–	–	300	mV
Idd	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

11.5.12 LCD Direct Drive

Table 11-39. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 Mhz, Vddio = Vdda = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	µA
I_{CC_SEG}	Current per segment driver	Strong drive mode	–	260	–	µA
V_{BIAS}	LCD bias range (V_{BIAS} refers to the main output voltage(V0) of LCD DAC)	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	2	–	5	V
	LCD bias step size	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	–	9.1 × V_{DDA}	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I_{OUT}	Output drive current per segment driver)	Vddio = 5.5V, strong drive mode	355	–	710	µA

Table 11-40. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LCD}	LCD frame rate		10	50	150	Hz

11.7 Memory

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-55. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	Vddd pin	1.71	-	5.5	V

Table 11-56. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Twrite	Block write time (erase + program)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	15	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	15	ms
Terase	Block erase time	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	10	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	10	ms
	Block program time	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	5	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	5	ms
Tbulk	Bulk erase time (16 KB to 64 KB)[53]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	35	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	35	ms
	Sector erase time (8 KB to 16 KB)[53]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	15	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	15	ms
	Total device program time (including JTAG, etc.)	No overhead [54]	-	-	5	seconds
	Flash data retention time [55]	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Retention period measured from last erase cycle after 100k progra/erase cycles at T_A ≤ 85 °C	10	–	–	

Notes
53. ECC not included.
54. See PSoC® 3 Device Programming Specifications for a description of a low-overhead method of programming PSoC 3 flash. (Please take care of Foot note numbers)
55. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +125 °C ambient temperature range. Contact customercare@cypress.com.

14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier

17. Revision History *(continued)*

Description Title: PSoC® 3: CY8C38 Automotive Family Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 001-54683				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*H (cont.)	4094193	08/30/2013	NFB / ANMD	Updated Electrical Specifications: Updated Device Level Specifications: Updated Table 11-2. Updated Table 11-3. Updated Inputs and Outputs: Updated GPIO: Updated Table 11-7. Removed figure “GPIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load” and figure “GPIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load”. Updated Analog Peripherals: Updated Delta-Sigma ADC: Updated Table 11-17. Updated Table 11-18. Updated Voltage Reference: Updated Table 11-24. Updated IDAC: Updated Table 11-28. Updated Memory: Updated Flash: Updated Table 11-56. Updated Clocking: Updated Internal Main Oscillator: Updated Table 11-76. Updated Packaging: spec 51-85048 – Changed revision from *G to *H. Updated in new template. Completing Sunset Review.
*I	4174912	10/26/2013	NFB / ANMD	Updated Pinouts: Added Note 8 and referred the same note in 100 mA in description. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 11-1. Added Note 18 and referred the same note in Table 11-1. Added Note 20 and referred the same note in Ivddio parameter in Table 11-1. Updated Device Level Specifications: Updated Table 11-2. Updated Analog Peripherals: Updated Opamp: Updated Table 11-15. Updated Voltage Reference: Updated Table 11-24. Updated Packaging: Updated Table 13-1.
*J	4188568	11/14/2013	WKA	No content update.