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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3865pva-063

Contents

■ Program branching instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. Table 4-1 lists the different arithmetic instructions.

Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

4.3.1.2 Logical Instructions

The logical instructions perform Boolean operations such as AND, OR, XOR on bytes, rotate of accumulator contents, and swap of nibbles in an accumulator. The Boolean operations on the bytes are performed on the bit-by-bit basis. Table 4-2 shows the list of logical instructions and their description.

Table 4-2. Logical Instructions

Mnemonic	Description	Bytes	Cycles
ANL A,Rn	AND register to accumulator	1	1
ANL A,Direct	AND direct byte to accumulator	2	2
ANL A,@Ri	AND indirect RAM to accumulator	1	2
ANL A,#data	AND immediate data to accumulator	2	2
ANL Direct, A	AND accumulator to direct byte	2	3
ANL Direct, #data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to accumulator	1	1
ORL A,Direct	OR direct byte to accumulator	2	2
ORL A,@Ri	OR indirect RAM to accumulator	1	2
ORL A,#data	OR immediate data to accumulator	2	2
ORL Direct, A	OR accumulator to direct byte	2	3
ORL Direct, #data	OR immediate data to direct byte	3	3
XRL A,Rn	XOR register to accumulator	1	1
XRL A,Direct	XOR direct byte to accumulator	2	2
XRL A,@Ri	XOR indirect RAM to accumulator	1	2
XRL A,#data	XOR immediate data to accumulator	2	2
XRL Direct, A	XOR accumulator to direct byte	2	3
XRL Direct, #data	XOR immediate data to direct byte	3	3
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right though carry	1	1
SWAP A	Swap nibbles within accumulator	1	1

4.3.1.3 Data Transfer Instructions

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed addressing mode. Table 4-3 lists the various data transfer instructions available.

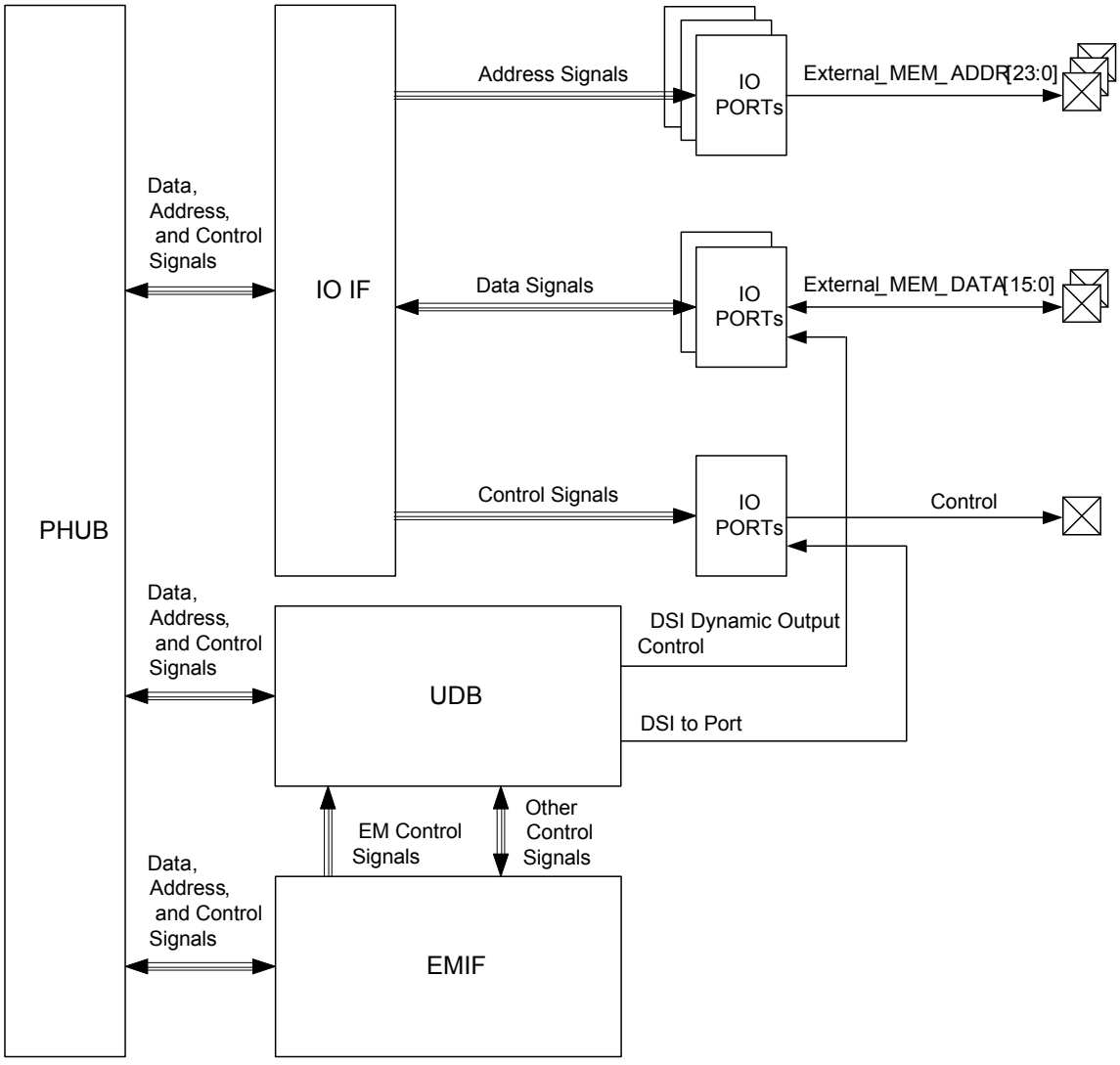
4.3.1.4 Boolean Instructions

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. Table 4-4 lists the available Boolean instructions.

5.6 External Memory Interface

CY8C38 provides an EMIF for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles. Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C38 supports only one type of external memory device at a time. External memory can be accessed through the 8051 xdata space; up to 24 address bits can be used. See "xdata Space" section on page 25. The memory can be 8 or 16 bits wide.

Figure 5-1. EMIF Block Diagram



6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to '1' and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt. While level sensitive interrupts are not directly supported; UDB provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip's analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin. The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[15]. See the "CapSense" section on page 58 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the "LCD Direct Drive" section on page 57 for details.

6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO's respective VDDIO. SIO pins are individually configurable to output either the standard VDDIO level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see Figure 6-11). The "DAC" section on page 59 has more details on VDAC use and reference routing to the SIO pins. Resistive pullup and pull-down drive modes are not available with SIO in regulated output mode.

6.4.12 Adjustable Input Level

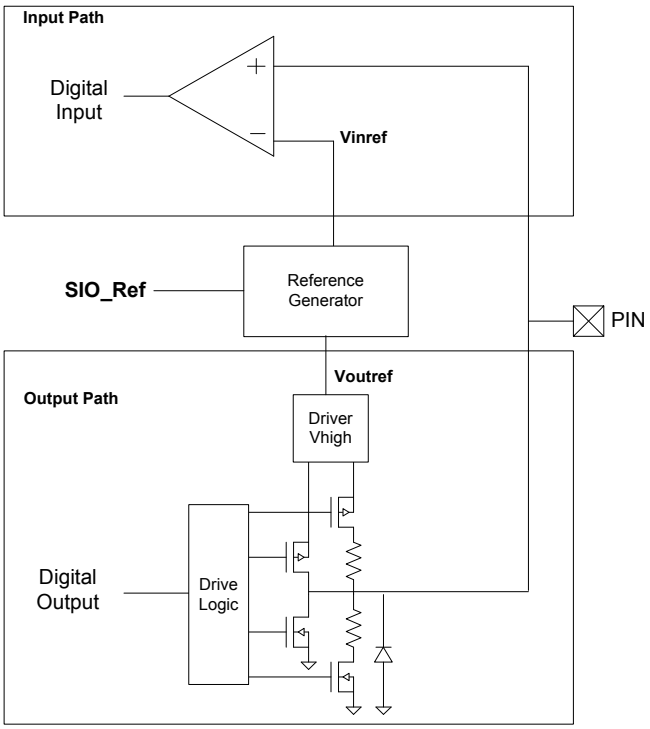
This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see Figure 6-11). Available input thresholds are:

- 0.5 × VDDIO
- 0.4 × VDDIO
- 0.5 × V_{REF}
- V_{REF}

Typically a voltage DAC (VDAC) generates the V_{REF} reference. "DAC" section on page 59 has more details on VDAC use and reference routing to the SIO pins.

Note
15. GPIOs with opamp outputs are not recommended for use with CapSense.

Figure 6-11. SIO Reference for Input and Output



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the Adjustable Input Level section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold. The digital input path in Figure 6-8 on page 35 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I2C bus may cause transient states on the SIO pins. The overall I2C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating V_{DD}.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where VDDIO $\leq V_{IN} \leq$ 5.5 V.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply where VDDIO $\leq V_{IN} \leq$ VDDA.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated VDDIO supply pin. The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See Figure 6-10 for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in Pinouts on page 5. The special features are:

- Digital
  - 4- to 25-MHz crystal oscillator
  - 32.768-kHz crystal oscillator
  - Wake from sleep on I^2C address match. Any pin can be used for I^2C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

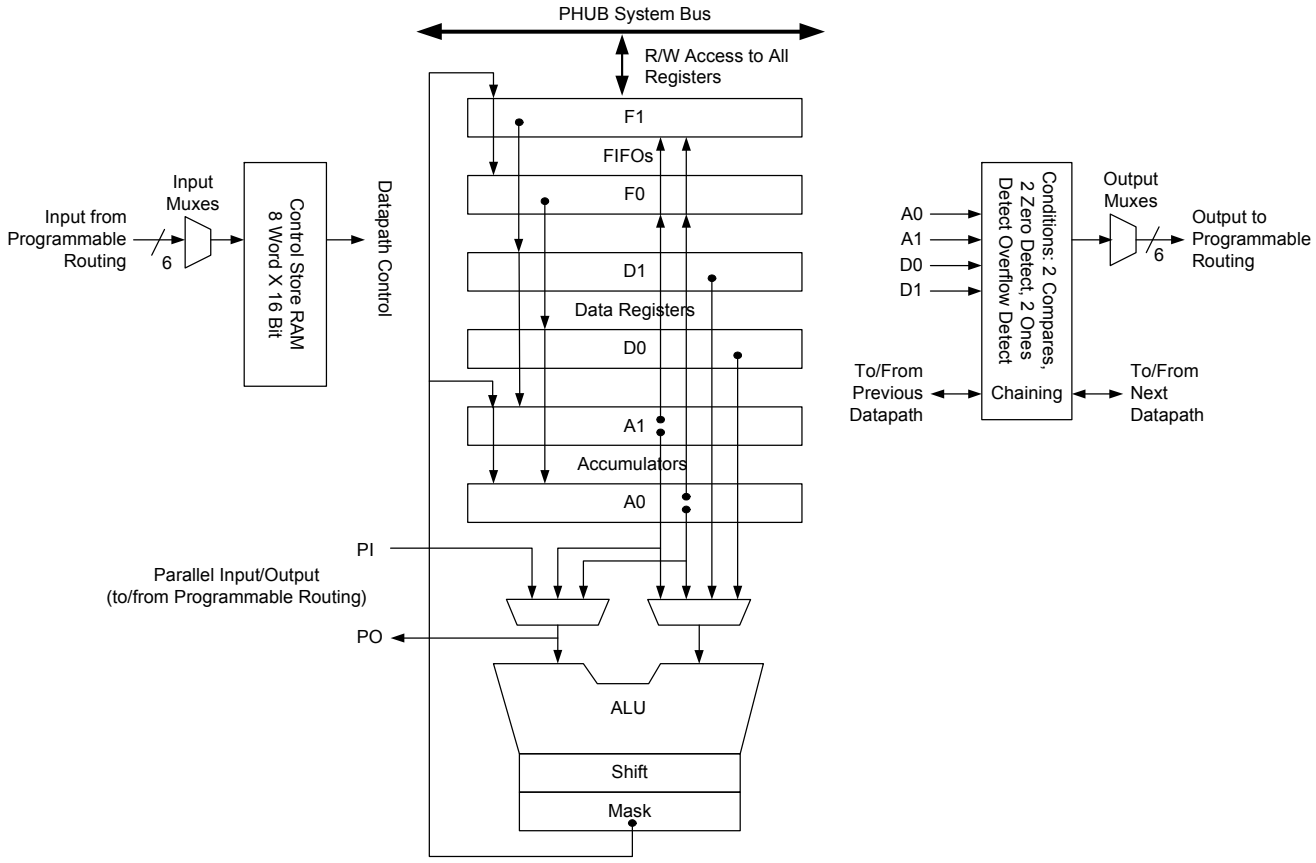
6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Datapath Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

8.2.2.4 Multi Sample (Turbo)

The multi sample (turbo) mode operates identical to the Multi-sample mode for resolutions of 8 to 16 bits. For resolutions of 17 to 20 bits, the performance is about four times faster than the multi sample mode, because the ADC is only reset once at the end of conversion.

More information on output formats is provided in the Technical Reference Manual.

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

8.3 Comparators

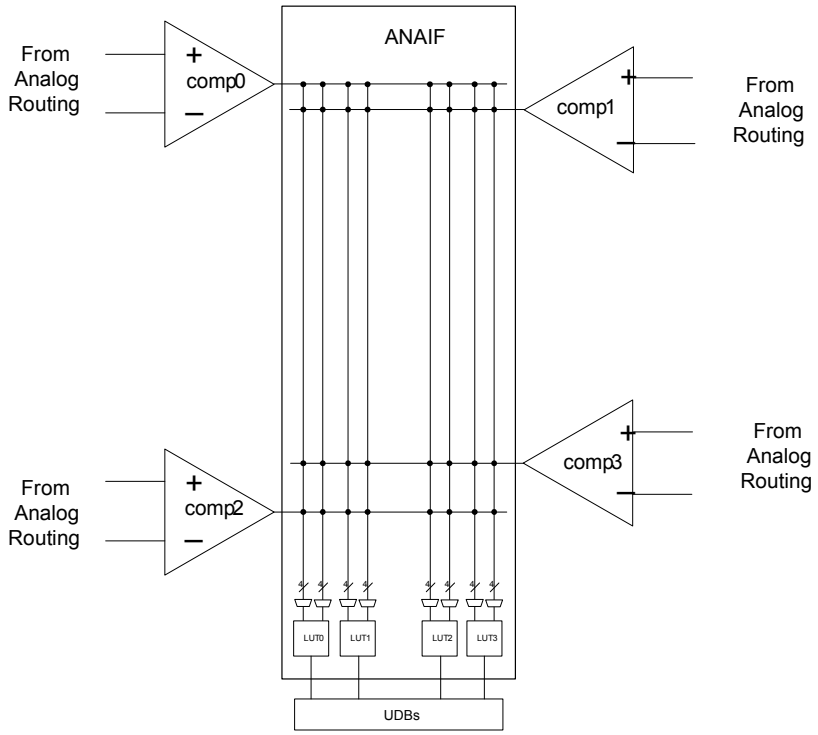
The CY8C38 family of devices contains four comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (VSSA to VDDA)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB DSI.

Figure 8-5. Analog Comparator



The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

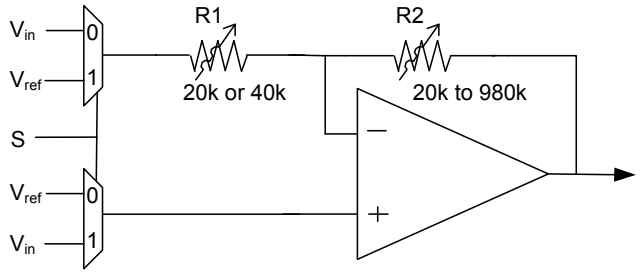
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8. The schematic in Figure 8-8 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	5.5 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-8. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

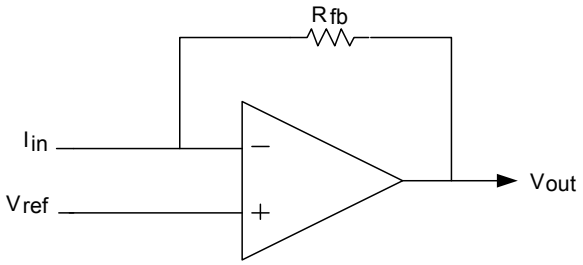
8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-9. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C38 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vdda	Input voltage		1.8	-	5.5	V
Vcca	Output voltage		-	1.80	-	V
	Regulator output capacitor	±10%, X5R ceramic or better (X7R for Ta > 85°C)	-	1	-	µF

Figure 11-5. Analog Regulator PSRR vs Frequency and V_{DD}

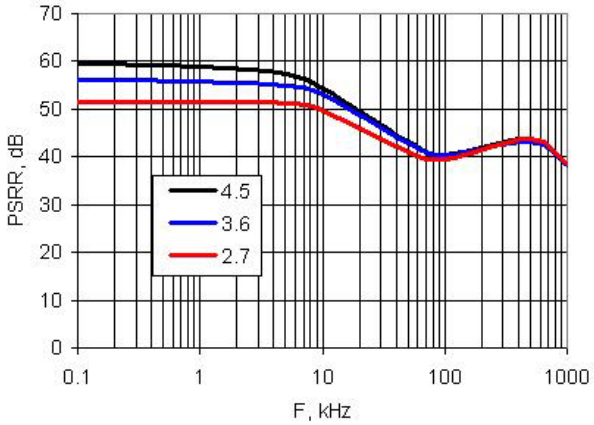


Table 11-9. SIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%)[30]	Cload = 25 pF, Vddio = 3.3 V	–	–	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%)[30]	Cload = 25 pF, Vddio = 3.3 V	–	–	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%)[30]	Cload = 25 pF, Vddio = 3.0 V	–	–	80	ns
TfallS	Fall time in Slow Strong Mode (90/10%)[30]	Cload = 25 pF, Vddio = 3.0 V	–	–	70	ns
Fsioout	SIO output operating frequency					
	3.3 V < Vddio < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	33	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	24	MHz
	1.71 V < Vddio < 3.3 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% Vddio into 25 pF	-	-	16	MHz
	3.3 V < Vddio < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% Vddio into 25 pF	-	-	5	MHz
	1.71 V < Vddio < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% Vddio into 25 pF	-	-	4	MHz
	3.3 V < Vddio < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	-	-	20	MHz
	1.71 V < Vddio < 3.3 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	-	-	10	MHz
	1.71 V < Vddio < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	-	-	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ Vddio ≤ 5.5 V	90/10% better than 60/40 duty cycle, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	66	MHz
		90/10% better than 60/40 duty cycle, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	50	MHz

Table 11-11. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 - 0.25%	12	12 + 0.25%	MHz
Tdjr1	Receiver data jitter tolerance to next transition		-8	-	8	ns
Tdjr2	Receiver data jitter tolerance to pair transition		-5	-	5	ns
Tudj1	Driver differential jitter to next transition		-3.5	-	3.5	ns
Tudj2	Driver differential jitter to pair transition		-4	-	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		-2	-	5	ns
Tfeopt	Source SE0 interval of EOP		160	-	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	-	-	ns
Tfst	Width of SE0 interval during differential transition		-	-	14	ns
Fgpio_out	GPIO mode output operating frequency	3 V ≤ Vddd ≤ 5.5 V	-	-	20	MHz
		Vddd = 1.71 V	-	-	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% Vddd	Vddd > 3 V, 25 pF load	–	–	12	ns
		Vddd = 1.71 V, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% Vddd	Vddd > 3 V, 25 pF load	–	–	12	ns
		Vddd = 1.71 V, 25 pF load	–	–	40	ns

Figure 11-15. USBIO Output Rise and Fall Times, GPIO Mode, V_{DDD} = 3.3 V, 25 pF Load

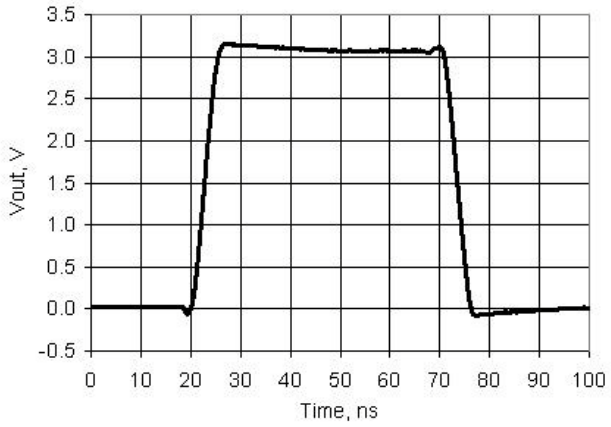


Table 11-12. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	VUSB_5, VUSB_3.3, see	90%	-	111%	
Vcrs	Output signal crossover voltage		1.3	-	2	V

Figure 11-50. VDAC Full Scale Error vs Temperature, 1 V Mode

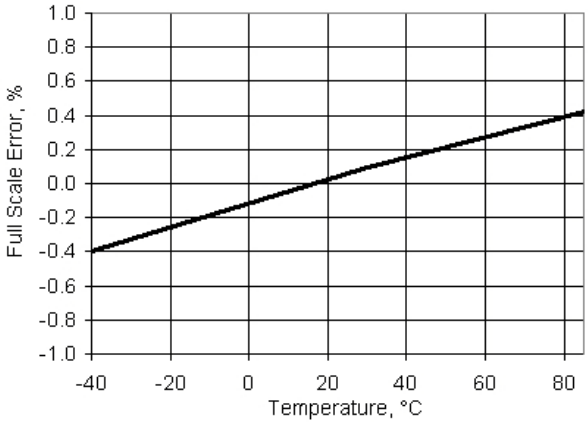


Figure 11-51. VDAC Full Scale Error vs Temperature, 4 V Mode

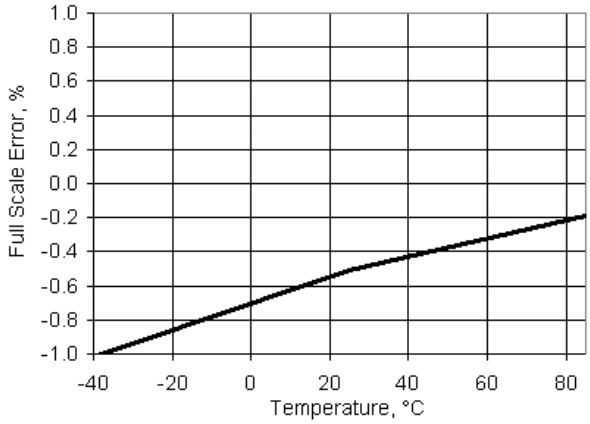
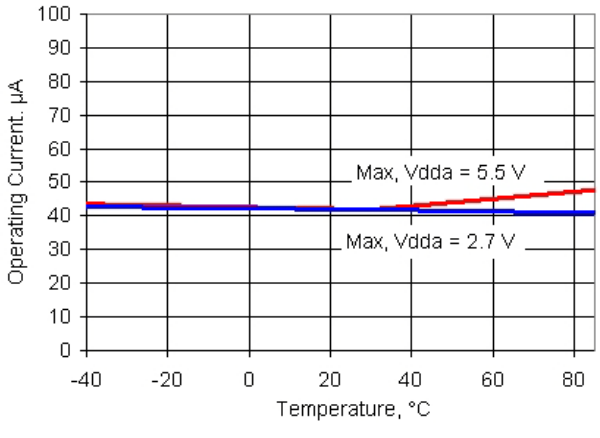


Figure 11-52. VDAC Operating Current vs Temperature, 1V Mode, Low speed mode



11.7.2 EEPROM

Table 11-57. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	-	5.5	V

Table 11-58. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	2	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, $T_A \leq 25$ °C, 1M erase/program cycles	20	–	–	years
		Average ambient temp, $T_A \leq 55$ °C, 100 K erase/program cycles	20	–	–	
		Average ambient temp. $T_A \leq 85$ °C, 10 K erase/program cycles	10	–	–	

11.7.3 Nonvolatile Latches (NVL)

Table 11-59. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	Vddd pin	1.71	-	5.5	V

Table 11-60. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25°C	1K	-	-	program/ erase cycles
		Programmed at 0-70°C	100	-	-	program/ erase cycles
	NVL data retention time	Programmed at 55°C	20	-	-	years
		Programmed at 0-70°C	10	-	-	years

11.7.4 SRAM

Table 11-61. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vsram	SRAM retention voltage		1.2	-	-	V

Table 11-62. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsram	SRAM operating frequency	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	DC	-	67	MHz
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	DC	-	50	MHz

Table 11-76. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO} [62]	IMO frequency stability (with factory trim)					
	62.6 MHz		–7	–	7	%
	48 MHz		–5	–	5	%
	24 MHz – Non USB mode		–4	–	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	–0.25	–	0.25	%
	12 MHz		–3	–	3	%
	6 MHz		–2	–	2	%
	3 MHz		–2	–	2	%
	3 MHz frequency stability after typical PCB assembly post-reflow.	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance.	-	±2	-	%
	Startup time[63]	From enable (during normal system operation)	–	–	13	µs
Jp–p	Jitter (peak to peak)[63]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	1.6	–	ns
Jperiod	Jitter (long term)[63]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	12	–	ns

Notes
62. F_{IMO} is measured after packaging, and thus accounts for substrate and die attach stresses.
63. Based on device characterization (Not production tested).

11.9.2 Internal Low Speed Oscillator

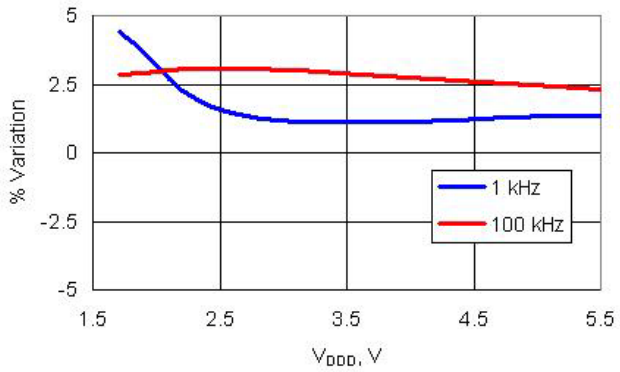
Table 11-77. ILO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[64]	F_{OUT} = 1 kHz	–	–	1.7	µA
		F_{OUT} = 33 kHz	–	–	2.6	µA
		F_{OUT} = 100 kHz	–	–	2.6	µA
	Leakage current[64]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	2.0	15	nA
		Power down mode				
	Leakage current[64]	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	200	nA
		Power down mode				

Table 11-78. ILO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time	Turbo mode	-	-	2	ms
Filo	ILO frequencies (trimmed)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C				
	100 kHz		45	100	200	kHz
	1 kHz		0.5	1	2	kHz
	ILO frequencies (untrimmed)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C				
	100 kHz		30	100	300	kHz
	1 kHz		0.3	1	3.5	kHz
Filo	ILO frequencies (trimmed)	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C				
	100 kHz		45	-	450	kHz
	1 kHz		0.5	-	5	kHz
	ILO frequencies (untrimmed)	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C				
	100 kHz		150	-	500	kHz
	1 kHz		0.3	-	6.5	kHz

Figure 11-70. ILO Frequency Variation vs. V_{DD}



Note
64. This value is calculated, not measured.
65. Based on device characterization (Not production tested).

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C38 device includes: a precision on-chip voltage reference, precision oscillators, Flash, ECC, DMA, a fixed function I^2C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and Analog Subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C38 derivatives incorporate device and Flash security in user-selectable security levels; see TRM for details.

Table 12-1. CY8C38 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[70]				Package	JTAG ID[71]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks	Opamps	DFB	CapSense	UDBs[69]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
32 KB Flash																						
CY8C3845PVE-173	50	32	4	1	-	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	-	-	29	25	4	0	48-SSOP	0x1E0AD069
CY8C3865AXA-018	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	-	-	70	62	8	0	100-TQFP	0x1E012069
CY8C3865AXA-019	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	-	72	62	8	2	100-TQFP	0x1E013069
CY8C3865PVA-060	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	-	-	29	25	4	0	48-SSOP	0x1E03C069
CY8C3865PVA-063	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	-	31	25	4	2	48-SSOP	0x1E03F069
64 KB Flash																						
CY8C3846AXE-175	50	64	8	2	-	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	-	✔	70	62	8	0	100-TQFP	0x1E0AF069
CY8C3846AXE-176	50	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x1E0B0069
CY8C3846PVE-174	50	64	8	2	-	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E0AE069
CY8C3866AXA-035	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	-	✔	70	62	8	0	100-TQFP	0x1E023069
CY8C3866AXA-038	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	-	-	70	62	8	0	100-TQFP	0x1E026069
CY8C3866AXA-039	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	-	72	62	8	2	100-TQFP	0x1E027069
CY8C3866AXA-040	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x1E028069
CY8C3866AXA-055	67	64	8	2	-	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	-	✔	70	62	8	0	100-TQFP	0x1E037069
CY8C3866PVA-005	67	64	8	2	-	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	-	-	29	25	4	0	48-SSOP	0x1E005069
CY8C3866PVA-021	67	64	8	2	-	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	-	31	25	4	2	48-SSOP	0x1E015069
CY8C3866PVA-047	67	64	8	2	-	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E02F069
CY8C3866PVA-070	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E046069

Notes

69. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the "Example Peripherals" section on page 40 for more information on how UDBs may be used.
70. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the ""I/O System and Routing" section on page 33" for details on the functionality of each of these types of I/O.
71. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

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