Infineon Technologies - CY8C3866AXA-038 Datasheet

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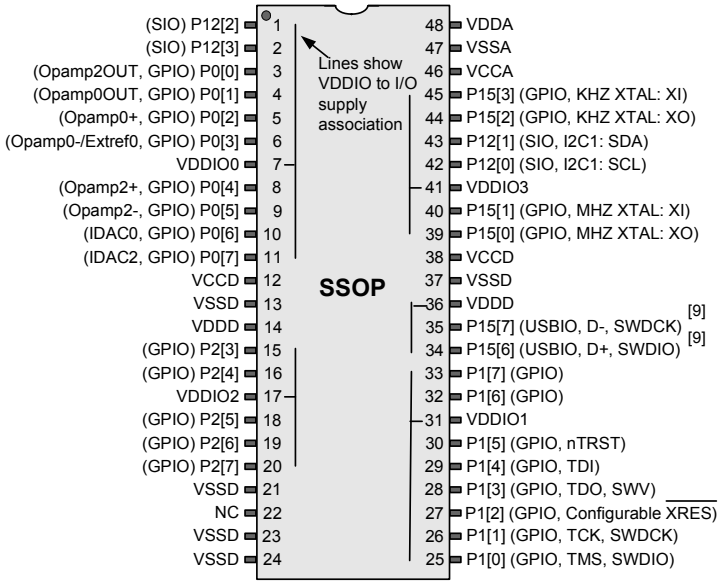
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866axa-038

Figure 2-3. 48-pin SSOP Part Pinout



Note
9. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase ‘subchains’ can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

Figure 4-2 on page 18 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 19 shows the interrupt structure and priority polling.

5.7.4 XData Space Access SFRs

The 8051 core features dual DPTR registers for faster data transfer operations. The data pointer select SFR, DPS, selects which data pointer register, DPTR0 or DPTR1, is used for the following instructions:

- MOVX @DPTR, A
- MOVX A, @DPTR
- MOVC A, @A+DPTR
- JMP @A+DPTR
- INC DPTR
- MOV DPTR, #data16

The extended data pointer SFRs, DPX0, DPX1, MXAX, and P2AX, hold the most significant parts of memory addresses during access to the xdata space. These SFRs are used only with the MOVX instructions.

During a MOVX instruction using the DPTR0/DPTR1 register, the most significant byte of the address is always equal to the contents of DPX0/DPX1.

During a MOVX instruction using the R0 or R1 register, the most significant byte of the address is always equal to the contents of MXAX, and the next most significant byte is always equal to the contents of P2AX.

5.7.5 I/O Port SFRs

The I/O ports provide digital input sensing, output drive, pin interrupts, connectivity for analog inputs and outputs, LCD, and access to peripherals through the DSI. Full information on I/O ports is found in I/O System and Routing on page 33.

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where × is port number and includes ports 0–6, 12 and 15).
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

5.7.5.1 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not 'external'—it is used by on-chip components. See Table 5-5. External, that is, off-chip, memory can be accessed using the EMIF. See External Memory Interface on page 23.

Table 5-5. XDATA Data Address Map

Address Range	Purpose
0×00 0000 – 0×00 1FFF	SRAM
0×00 4000 – 0×00 42FF	Clocking, PLLs, and oscillators
0×00 4300 – 0×00 43FF	Power management
0×00 4400 – 0×00 44FF	Interrupt controller
0×00 4500 – 0×00 45FF	Ports interrupt control
0×00 4700 – 0×00 47FF	Flash programming interface
0×00 4800 - 0×00 48FF	Cache controller
0×00 4900 – 0×00 49FF	I^2C controller
0×00 4E00 – 0×00 4EFF	Decimator
0×00 4F00 – 0×00 4FFF	Fixed timer/counter/PWMs
0×00 5000 – 0×00 51FF	I/O ports control
0×00 5400 – 0×00 54FF	EMIF control registers
0×00 5800 – 0×00 5FFF	Analog subsystem interface
0×00 6000 – 0×00 60FF	USB controller
0×00 6400 – 0×00 6FFF	UDB Working Registers
0×00 7000 – 0×00 7FFF	PHUB configuration
0×00 8000 – 0×00 8FFF	EEPROM
0×00 A000 – 0×00 A400	CAN
0×00 C000 – 0×00 C800	DFB
0×01 0000 – 0×01 FFFF	Digital Interconnect configuration
0×05 0220 – 0×05 02F0	Debug controller
0×08 0000 – 0×08 1FFF	Flash ECC bytes
0×80 0000 – 0×FF FFFF	External memory interface

Figure 6-7. GPIO Block Diagram

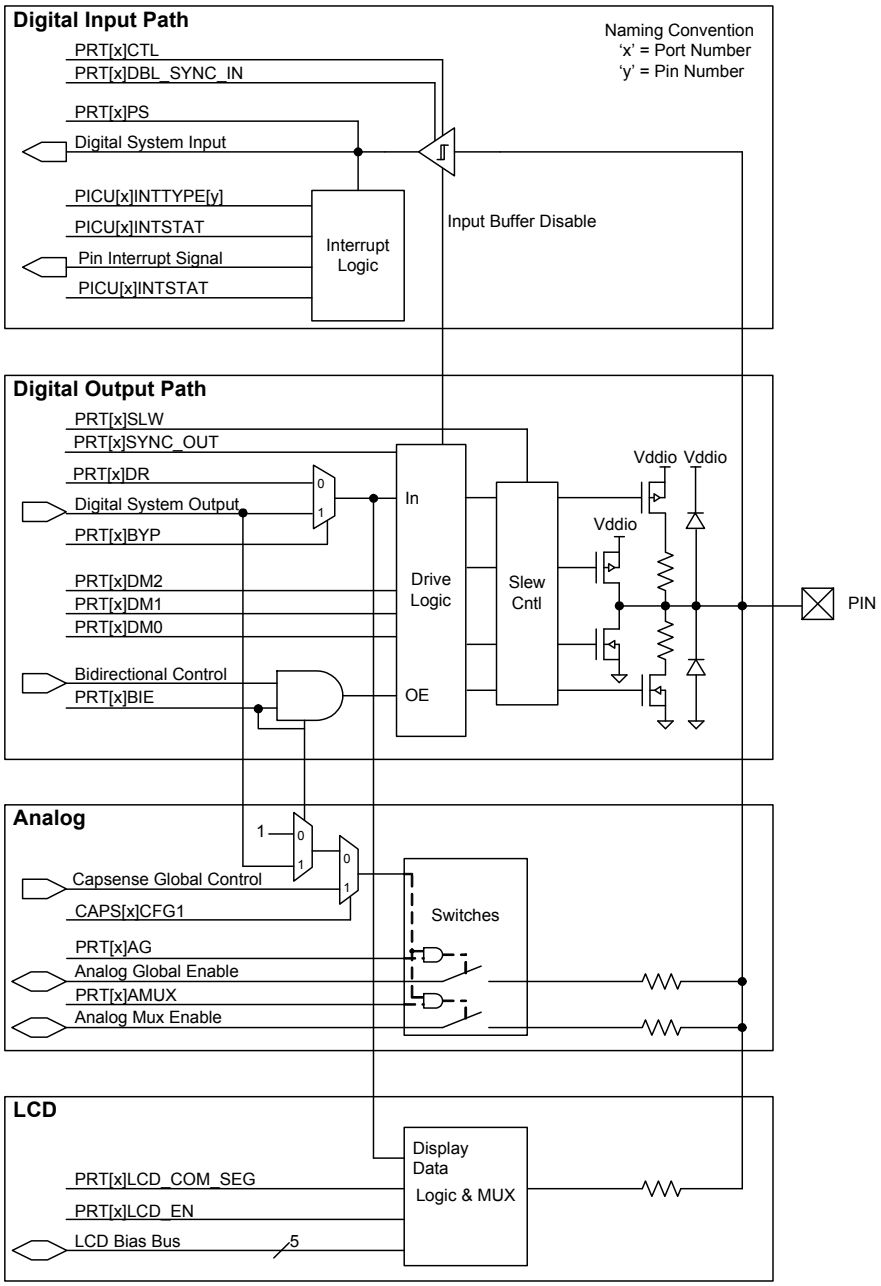
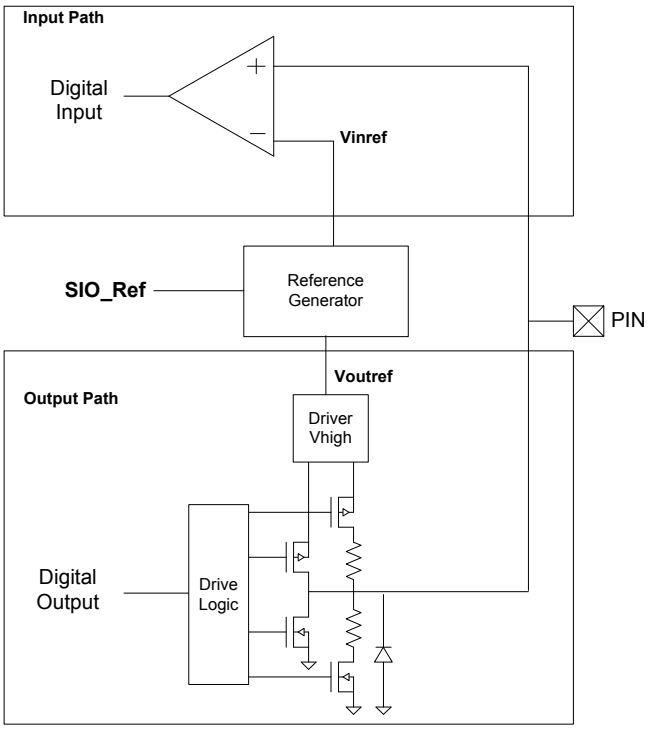


Figure 6-11. SIO Reference for Input and Output



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the Adjustable Input Level section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold. The digital input path in Figure 6-8 on page 35 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I2C bus may cause transient states on the SIO pins. The overall I2C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating V_{DD}.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where VDDIO $\leq V_{IN} \leq$ 5.5 V.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply where VDDIO $\leq V_{IN} \leq$ VDDA.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated VDDIO supply pin. The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See Figure 6-10 for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in Pinouts on page 5. The special features are:

- Digital
  - 4- to 25-MHz crystal oscillator
  - 32.768-kHz crystal oscillator
  - Wake from sleep on I^2C address match. Any pin can be used for I^2C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

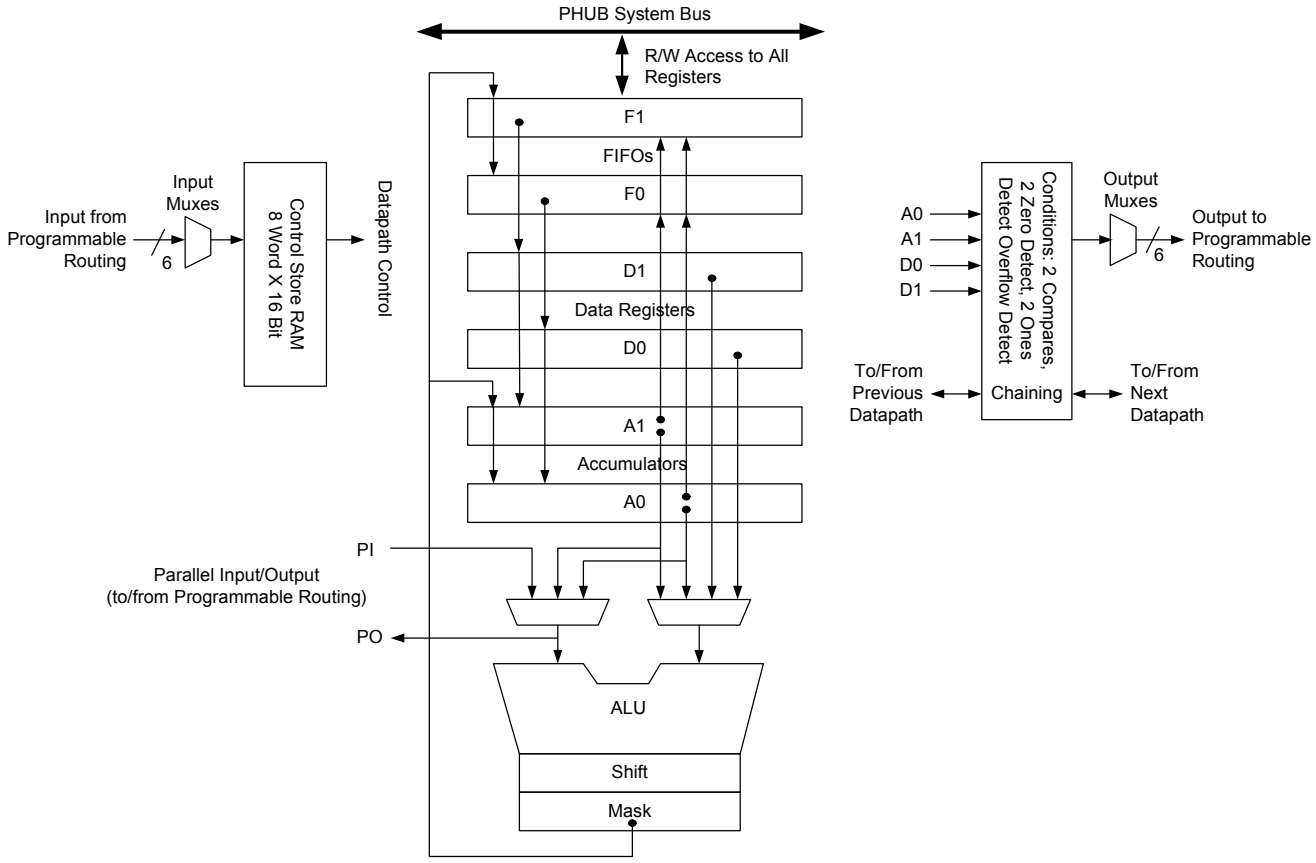
6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Datapath Configuration RAM

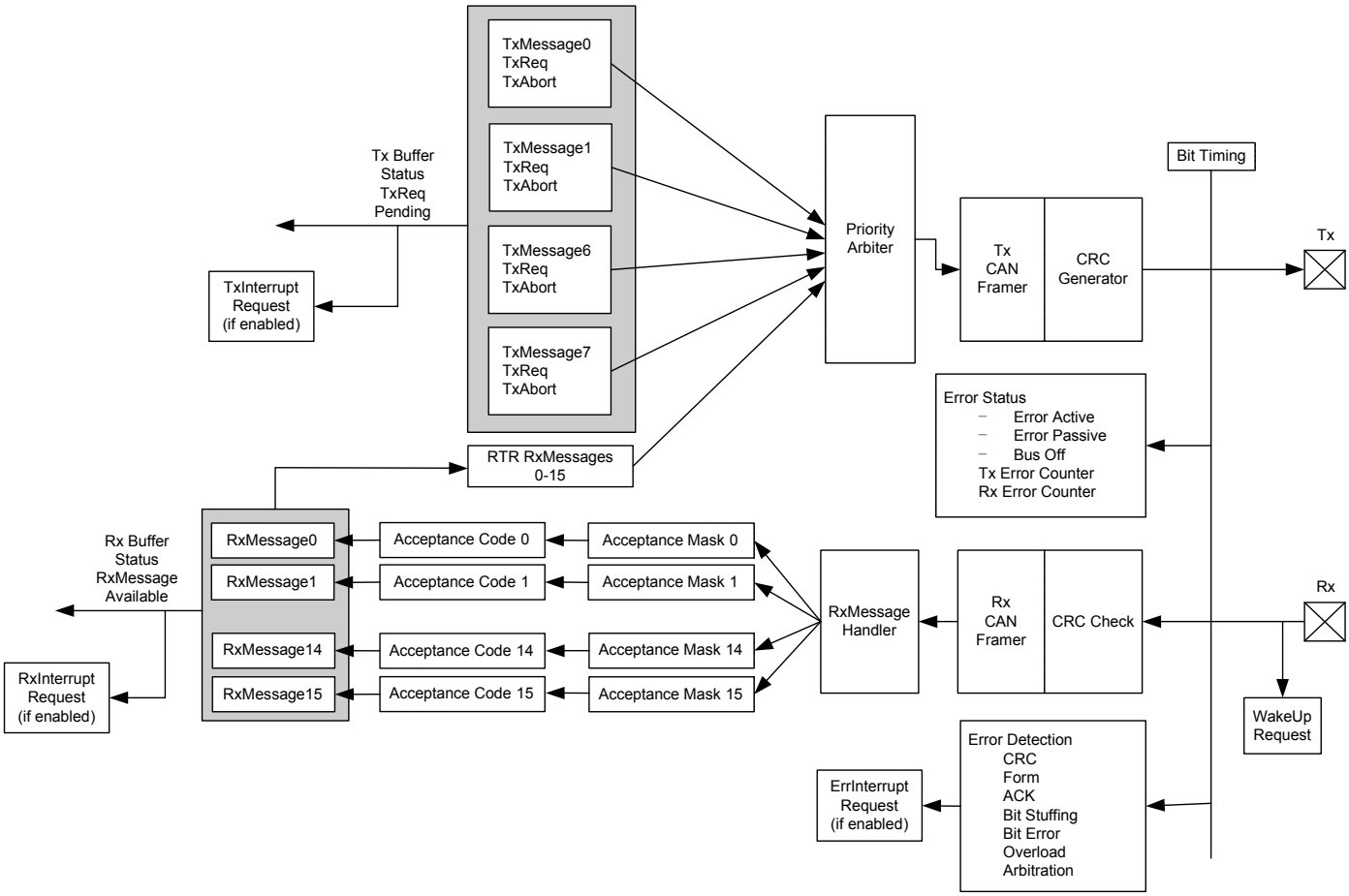
Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

Figure 7-15. CAN Controller Block Diagram



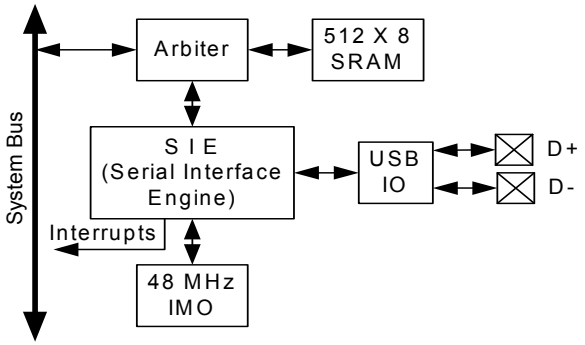
7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 33.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual memory management with no DMA access
  - Manual memory management with manual DMA access
  - Automatic memory management with automatic DMA access
- Internal 3.3-V regulator for transceiver
- Internal 48-MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB reset, suspend, and resume operations
- Bus-powered and self-powered modes

Figure 7-16. USB



7.7 Timers, Counters, and PWMs

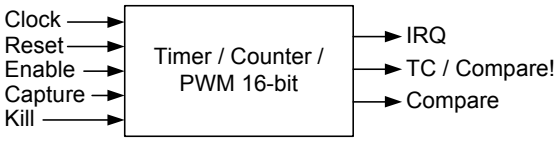
The timer/counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in UDBs as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The timer/counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-17. Timer/Counter/PWM



The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

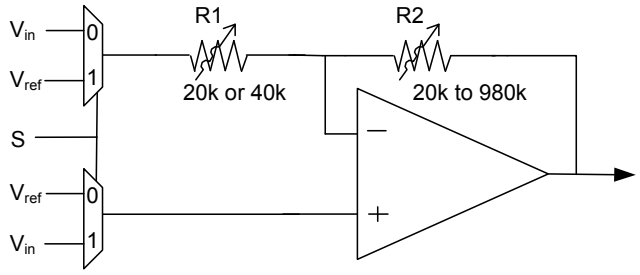
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8. The schematic in Figure 8-8 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	5.5 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-8. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

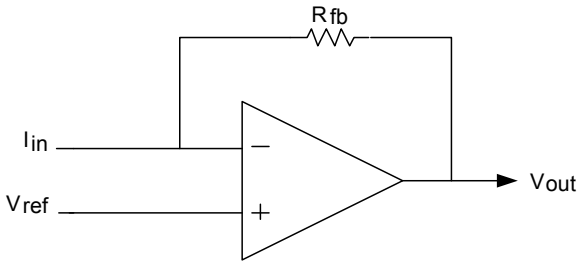
8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-9. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C38 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

9.2 Serial Wire Debug Interface

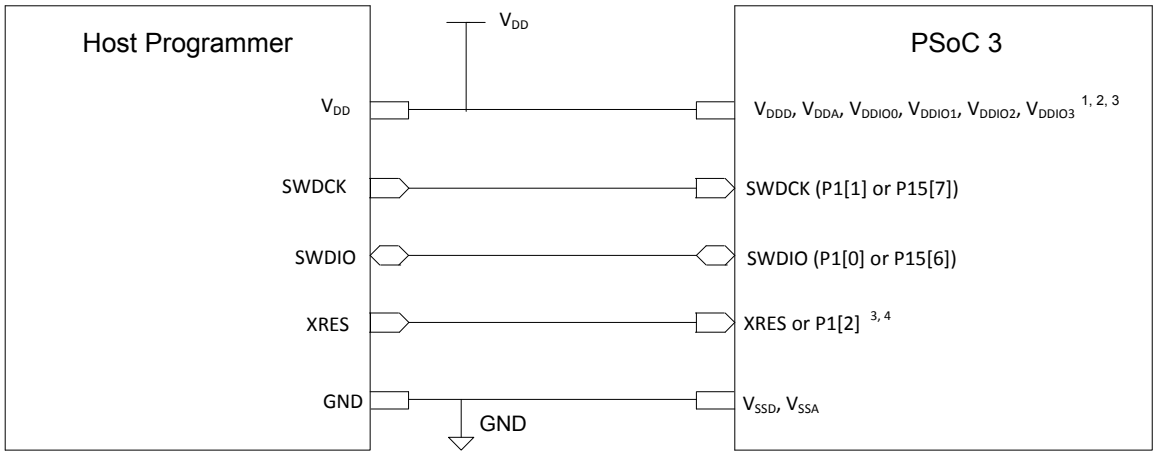
The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D– pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output.

SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 µs (key window) after reset, that pin pair (JTAG or USB) receives a predetermined sequence of 1s and 0s. SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenable the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

Figure 9-2. SWD Interface Connections between PSoC 3 and Programmer



[1] The voltage levels of the Host Programmer and the PSoC 3 voltage domains involved in Programming should be the same. XRES pin (XRES_N or P1[2]) is powered by V_{DDIO1}. The USB SWD pins are powered by V_{DDD}. So for Programming using the USB SWD pins with XRES pin, the V_{DDD}, V_{DDIO1} of PSoC 3 should be at the same voltage level as Host V_{DD}. Rest of PSoC 3 voltage domains (V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by V_{DDIO1}. So V_{DDIO1} of PSoC 3 should be at same voltage level as host V_{DD} for Port 1 SWD programming. Rest of PSoC 3 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 3.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 3. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] P1[2] will be configured as XRES by default only for 48-pin devices (without dedicated XRES pin). For devices with dedicated XRES pin, P1[2] is GPIO pin by default. So use P1[2] as Reset pin only for 48-pin devices, but use dedicated XRES pin for rest of devices.

11. Electrical Specifications

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component data sheets for full AC/DC specifications of individual functions. See the Example Peripherals on page 40 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

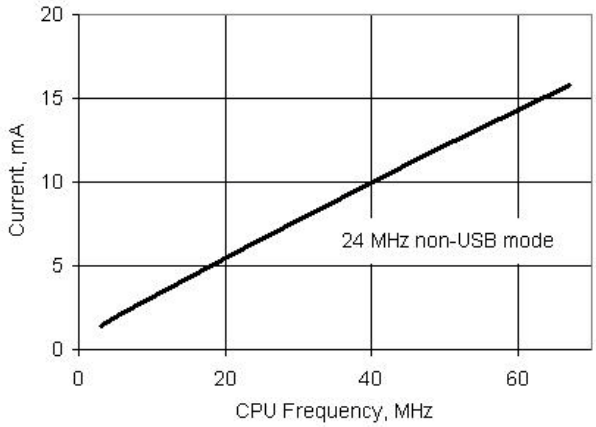
Table 11-1. Absolute Maximum Ratings DC Specifications [18]

Parameter	Description	Conditions	Min	Typ	Max	Units
Tstorag	Storage temperature	Recommended storage temperature is 0 °C–50 °C. Exposure to storage temperatures above 125 °C for extended periods may affect device reliability	–55	25	125	°C
Vdda	Analog supply voltage relative to Vssd		–0.5	–	6	V
Vddd	Digital supply voltage relative to Vssd		–0.5	–	6	V
Vddio	I/O supply voltage relative to Vssd		–0.5	–	6	V
Vcca	Direct analog core voltage input		–0.5	–	1.95	V
Vccd	Direct digital core voltage input		–0.5	–	1.95	V
Vssa	Analog ground voltage		Vssd – 0.5	–	Vssd + 0.5	V
Vgpio[19]	DC input voltage on GPIO	Includes signals sourced by Vdda and routed internal to the pin	Vssd – 0.5	–	Vddio + 0.5	V
Vsio	DC input voltage on SIO	Output disabled	Vssd – 0.5	–	7	V
		Output enabled	Vssd – 0.5	–	6	V
Ivddio [20]	Current per Vddio supply pin	–40 °C to +85 °C	–	–	100	mA
		–40 °C to +125 °C	–	–	40	
I_{GPIO}	GPIO current		–30	–	41	mA
I_{SIO}	SIO current		–49	–	28	mA
I_{USBIO}	USBIO current		–56	–	59	mA
V_{EXTREF}	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current [21]		–140	–	140	mA
ESD_{HBM}	Electrostatic discharge voltage, Human body model	V_{SSA} tied to V_{SSD}	2200	–	–	V
		V_{SSA} not tied to V_{SSD}	750	–	–	V
ESD_{CDM}	Electro-static discharge voltage	Charge Device Model	500	–	–	V

Note Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

Notes
18. Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.
19. The Vddio supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin ≤ Vddio ≤ Vdda.
20. Maximum value 100 mA of Iddio applies only to –40 °C to +85 °C range and the limit of Iddio parameter for the –40 °C to +125 °C range is 40 mA.
21. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

Figure 11-1. Active Mode Current vs F_{CPU}, V_{DD} = 3.3 V, Temperature = 25 °C



11.4.3 USBIO

Table 11-10. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull up resistance	With idle bus	0.900	-	1.575	kΩ
Rusba	USB D+ pull up resistance	While receiving traffic	1.425	-	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to Vss, internal pull up enabled	2.8	-	3.6	V
Volusb	Static output low	15 kΩ ±5% to Vss, internal pull up enabled	-	-	0.3	V
Vihgpio	Input voltage high, GPIO mode	$V_{DDD} \geq 3$ V	2	–	–	V
Vilgpio	Input voltage low, GPIO mode	$V_{DDD} \geq 3$ V	–	–	0.8	V
Vohgpio	Output voltage high, GPIO mode	Ioh = 4 mA, Vddio ≥ 3 V	2.4	-	-	V
Volgpio	Output voltage low, GPIO mode	Iol = 4 mA, Vddio ≥ 3 V	-	-	0.3	V
Vdi	Differential input sensitivity	|(D+)-(D-)|	-	-	0.2	V
Vcm	Differential input common mode range		0.8	-	2.5	V
Vse	Single ended receiver threshold		0.8	-	2	V
Rps2	PS/2 pull up resistance	In PS/2 mode, with PS/2 pull up enabled	3	-	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (-1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	28	-	44	Ω
		Including Rext, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	28	-	46	Ω
Cin	USB transceiver input capacitance		-	-	20	pF
Iil [35]	Input leakage current (absolute value)	25°C, Vddio = 3.0 V	-	-	2	nA

Note
35. Based on device characterization (not production tested).

Figure 11-20. Opamp Operating Current vs Vdda and Power Mode

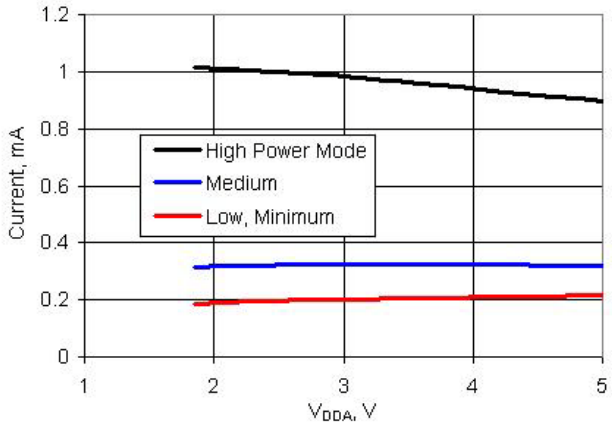
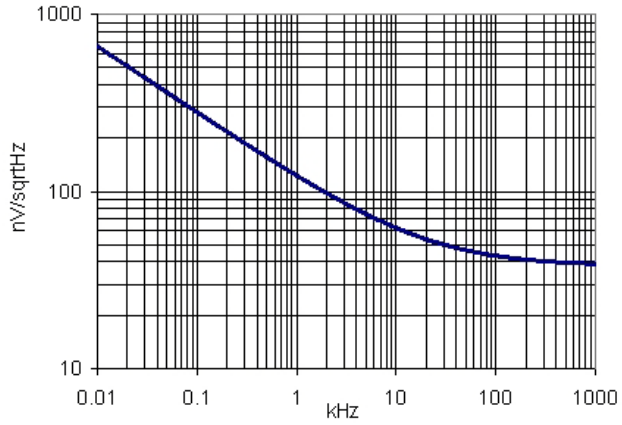


Table 11-16. Opamp AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 15 pF load	1	–	–	MHz
		Power mode = low, 15 pF load	2	–	–	MHz
		Power mode = medium, 200 pF load	1	–	–	MHz
		Power mode = high, 200 pF load	2.5	–	–	MHz
SR	Slew rate, 20% - 80%	Power mode = low, 15 pF load	1.1	–	–	V/µs
		Power mode = medium, 200 pF load	0.9	–	–	V/µs
		Power mode = high, 200 pF load	3	–	–	V/µs
e_n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	45	–	nV/sqrtHz

Figure 11-21. Opamp Noise vs Frequency, Power Mode = High, Vdda = 5 V



11.5.2 Delta-Sigma ADC

Unless otherwise specified, operating conditions are:

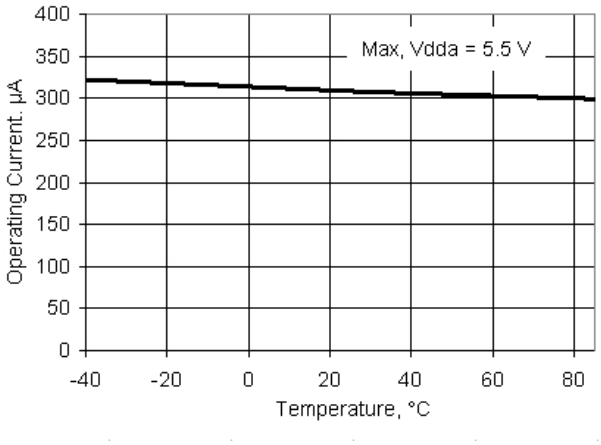
- Operation in continuous sample mode
- fclk = 3.072 MHz for resolution = 16 to 20 bits; fclk = 6.144 MHz for resolution = 8 to 15 bits
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-17. 20-bit Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	20	bits
	Number of channels, single ended		–	–	No. of GPIO	–
	Number of channels, differential	Differential pair is formed using a pair of GPIOs.	–	–	No. of GPIO/2	–
	Monotonic	Yes	–	–	–	–
Ge	Gain error	Buffered, buffer gain = 1, Range = ±1.024 V, 16-bit mode, 25 °C	–	–	±0.2	%
Gd	Gain drift	Buffered, buffer gain = 1, Range = ±1.024 V, 16-bit mode	–	–	50	ppm/°C
Vos	Input offset voltage	Buffered, 16-bit mode, full voltage range	–	–	±0.2	mV
		Buffered, 16-bit mode, V_{DDA} = 1.8 V ± 5%	–	–	±0.1	mV
TCVos	Temperature coefficient, input offset voltage	Buffer gain = 1, 16-bit, Range = ±1.024 V	–	–	1	µV/°C
	Input voltage range, single ended[36]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential unbuffered[36]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential, buffered[36]		V_{SSA}	–	V_{DDA} – 1	V
PSRRb	Power supply rejection ratio, buffered[36]	Buffer gain = 1, 16-bit, Range = ±1.024 V	90	–	–	dB
CMRRb	Common mode rejection ratio, buffered[36]	Buffer gain = 1, 16 bit, Range = ±1.024 V	85	–	–	dB
INL20	Integral non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±32	LSB
DNL20	Differential non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL16	Integral non linearity[36]	Range = ±1.024 V, unbuffered; 2.7 V ≤ V_{DDA} ≤ 5.5 V range	–	–	±2	LSB
		1.71 V ≤ V_{DDA} < 2.7 V range	–2.1	–	+2.7	LSB
DNL16	Differential non linearity[36]	Range = ±1.024 V, unbuffered; 2.7 V ≤ V_{DDA} ≤ 5.5 V range	–	–	±1	LSB
		1.71 V ≤ V_{DDA} < 2.7 V range	–1	–	+1.1	LSB
INL12	Integral non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL12	Differential non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL8	Integral non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL8	Differential non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB

Note
36. Based on device characterization (not production tested).

Figure 11-53. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode

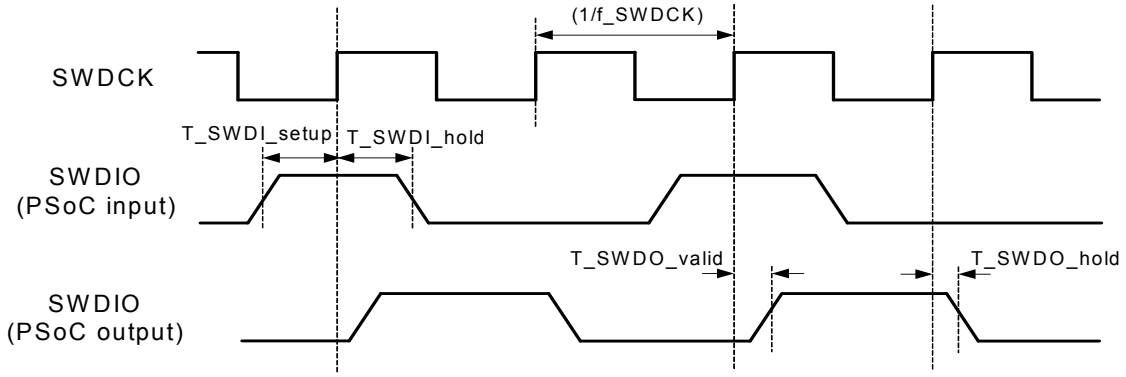


11.8.5 SWD Interface

Table 11-73. SWD Interface AC Specifications[30]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_SWDCK	SWDCLK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14[61]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[61]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V, SWD over USBIO pins	–	–	5.5[61]	MHz
T_SWDI_setup	SWDIO input setup before SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDI_hold	SWDIO input hold after SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDO_valid	SWDCK high to SWDIO output	T = 1/f_SWDCK max	–	–	2T/5	

Figure 11-66. SWD Interface Timing



11.8.6 SWV Interface

Table 11-74. SWV Interface AC Specifications[30]

Parameter	Description	Conditions	Min	Typ	Max	Units
	SWV mode SWV bit rate		-	-	33	Mbit

Notes
60. f_TCK must also be no more than 1/3 CPU clock frequency.
61. f_SWDCK must also be no more than 1/3 CPU clock frequency.

17. Revision History

Description Title: PSoC® 3: CY8C38 Automotive Family Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 001-54683				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2742918	07/23/09	VIVG / PYRS	New data sheet for PSoC 3 Automotive
*A	2750090	08/10/09	SHEA	Minor ECN to correct title on first page
*B	2800070	01/05/10	SECA	Added Tio_init parameter and updated Tstartup values. Updated PGA and UGB AC Specs table and changed gain error condition in PGA DC table. Added PCB Layout and PCB Schematic figures. Updated Figure 1-1 and Figure 8-1. Removed 12-Bit Del-Sig ADC table.
*C	2921624	04/26/2010	MKEA	Updated Active Mode Idd values in Table 11-2 Updated Boost AC and DC specifications Updated solder paste reflow temperature (Table 11-3) Moved Filo spec from ILO DC to ILO AC table Updated Figure 7-14, Interrupt and DMA processing Added Bytes column in Tables 4-1 and 4-5 Updated Figure 6-3, Power mode transitions Updated JTAG and SWD specifications Updated Interrupt Vector table Updated Sales links Updated PCB Schematic Updated Vbias spec Added UDBs subsection under 11.6 Digital Peripherals Updated Iout parameter in LCD Direct Drive DC Specs table Added footnote in PLL AC Specification table Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table Updated Icc parameter in LCD Direct Drive DC Specs table Updated Tstartup parameter in AC Specifications table Updated LVD in Tables 6-2 and 6-3 In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9 Added PLL intermediate frequency row with footnote in PLL AC Specs table Added bullets on CapSense in page 1; added CapSense column in Section Updated Figure 2-6 (PCB Layout) Updated Tstartup values in Table 11-3 Updated IMO frequency Updated section 5.2 and Table 11-2 to correct suggestion of execution from Flash Updated Vref specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Tresp, high and low power modes, in Table 11-24. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table 72. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Updated SNR condition in Table 11-20
*D	3490311	01/11/2012	GIR	Updated Figure 6-7.
*E	3648803	06/18/2012	WKA / MKEA	No changes. EROS update. Updated 100-Pin TQFP package outline spec 51-85048 from *E to *G revision.
*F	3732521	09/03/2012	MKEA	Updated package diagram 51-85061 to *F revision.
*G	3994809	05/08/2013	KPAT	Updated all tables in Electrical Specifications. Updated Ordering Information (Updated part numbers, JTAG ID). Removed all references of Vboost across the document.

17. Revision History *(continued)*

Description Title: PSoC® 3: CY8C38 Automotive Family Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 001-54683				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*H (cont.)	4094193	08/30/2013	NFB / ANMD	Updated Electrical Specifications: Updated Device Level Specifications: Updated Table 11-2. Updated Table 11-3. Updated Inputs and Outputs: Updated GPIO: Updated Table 11-7. Removed figure “GPIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load” and figure “GPIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load”. Updated Analog Peripherals: Updated Delta-Sigma ADC: Updated Table 11-17. Updated Table 11-18. Updated Voltage Reference: Updated Table 11-24. Updated IDAC: Updated Table 11-28. Updated Memory: Updated Flash: Updated Table 11-56. Updated Clocking: Updated Internal Main Oscillator: Updated Table 11-76. Updated Packaging: spec 51-85048 – Changed revision from *G to *H. Updated in new template. Completing Sunset Review.
*I	4174912	10/26/2013	NFB / ANMD	Updated Pinouts: Added Note 8 and referred the same note in 100 mA in description. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 11-1. Added Note 18 and referred the same note in Table 11-1. Added Note 20 and referred the same note in Ivddio parameter in Table 11-1. Updated Device Level Specifications: Updated Table 11-2. Updated Analog Peripherals: Updated Opamp: Updated Table 11-15. Updated Voltage Reference: Updated Table 11-24. Updated Packaging: Updated Table 13-1.
*J	4188568	11/14/2013	WKA	No content update.

17. Revision History *(continued)*

Description Title: PSoC® 3: CY8C38 Automotive Family Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 001-54683				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*K	4296459	03/03/2014	ANMD	Updated Digital Subsystem: Updated I^2C: Updated Note 17. Updated Electrical Specifications: Updated Analog Peripherals: Updated Delta-Sigma ADC: Updated Table 11-17: Updated Conditions of Vos parameter. Updated Memory: Updated Flash: Updated Table 11-56: Added Note 55 and referred the same note in “Flash data retention time” in description column. Replaced “Tjavg” with “T_A” in last row in conditions column. Updated Packaging: spec 51-85048 – Changed revision from *H to *I.