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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866axa-039

Contents

Figure 2-4. 100-pin TQFP Part Pinout

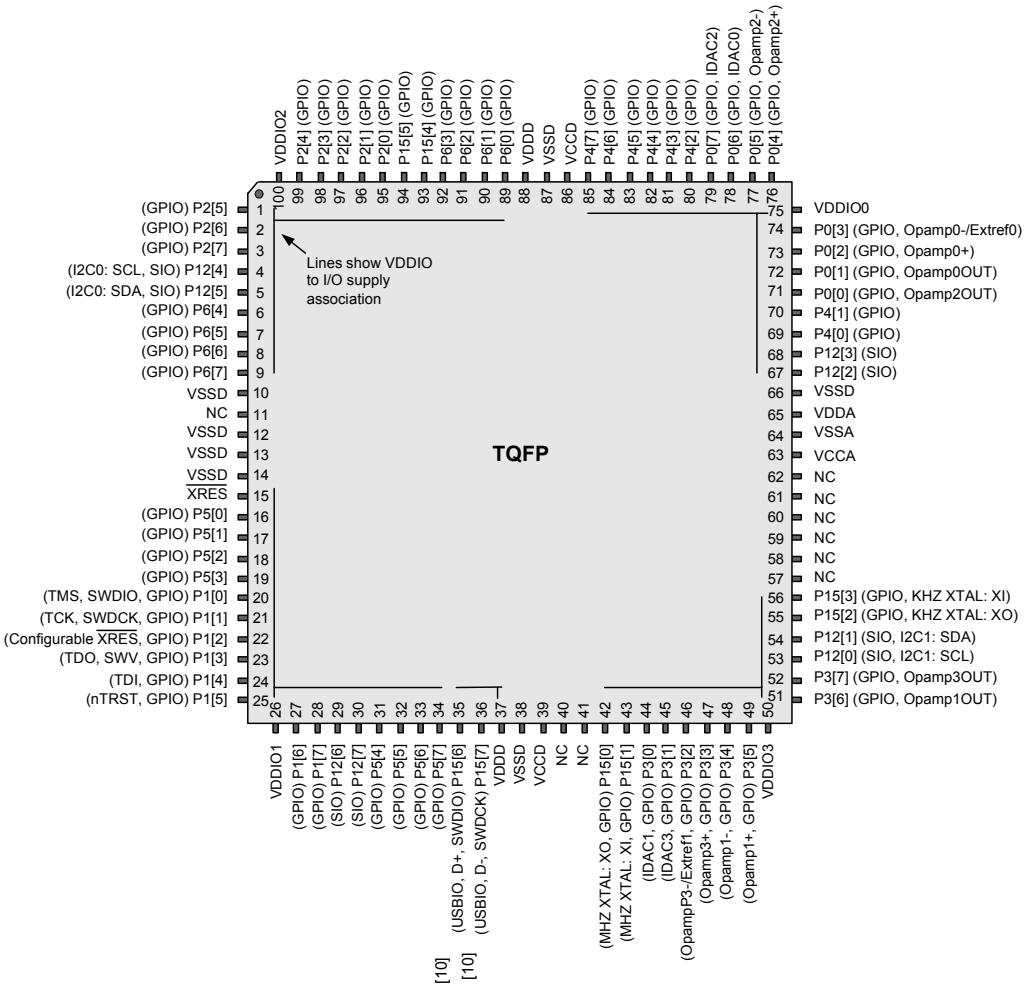


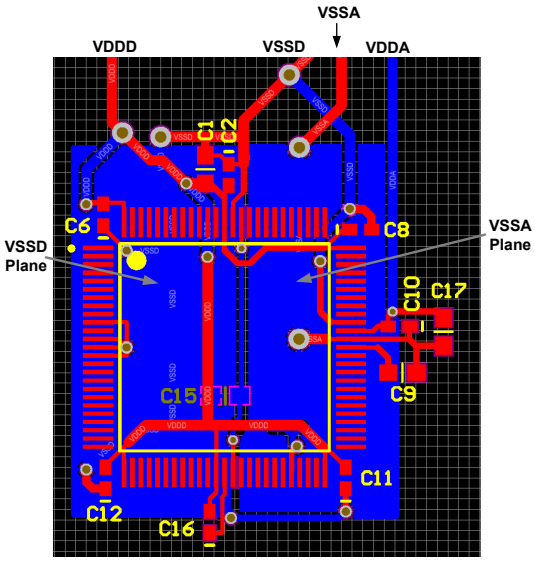
Figure 2-5 and Figure 2-6 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-5 and Power System on page 29. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled Vssd must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note, AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

Note
10. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3

Low resistance output pin for high current DACs (IDAC).

Opamp0OUT, Opamp1OUT, Opamp2OUT, Opamp3OUT

High current output of uncommitted opamp[11].

Extref0, Extref1

External reference input to the analog system.

Opamp0–, Opamp1–, Opamp2–, Opamp3–

Inverting input to uncommitted opamp.

Opamp0+, Opamp1+, Opamp2+, Opamp3+

Noninverting input to uncommitted opamp.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[11].

I2C0: SCL, I2C1: SCL

I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25-MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

TMS

JTAG test mode select programming and debug port connection.

Note
11. GPIOs with opamp outputs are not recommended for use with CapSense.

4.3.1.2 Logical Instructions

The logical instructions perform Boolean operations such as AND, OR, XOR on bytes, rotate of accumulator contents, and swap of nibbles in an accumulator. The Boolean operations on the bytes are performed on the bit-by-bit basis. Table 4-2 shows the list of logical instructions and their description.

Table 4-2. Logical Instructions

Mnemonic	Description	Bytes	Cycles
ANL A,Rn	AND register to accumulator	1	1
ANL A,Direct	AND direct byte to accumulator	2	2
ANL A,@Ri	AND indirect RAM to accumulator	1	2
ANL A,#data	AND immediate data to accumulator	2	2
ANL Direct, A	AND accumulator to direct byte	2	3
ANL Direct, #data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to accumulator	1	1
ORL A,Direct	OR direct byte to accumulator	2	2
ORL A,@Ri	OR indirect RAM to accumulator	1	2
ORL A,#data	OR immediate data to accumulator	2	2
ORL Direct, A	OR accumulator to direct byte	2	3
ORL Direct, #data	OR immediate data to direct byte	3	3
XRL A,Rn	XOR register to accumulator	1	1
XRL A,Direct	XOR direct byte to accumulator	2	2
XRL A,@Ri	XOR indirect RAM to accumulator	1	2
XRL A,#data	XOR immediate data to accumulator	2	2
XRL Direct, A	XOR accumulator to direct byte	2	3
XRL Direct, #data	XOR immediate data to direct byte	3	3
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right though carry	1	1
SWAP A	Swap nibbles within accumulator	1	1

4.3.1.3 Data Transfer Instructions

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed addressing mode. Table 4-3 lists the various data transfer instructions available.

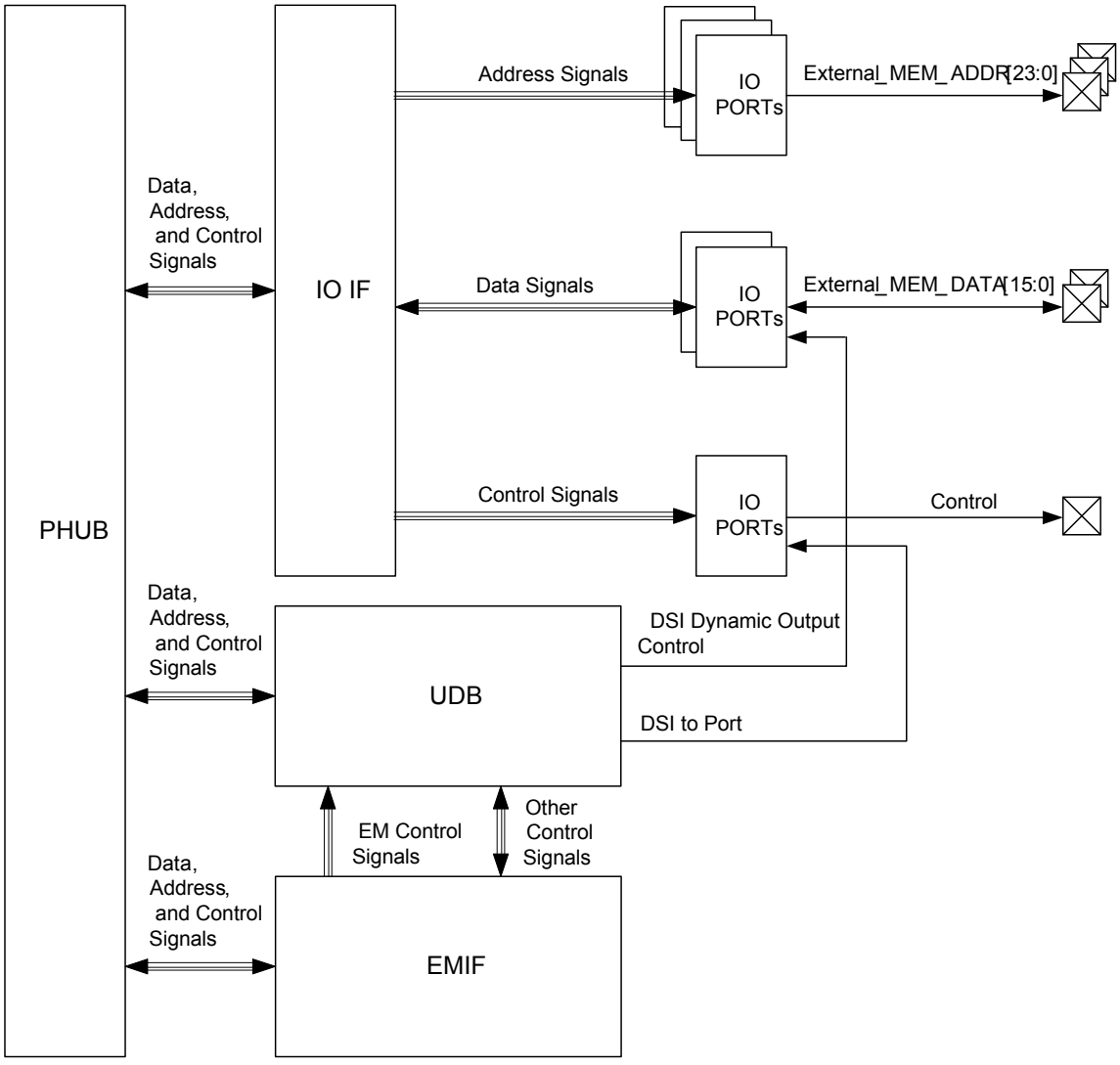
4.3.1.4 Boolean Instructions

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. Table 4-4 lists the available Boolean instructions.

5.6 External Memory Interface

CY8C38 provides an EMIF for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles. Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C38 supports only one type of external memory device at a time. External memory can be accessed through the 8051 xdata space; up to 24 address bits can be used. See "xdata Space" section on page 25. The memory can be 8 or 16 bits wide.

Figure 5-1. EMIF Block Diagram



detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

- IPOR – Initial power-on reset

  At initial power on, IPOR monitors the power voltages V_{DDD}, V_{DDA}, V_{CCD} and V_{CCA}. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 150 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  If after the IPOR triggers either V_{DDX} drops back below the trigger point, in a non-monotonic fashion, it must remain below that point for at least 10 µs. The hysteresis of the IPOR trigger point is typically 100 mV.

  After boot, the IPOR circuit is disabled and voltage supervision is handed off to the precise low-voltage reset (PRES) circuit.

- PRES – Precise low voltage reset

  This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

  After PRES has been deasserted, at least 10 µs must elapse before it can be reasserted.

  In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

- ALVI, DLVI, AHVI – Analog/digital low voltage interrupt, analog high voltage interrupt

  Interrupt circuits are available to detect when VDDA and VDDD go outside a voltage range. For AHVI, VDDA is compared to a fixed trip level. For ALVI and DLVI, VDDA and VDDD are compared to trip levels that are programmable, as listed in Table 6-4. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-4. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	1.71 V–5.5 V	1.70 V–5.45 V in 250 mV increments
ALVI	VDDA	1.71 V–5.5 V	1.70 V–5.45 V in 250 mV increments
AHVI	VDDA	1.71 V–5.5 V	5.75 V

  The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wakeup sequence. The interrupt is then recognized and may be serviced.

  The buzz frequency is adjustable, and should be set to be less than the minimum time that any voltage is expected to be out of range. For details on how to adjust the buzz frequency, see the TRM.

6.3.1.2 Other Reset Sources

- XRES – External reset

  PSoC 3 has either a single GPIO pin that is configured as an external reset or a dedicated XRES pin. Either the dedicated XRES pin or the GPIO pin, if configured, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

  After XRES has been deasserted, at least 10 µs must elapse before it can be reasserted.

  The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

- SRES – Software reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES – Watchdog timer reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and SIO provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[13], and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

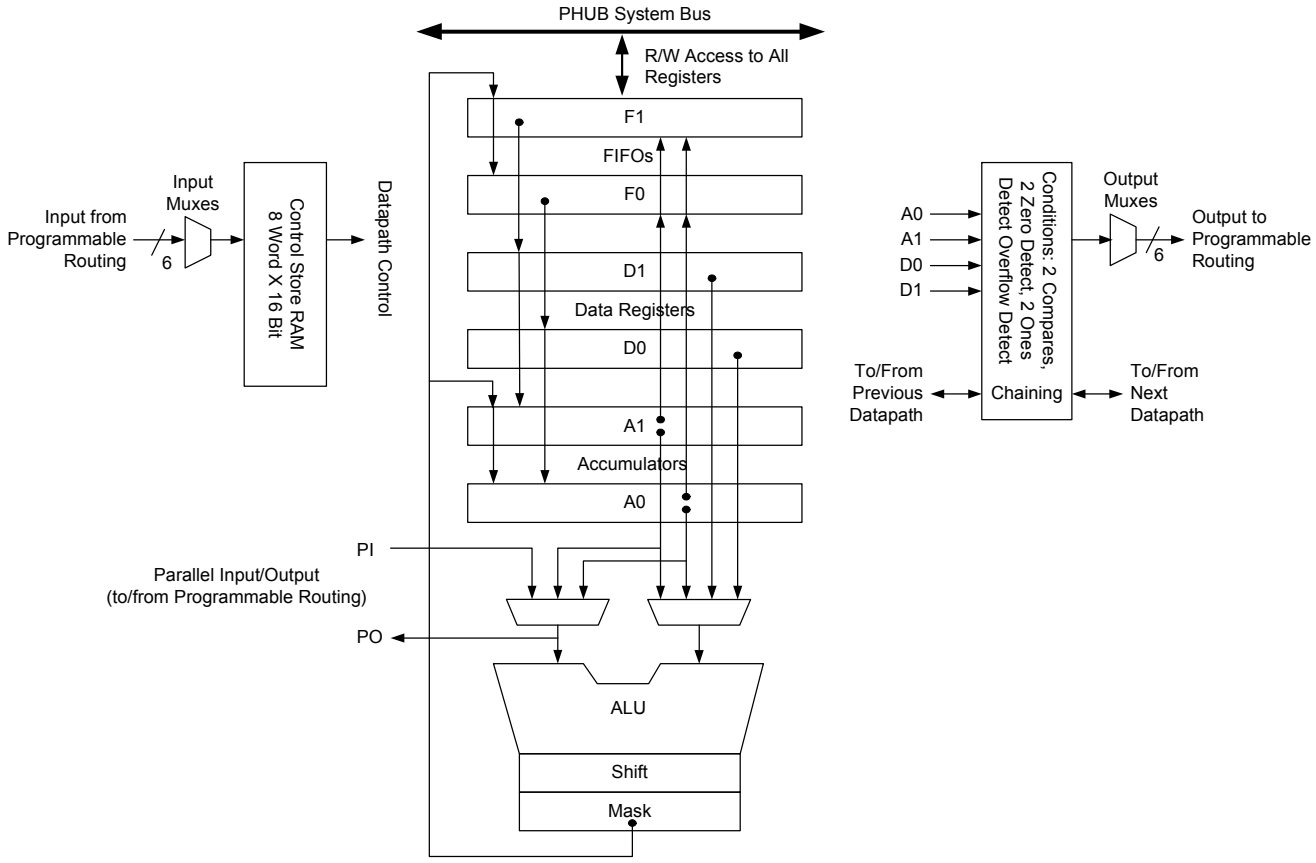
- Features supported by both GPIO and SIO:
  - User programmable port reset state
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins
  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port
  - Slew rate controlled digital output drive mode
  - Access port control and configuration registers on either port basis or pin basis
  - Separate port read (PS) and write (DR) data registers to avoid read modify write errors
  - Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense[13]
  - Analog input and output capability
  - Continuous 100 µA clamp current capability
  - Standard drive strength down to 1.7 V
- Additional features only provided on SIO pins:
  - Higher drive strength than GPIO
  - Hot swap capability (5 V tolerance at any operating V_{DD})
  - Programmable and regulated high input and output drive levels down to 1.2 V
  - No analog input, CapSense, or LCD capability
  - Over voltage tolerance up to 5.5 V
  - SIO can act as a general purpose analog comparator
- USBIO features:
  - Full speed USB 2.0 compliant I/O
  - Highest drive strength for general purpose use
  - Input, output, or both for CPU and DMA
  - Input, output, or both for digital peripherals
  - Digital output (CMOS) drive mode
  - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

Note
13. GPIOs with opamp outputs are not recommended for use with CapSense.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Datapath Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

Figure 7-15. CAN Controller Block Diagram

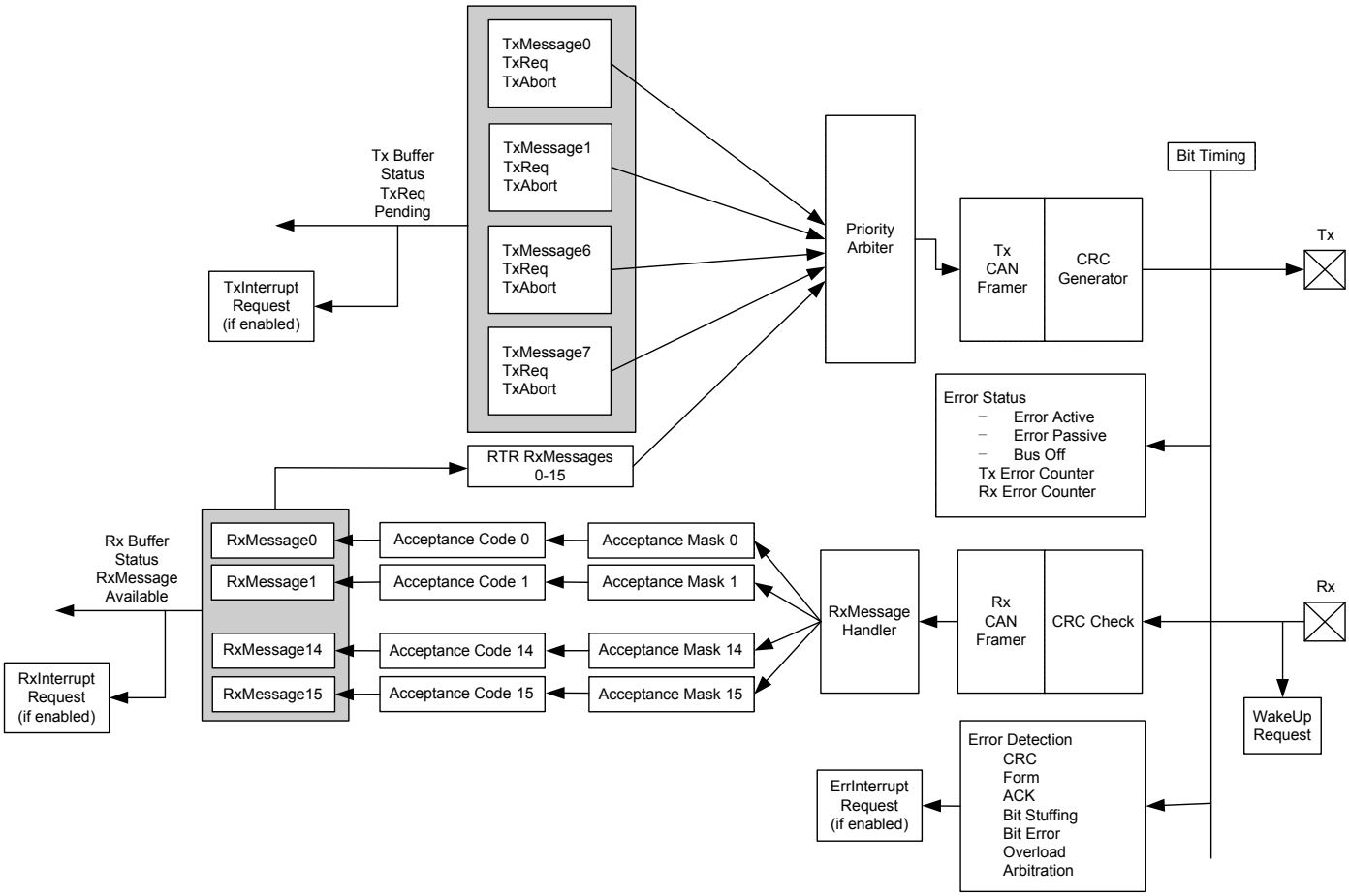
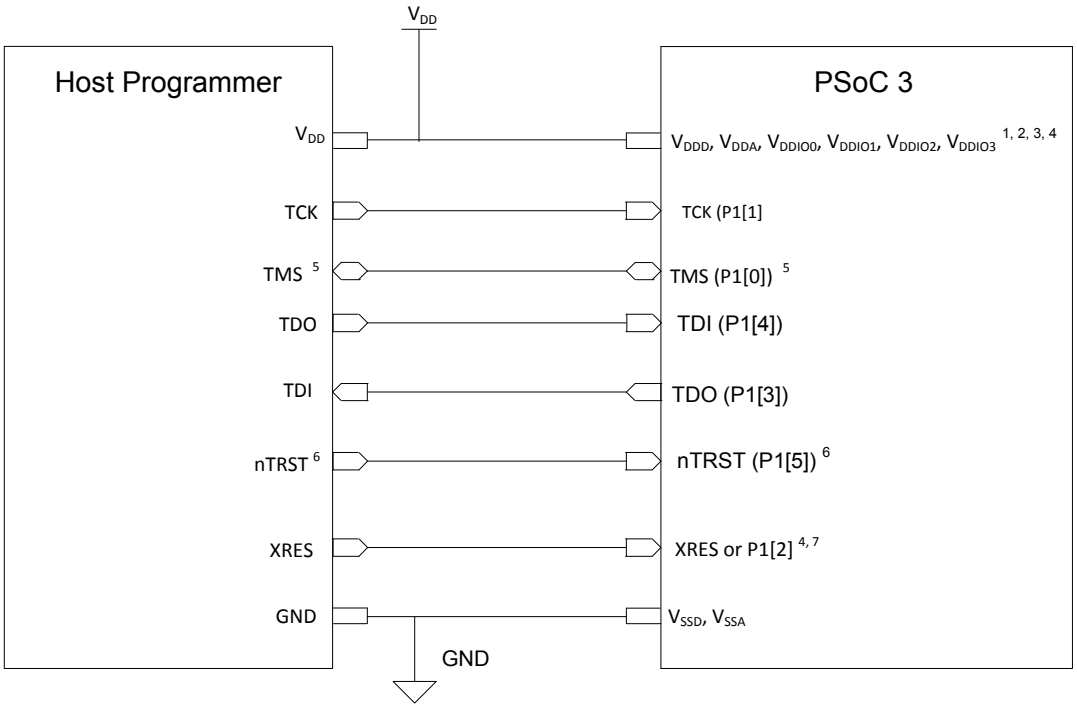


Figure 9-1. JTAG Interface Connections between PSoC 3 and Programmer



[1] The voltage levels of Host Programmer and the PSoC 3 voltage domains involved in Programming should be same. The Port 1 JTAG pins, XRES pin (XRES_N or P1[2]) are powered by V_{DDIO1}. So, V_{DDIO1} of PSoC 3 should be at same voltage level as host V_{DD}. Rest of PSoC 3 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 3.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 3. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] For JTAG Programming, Device reset can also be done without connecting to the XRES pin or Power cycle mode by using the TMS,TCK,TDI, TDO pins of PSoC 3, and writing to a specific register. But this requires that the DPS setting in NVL is not equal to "Debug Ports Disabled".

[5] By default, PSoC 3 is configured for 4-wire JTAG mode unless user changes the DPS setting. So the TMS pin is unidirectional. But if the DPS setting is changed to non-JTAG mode, the TMS pin in JTAG is bi-directional as the SWD Protocol has to be used for acquiring the PSoC 3 device initially. After switching from SWD to JTAG mode, the TMS pin will be uni-directional. In such a case, unidirectional buffer should not be used on TMS line.

[6] nTRST JTAG pin (P1[5]) cannot be used to reset the JTAG TAP controlller during first time programming of PSoC 3 as the default setting is 4-wire JTAG (nTRST disabled). Use the TMS, TCK pins to do a reset of JTAG TAP controller.

[7] If XRES pin is used by host, P1[2] will be configured as XRES by default only for 48-pin devices (without dedicated XRES pin). For devices with dedicated XRES pin, P1[2] is GPIO pin by default. So use P1[2] as Reset pin only for 48-pin devices, but use dedicated XRES pin for rest of devices.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ	Max	Units
	Sleep Mode[26]						
	CPU OFF RTC = ON (= ECO32K ON, in low power mode) Sleep timer = ON (= ILO ON at 1 kHz) [27] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V–5.5 V	T = –40 °C	–	1.1	2.3	µA
			T = 25 °C	–	1.1	2.2	µA
			T = 85 °C	–	15	30	µA
			T = 125 °C	–	20.3	30	µA
		$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = –40 °C	–	1	2.2	µA
			T = 25 °C	–	1	2.1	µA
			T = 85 °C	–	12	28	µA
			T = 125 °C	–	18.5	28	µA
		$V_{CC} = V_{DDIO}$ = 1.71 V–1.95 V	T = 25 °C	–	2.2	4.2	µA
			T = 125 °C	–	16.2	28	µA
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I^2C Wake = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = 25 °C	–	2.2	2.7	µA
	I^2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = 25 °C	–	2.2	2.8	µA

Notes
26. If Vccd and Vcca are externally regulated, the voltage difference between Vccd and Vcca must be less than 50 mV.
27. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.

11.4.3 USBIO

Table 11-10. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull up resistance	With idle bus	0.900	-	1.575	kΩ
Rusba	USB D+ pull up resistance	While receiving traffic	1.425	-	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to Vss, internal pull up enabled	2.8	-	3.6	V
Volusb	Static output low	15 kΩ ±5% to Vss, internal pull up enabled	-	-	0.3	V
Vihgpio	Input voltage high, GPIO mode	$V_{DDD} \geq 3$ V	2	–	–	V
Vilgpio	Input voltage low, GPIO mode	$V_{DDD} \geq 3$ V	–	–	0.8	V
Vohgpio	Output voltage high, GPIO mode	Ioh = 4 mA, Vddio ≥ 3 V	2.4	-	-	V
Volgpio	Output voltage low, GPIO mode	Iol = 4 mA, Vddio ≥ 3 V	-	-	0.3	V
Vdi	Differential input sensitivity	|(D+)-(D-)|	-	-	0.2	V
Vcm	Differential input common mode range		0.8	-	2.5	V
Vse	Single ended receiver threshold		0.8	-	2	V
Rps2	PS/2 pull up resistance	In PS/2 mode, with PS/2 pull up enabled	3	-	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (-1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	28	-	44	Ω
		Including Rext, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	28	-	46	Ω
Cin	USB transceiver input capacitance		-	-	20	pF
Iil [35]	Input leakage current (absolute value)	25°C, Vddio = 3.0 V	-	-	2	nA

Note
35. Based on device characterization (not production tested).

Table 11-11. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 - 0.25%	12	12 + 0.25%	MHz
Tdjr1	Receiver data jitter tolerance to next transition		-8	-	8	ns
Tdjr2	Receiver data jitter tolerance to pair transition		-5	-	5	ns
Tudj1	Driver differential jitter to next transition		-3.5	-	3.5	ns
Tudj2	Driver differential jitter to pair transition		-4	-	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		-2	-	5	ns
Tfeopt	Source SE0 interval of EOP		160	-	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	-	-	ns
Tfst	Width of SE0 interval during differential transition		-	-	14	ns
Fgpio_out	GPIO mode output operating frequency	3 V ≤ Vddd ≤ 5.5 V	-	-	20	MHz
		Vddd = 1.71 V	-	-	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% Vddd	Vddd > 3 V, 25 pF load	–	–	12	ns
		Vddd = 1.71 V, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% Vddd	Vddd > 3 V, 25 pF load	–	–	12	ns
		Vddd = 1.71 V, 25 pF load	–	–	40	ns

Figure 11-15. USBIO Output Rise and Fall Times, GPIO Mode, V_{DDD} = 3.3 V, 25 pF Load

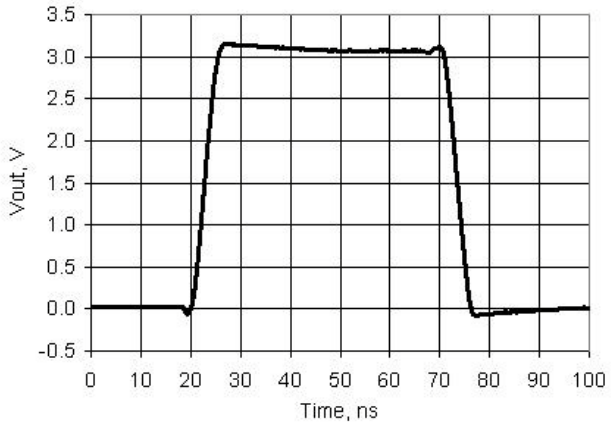


Table 11-12. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	VUSB_5, VUSB_3.3, see	90%	-	111%	
Vcrs	Output signal crossover voltage		1.3	-	2	V

11.5 Analog Peripherals

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-15. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vioff	Input offset voltage	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	±2.5	mV
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	±5.0	mV
TCVos	Input offset voltage drift with temperature	Power mode = high	–	–	±30	µV / °C
Ge1	Gain error, unity gain buffer mode	Rload = 1 kΩ	-	-	±0.1	%
Vi	Input voltage range		Vssa	-	Vdda	mV
Vo	Output voltage range	Output load = 1 mA	Vssa + 50	-	Vdda - 50	mV
Iout	Output current	Output voltage is between Vssa +500 mV and Vdda -500 mV, and Vdda > 2.7 V, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	25	-	-	mA
		Output voltage is between Vssa +500 mV and Vdda -500 mV, and Vdda > 2.7 V, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	20	-	-	mA
Iout	Output current	Output voltage is between Vssa +500 mV and Vdda -500 mV, and Vdda > 1.7 V and Vdda < 2.7 V	16	-	-	mA
I_{DD}	Quiescent current	Power mode = min	–	250	400	µA
		Power mode = low	–	250	400	µA
		Power mode = med	–	330	950	µA
		Power mode = high	–	1000	2500	µA
CMRR	Common mode rejection ratio[30]		80	–	–	dB
PSRR	Power supply rejection ratio	Vdda ≥ 2.7 V	85	–	–	dB
		Vdda < 2.7 V	70	–	–	dB

Figure 11-16. Opamp Voffset Histogram, 3388 samples/847 parts, 25 °C, Vdda = 5 V

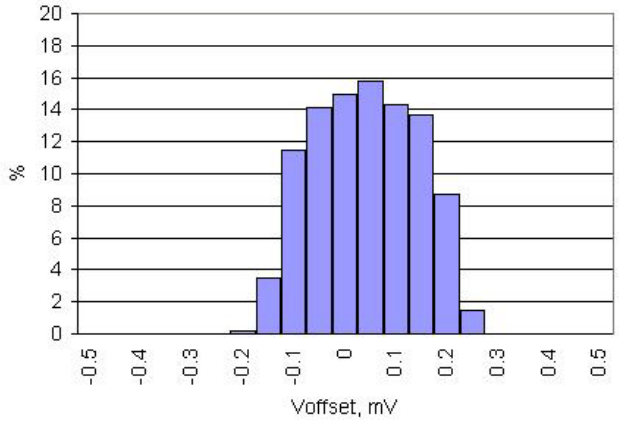


Table 11-23. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 20-bit, External Reference, Differential

Sample rate, sps	Input Voltage Range				
	±VREF	±VREF / 2	±VREF / 4	±VREF / 8	±VREF / 16
8	0.70	0.84	1.02	1.40	2.65
11.3	0.69	0.86	0.96	1.40	2.69
22.5	0.73	0.82	1.25	1.77	2.67
45	0.76	0.94	1.02	1.76	2.75
61	0.75	1.01	1.13	1.65	2.98
170	0.75	0.98	INVALID OPERATING REGION		
187	0.73				

Figure 11-28. Delta-sigma ADC DNL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V

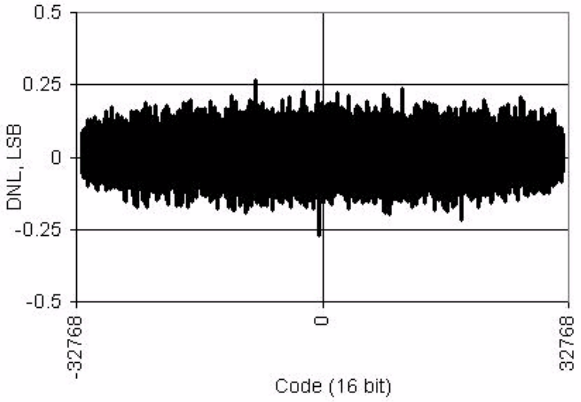
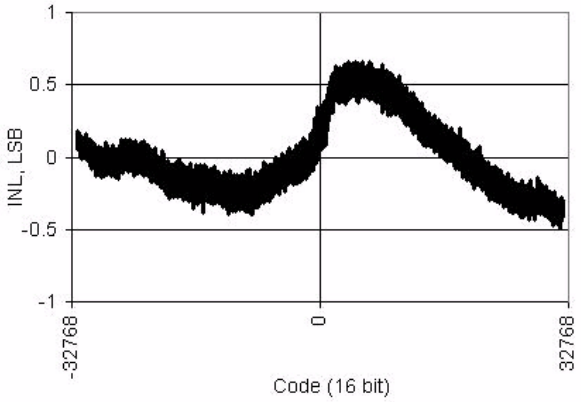


Figure 11-29. Delta-sigma ADC INL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V



11.5.4 Analog Globals

Table 11-25. Analog Globals Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through P2[4], AGL0, DSM INP, AGL1, P2[5][42]	V_{DDA} = 3 V	–	1472	2200	Ω
Rppmuxbus	Resistance pin-to-pin through P2[3], amuxbusL, P2[4][42]	V_{DDA} = 3 V	–	706	1100	Ω

11.5.5 Comparator

Table 11-26. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, Vdda > 2.7 V, Vin ≥ 0.5 V	–		10	mV
	Input offset voltage in slow mode	Factory trim, Vin ≥ 0.5 V	–		9	mV
	Input offset voltage in fast mode[43]	Custom trim	–	–	4	mV
	Input offset voltage in slow mode[43]	Custom trim	–	–	4	mV
	Input offset voltage in ultra low-power mode	V_{DDA} ≤ 4.6 V	–	±12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA}	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low-power mode V_{DDA} ≤ 4.6 V	V_{SSA}	–	V_{DDA} – 1.15	V
CMRR	Common mode rejection ratio		–	50	–	dB
Icmp	High current mode/fast mode[30]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	400	µA
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	600	µA
	Low current mode/slow mode[30]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	100	µA
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	150	µA
	Ultra low power mode[30]	VDDA ≤ 4.6 V	-	6	-	µA

Table 11-27. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode[44]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode[44]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low-power mode[44]	50 mV overdrive, measured pin-to-pin, V_{DDA} ≤ 4.6 V	–	55	–	µs

Note
42. The resistance of the analog global and analog mux bus is high if V_{DDA} ≤ 2.7 V, and the chip is in either sleep or hibernate mode. Use of analog global and analog mux bus under these conditions is not recommended.
43. The recommended procedure for using a custom trim value for the on-chip comparators can be found in the TRM.
44. Based on device characterization (Not production tested).

Figure 11-33. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

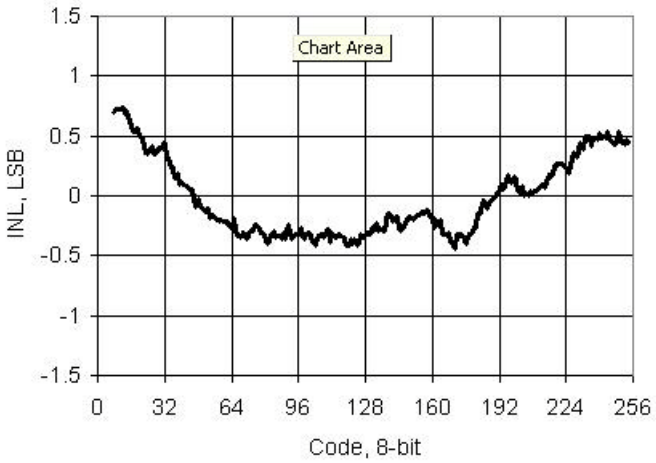


Figure 11-34. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

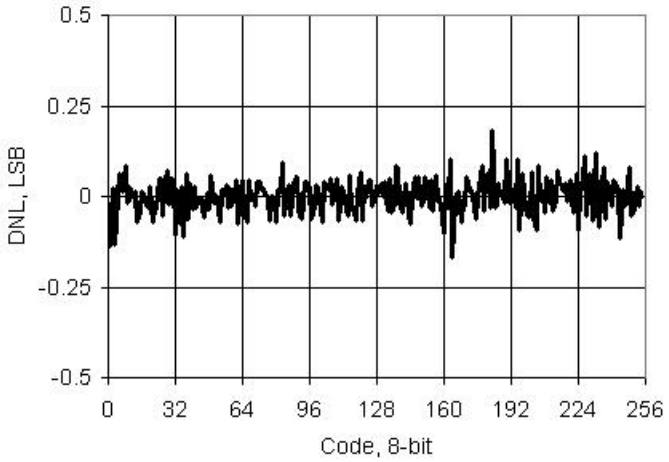


Figure 11-35. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode

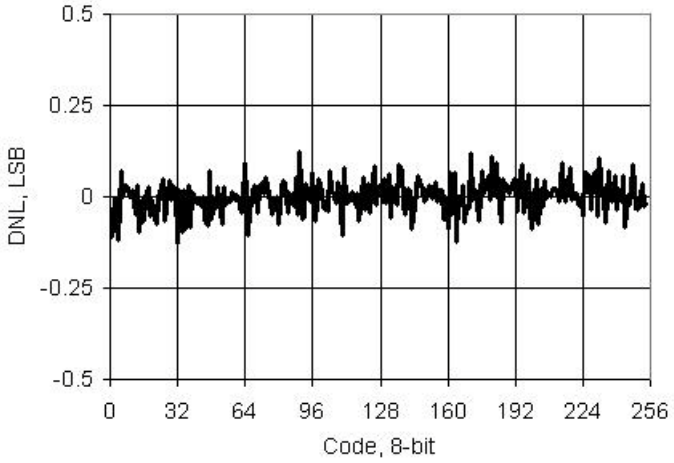


Figure 11-53. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode

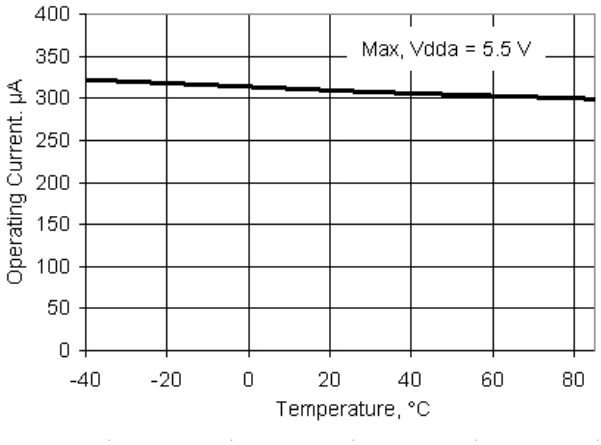
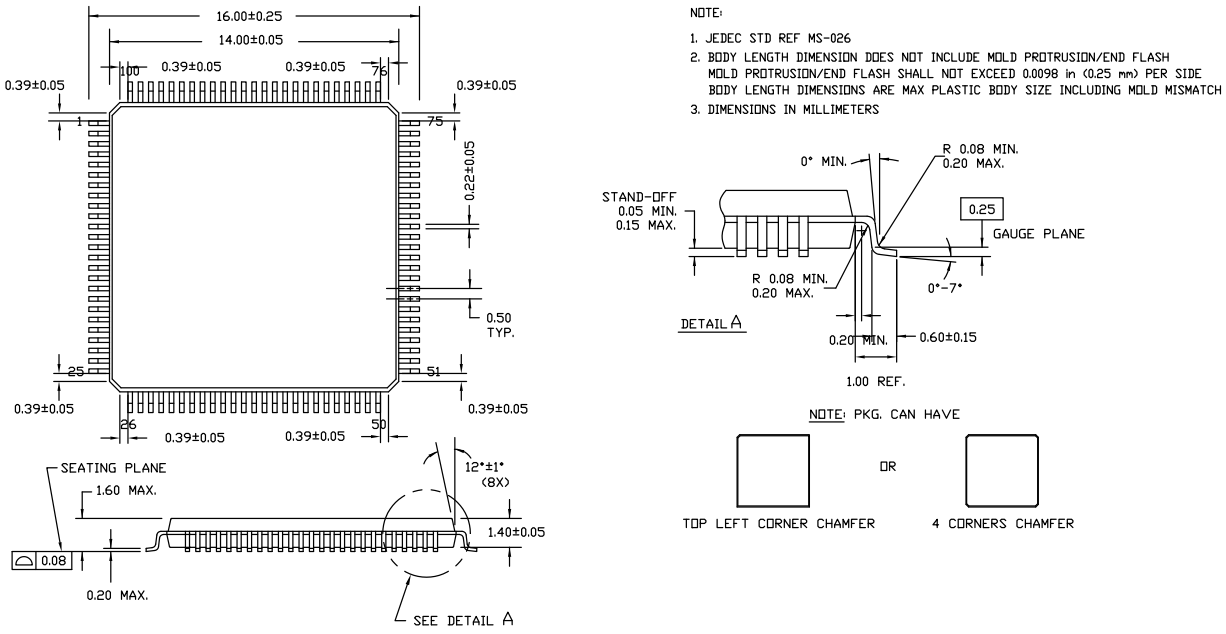


Figure 13-2. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048



51-85048 *I

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts