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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866axa-040

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and SIO provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[13], and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

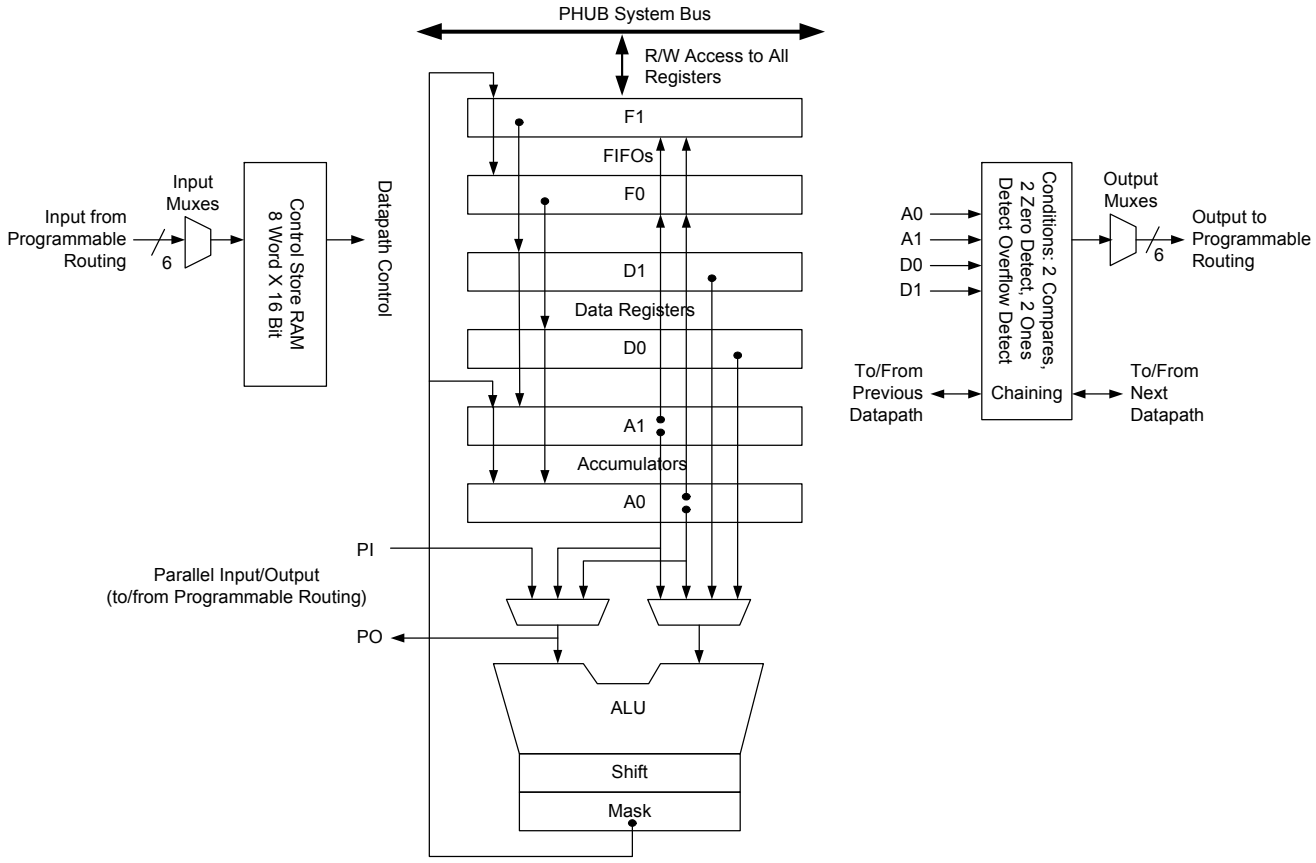
- Features supported by both GPIO and SIO:
  - User programmable port reset state
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins
  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port
  - Slew rate controlled digital output drive mode
  - Access port control and configuration registers on either port basis or pin basis
  - Separate port read (PS) and write (DR) data registers to avoid read modify write errors
  - Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense[13]
  - Analog input and output capability
  - Continuous 100 µA clamp current capability
  - Standard drive strength down to 1.7 V
- Additional features only provided on SIO pins:
  - Higher drive strength than GPIO
  - Hot swap capability (5 V tolerance at any operating V_{DD})
  - Programmable and regulated high input and output drive levels down to 1.2 V
  - No analog input, CapSense, or LCD capability
  - Over voltage tolerance up to 5.5 V
  - SIO can act as a general purpose analog comparator
- USBIO features:
  - Full speed USB 2.0 compliant I/O
  - Highest drive strength for general purpose use
  - Input, output, or both for CPU and DMA
  - Input, output, or both for digital peripherals
  - Digital output (CMOS) drive mode
  - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

Note
13. GPIOs with opamp outputs are not recommended for use with CapSense.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Datapath Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

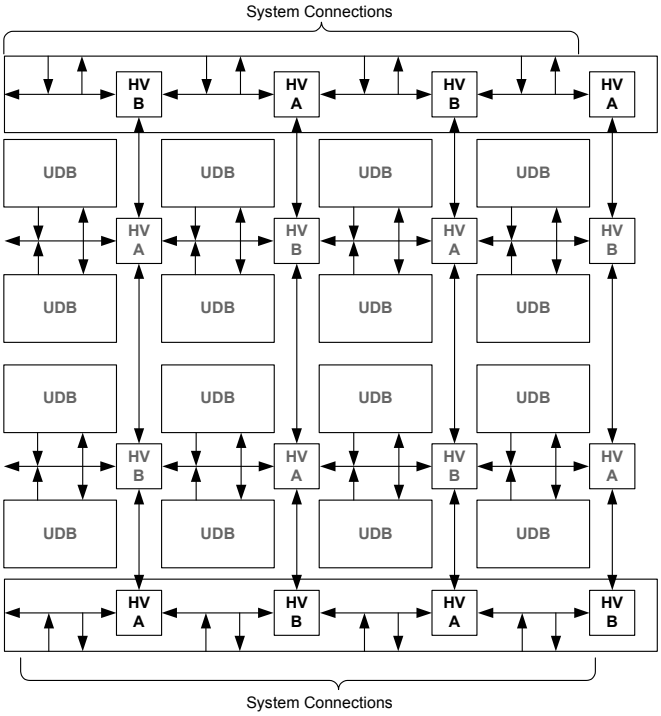
7.2.3.2 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

7.3 UDB Array Description

Figure 7-7 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-7. Digital System Interface Structure

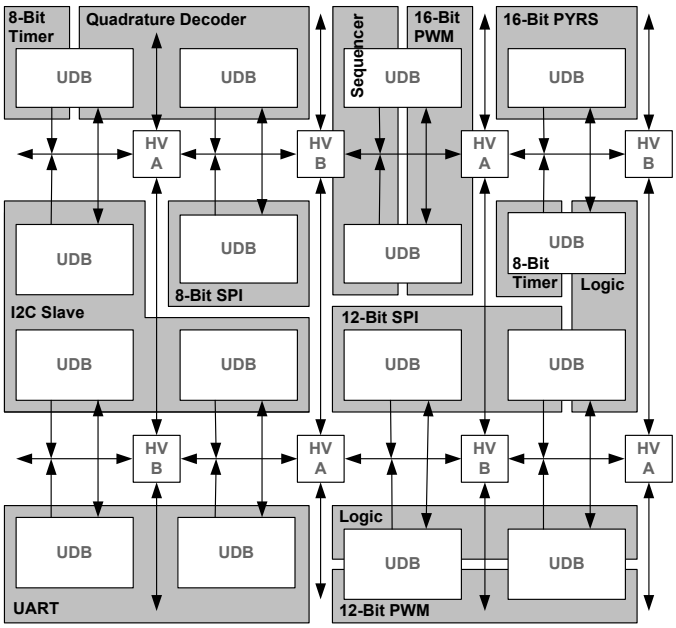


7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-8. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

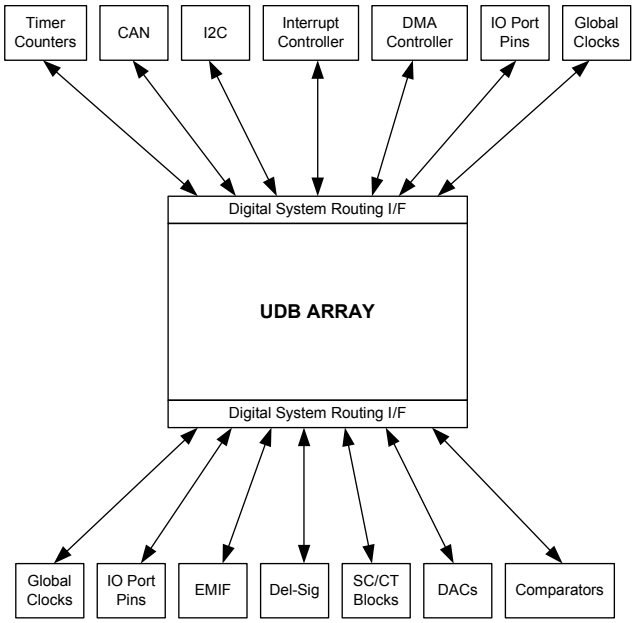
The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

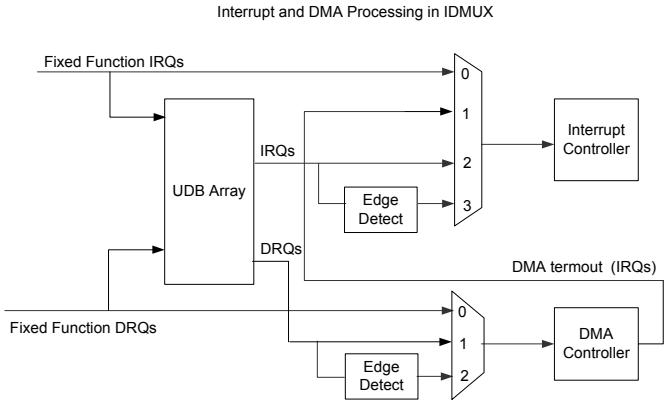
- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

Figure 7-9. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C38 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-10. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the master clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-11. I/O Pin Synchronization Routing

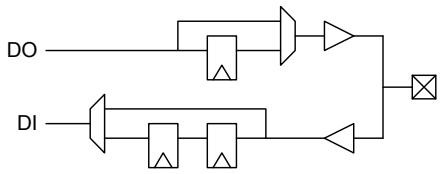
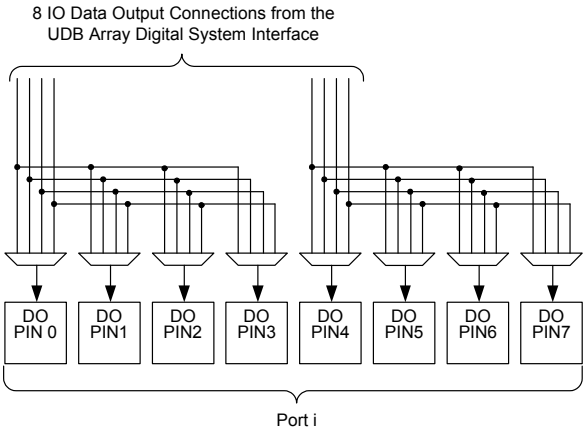
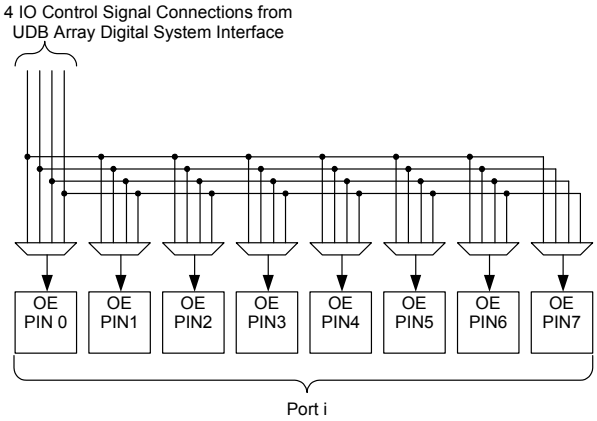


Figure 7-12. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-13. I/O Pin Output Enable Connectivity



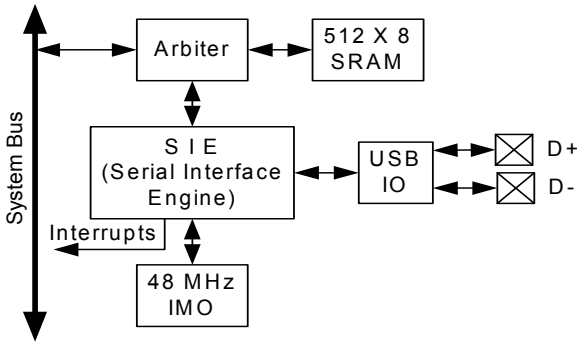
7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 33.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual memory management with no DMA access
  - Manual memory management with manual DMA access
  - Automatic memory management with automatic DMA access
- Internal 3.3-V regulator for transceiver
- Internal 48-MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB reset, suspend, and resume operations
- Bus-powered and self-powered modes

Figure 7-16. USB



7.7 Timers, Counters, and PWMs

The timer/counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in UDBs as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The timer/counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-17. Timer/Counter/PWM

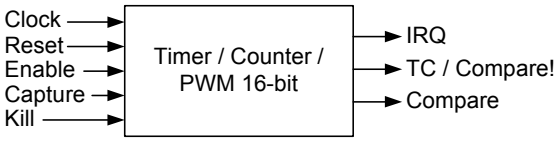
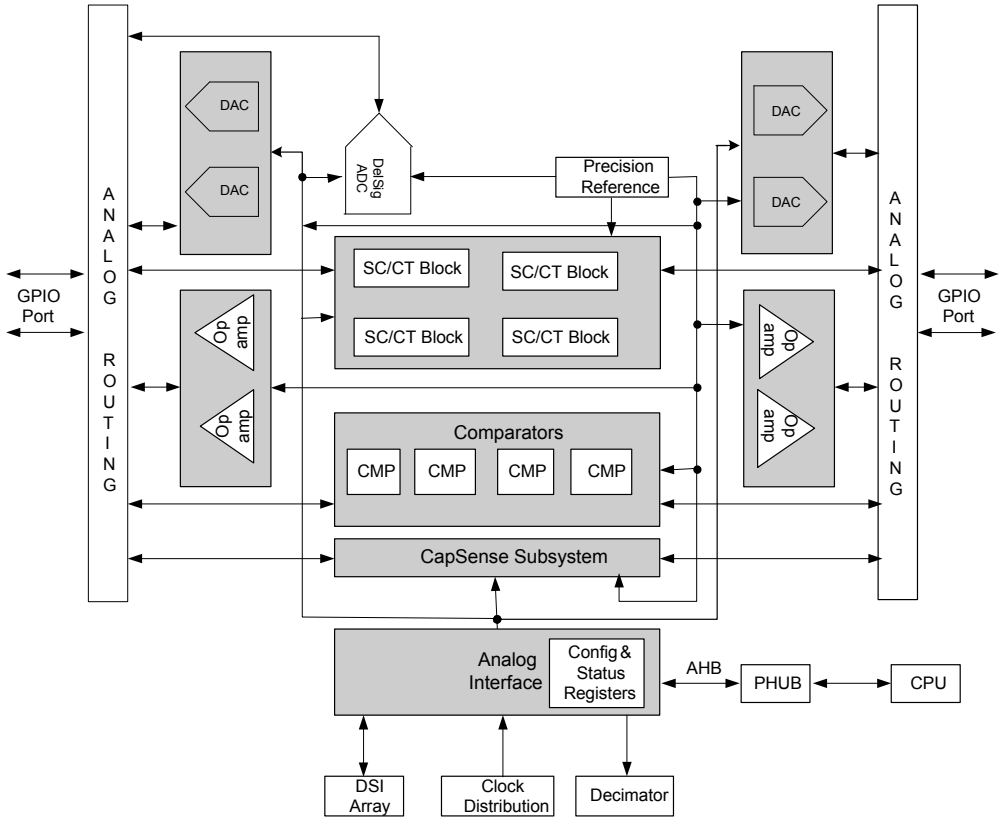


Figure 8-1. Analog Subsystem Block Diagram



The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

8.1 Analog Routing

The CY8C38 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

For information on how to make pin selections for optimal analog routing, refer to the application note, AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs.

8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- Eight analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the CY8C38 family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in CY8C38, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2 on page 53.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ	Max	Units
	Sleep Mode[26]						
	CPU OFF RTC = ON (= ECO32K ON, in low power mode) Sleep timer = ON (= ILO ON at 1 kHz) [27] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V–5.5 V	T = –40 °C	–	1.1	2.3	µA
			T = 25 °C	–	1.1	2.2	µA
			T = 85 °C	–	15	30	µA
			T = 125 °C	–	20.3	30	µA
		$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = –40 °C	–	1	2.2	µA
			T = 25 °C	–	1	2.1	µA
			T = 85 °C	–	12	28	µA
			T = 125 °C	–	18.5	28	µA
		$V_{CC} = V_{DDIO}$ = 1.71 V–1.95 V	T = 25 °C	–	2.2	4.2	µA
			T = 125 °C	–	16.2	28	µA
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I^2C Wake = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = 25 °C	–	2.2	2.7	µA
	I^2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = 25 °C	–	2.2	2.8	µA

Notes
26. If Vccd and Vcca are externally regulated, the voltage difference between Vccd and Vcca must be less than 50 mV.
27. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ	Max	Units
	Hibernate Mode[28]						
	Hibernate mode current All regulators and oscillators off. SRAM retention GPIO interrupts are active SIO Pins in single ended input, unregulated output mode	V_{DD} = V_{DDIO} = 4.5 V–5.5 V	T = –40 °C	–	0.2	1.6	µA
			T = 25 °C	–	0.5	1.5	µA
			T = 85 °C	–	4.1	5.3	µA
			T = 125 °C	–	6.3	10	µA
		V_{DD} = V_{DDIO} = 2.7 V–3.6 V	T = –40 °C	–	0.2	1.5	µA
			T = 25 °C	–	0.2	1.5	µA
			T = 85 °C	–	3.2	4.2	µA
			T = 125 °C	–	6	10	µA
		V_{CC} = V_{DDIO} = 1.71 V–1.95 V	T = –40 °C	–	0.2	1.5	µA
			T = 25 °C	–	0.2	1.5	µA
			T = 85 °C	–	2.8	4.3	µA
			T = 125 °C	–	5.4	10	µA
I_{DDAR}	Analog current consumption while device is reset [29]	$V_{DDA} \leq 3.6$ V		–	0.3	1	mA
		$V_{DDA} > 3.6$ V		–	1.4	3.3	mA
I_{DDDR}	Digital current consumption while device is reset [29]	$V_{DDD} \leq 3.6$ V		–	1.1	6	mA
		$V_{DDD} > 3.6$ V		–	0.7	6	mA
I_{IB}	Input bias current [29]		T = 25 °C	–	10	–	pA

Notes
28. If Vccd and Vcca are externally regulated, the voltage difference between Vccd and Vcca must be less than 50 mV.
29. Based on device characterization (not production tested). USBIO pins tied to ground (V_{SSD}).

Figure 11-20. Opamp Operating Current vs Vdda and Power Mode

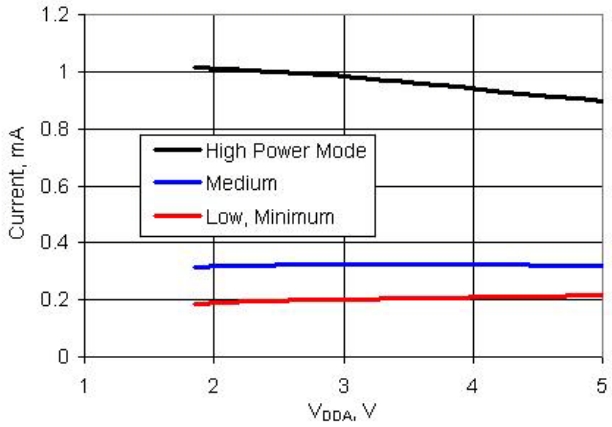


Table 11-16. Opamp AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 15 pF load	1	–	–	MHz
		Power mode = low, 15 pF load	2	–	–	MHz
		Power mode = medium, 200 pF load	1	–	–	MHz
		Power mode = high, 200 pF load	2.5	–	–	MHz
SR	Slew rate, 20% - 80%	Power mode = low, 15 pF load	1.1	–	–	V/µs
		Power mode = medium, 200 pF load	0.9	–	–	V/µs
		Power mode = high, 200 pF load	3	–	–	V/µs
e_n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	45	–	nV/sqrtHz

Figure 11-21. Opamp Noise vs Frequency, Power Mode = High, Vdda = 5 V

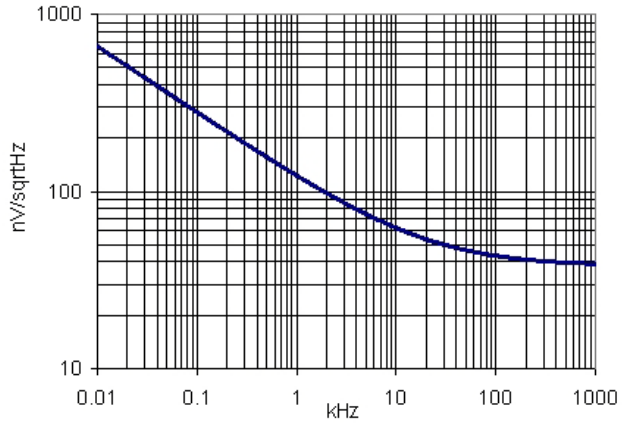


Table 11-17. 20-bit Delta-sigma ADC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC16	ADC input resistance	Input buffer bypassed, 16-bit, Range = ±1.024 V	–	74[37]	–	kΩ
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = ±1.024 V	–	148[37]	–	kΩ
Vextref	ADC external reference input voltage	Pins P0[3], P3[2]	0.9	–	1.3	V
Current Consumption						
I_{DD_20}	I_{DDD} + I_{DDA} Current consumption, 20 bit [38]	187 sps, unbuffered	–	–	1.5	mA
I_{DD_16}	I_{DDD} + I_{DDA} Current consumption, 16 bit [38]	48 ksps, unbuffered	–	–	1.5	mA
I_{DD_12}	I_{DDD} + I_{DDA} Current consumption, 12 bit [38]	192 ksps, unbuffered	–	–	1.95	mA
I_{BUFF}	Buffer current consumption[38]		–	–	2.5	mA

Notes
37. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.
38. Based on device characterization (Not production tested).

Figure 11-27. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

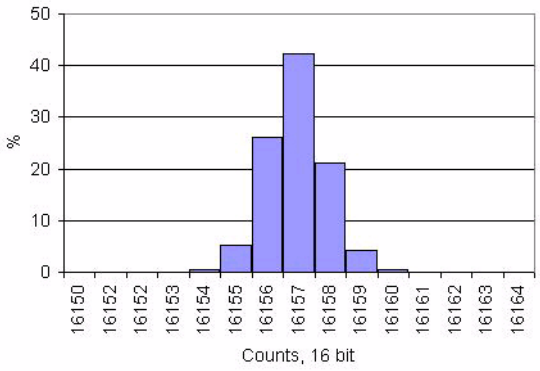


Table 11-20. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 16-bit, Internal Reference, Single Ended

Sample rate, sps	Input Voltage Range			
	0 to VREF	0 to VREF x 2	VSSA to VDDA	0 to VREF x 6
2000	1.21	1.02	1.14	0.99
3000	1.28	1.15	1.25	1.22
6000	1.36	1.22	1.38	1.22
12000	1.44	1.33	1.43	1.40
24000	1.67	1.50	1.43	1.53
48000	1.91	1.60	1.85	1.67

Table 11-21. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 16-bit, Internal Reference, Differential

Sample rate, sps	Input Voltage Range				
	±VREF	±VREF / 2	±VREF / 4	±VREF / 8	±VREF / 16
2000	0.56	0.65	0.74	1.02	1.77
4000	0.58	0.72	0.81	1.10	1.98
8000	0.53	0.72	0.82	1.12	2.18
15625	0.58	0.72	0.85	1.13	2.20
32000	0.60	0.76	INVALID OPERATING REGION		
43750	0.58	0.75			
48000	0.59				

Table 11-22. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 20-bit, External Reference, Single Ended

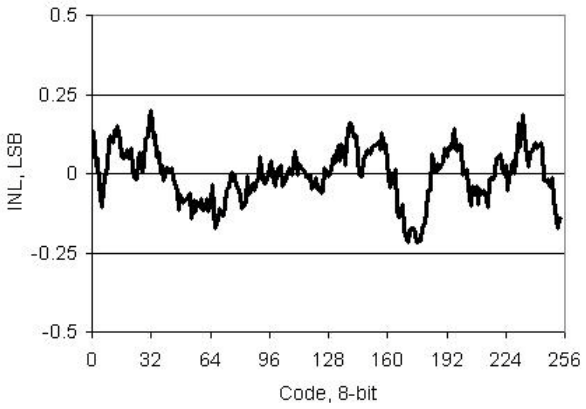
Sample rate, sps	Input Voltage Range			
	0 to VREF	0 to VREF x 2	VSSA to VDDA	0 to VREF x 6
8	1.28	1.24	6.02	0.97
23	1.33	1.28	6.09	0.98
45	1.77	1.26	6.28	0.96
90	1.65	0.91	6.84	0.95
187	1.87	1.06	7.97	1.01

11.5.7 VDAC

Table 11-30. VDAC (Voltage Digital-to-Analog Converter) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Resolution			-	8	-	
Rout	Output resistance[30]					
	High	Vout = 4 V	-	16	-	kΩ
	Low	Vout = 1 V	-	4	-	kΩ
Vout	Output voltage range, code = 255	1 V scale	–	1.02	–	V
		4 V scale, Vdda = 5 V	–	4.08	–	V
INL	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
DNL	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
	Monotonicity		–	–	Yes	–
Eg	Gain error	1 V scale,	–	–	±2.5	%
		4 V scale	–	–	±2.5	%
TC_Eg	Temperature coefficient, gain error	1 V scale,	–	–	0.03	%FSR / °C
		4 V scale	–	–	0.03	%FSR / °C
VDAC_ICC	Operating current	Low speed mode	–	–	100	µA
		High speed mode	–	–	500	µA
V_{OS}	Zero scale error		–	0	±0.9	LSB

Figure 11-46. VDAC INL vs Input Code, 1 V Mode



11.5.12 LCD Direct Drive

Table 11-39. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 Mhz, Vddio = Vdda = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	µA
I_{CC_SEG}	Current per segment driver	Strong drive mode	–	260	–	µA
V_{BIAS}	LCD bias range (V_{BIAS} refers to the main output voltage(V0) of LCD DAC)	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	2	–	5	V
	LCD bias step size	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	–	9.1 × V_{DDA}	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I_{OUT}	Output drive current per segment driver)	Vddio = 5.5V, strong drive mode	355	–	710	µA

Table 11-40. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LCD}	LCD frame rate		10	50	150	Hz

11.7 Memory

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-55. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	Vddd pin	1.71	-	5.5	V

Table 11-56. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Twrite	Block write time (erase + program)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	15	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	15	ms
Terase	Block erase time	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	10	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	10	ms
	Block program time	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	5	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	5	ms
Tbulk	Bulk erase time (16 KB to 64 KB)[53]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	35	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	35	ms
	Sector erase time (8 KB to 16 KB)[53]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	15	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	15	ms
	Total device program time (including JTAG, etc.)	No overhead [54]	-	-	5	seconds
	Flash data retention time [55]	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Retention period measured from last erase cycle after 100k progra/erase cycles at T_A ≤ 85 °C	10	–	–	

Notes
53. ECC not included.
54. See PSoC® 3 Device Programming Specifications for a description of a low-overhead method of programming PSoC 3 flash. (Please take care of Foot note numbers)
55. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +125 °C ambient temperature range. Contact customercare@cypress.com.

11.7.2 EEPROM

Table 11-57. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	-	5.5	V

Table 11-58. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	2	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, $T_A \leq 25$ °C, 1M erase/program cycles	20	–	–	years
		Average ambient temp, $T_A \leq 55$ °C, 100 K erase/program cycles	20	–	–	
		Average ambient temp. $T_A \leq 85$ °C, 10 K erase/program cycles	10	–	–	

11.7.3 Nonvolatile Latches (NVL)

Table 11-59. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	Vddd pin	1.71	-	5.5	V

Table 11-60. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25°C	1K	-	-	program/ erase cycles
		Programmed at 0-70°C	100	-	-	program/ erase cycles
	NVL data retention time	Programmed at 55°C	20	-	-	years
		Programmed at 0-70°C	10	-	-	years

11.7.4 SRAM

Table 11-61. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vsram	SRAM retention voltage		1.2	-	-	V

Table 11-62. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsram	SRAM operating frequency	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	DC	-	67	MHz
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	DC	-	50	MHz

Figure 11-63. Synchronous Read Cycle Timing

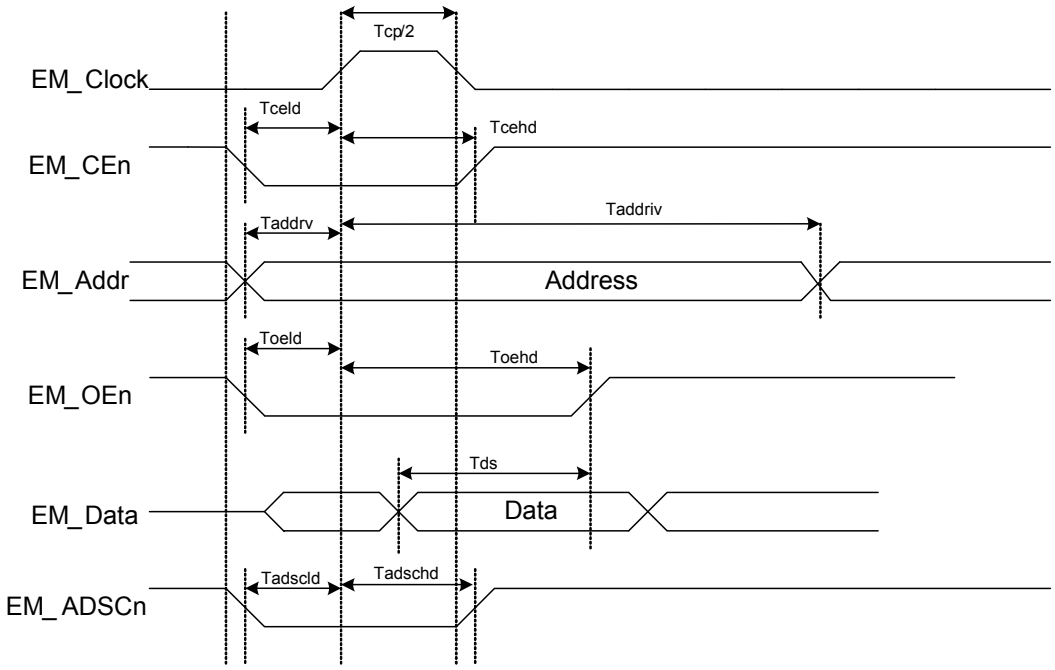


Table 11-65. Synchronous Read Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock period[57]	Vdda ≥ 3.3 V	30.3	–	–	ns
Tcp/2	EM_Clock pulse high		T/2	–	–	ns
Tceld	EM_CEn low to EM_Clock high		5	–	–	ns
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	–	–	ns
Taddrv	EM_Addr valid to EM_Clock high		5	–	–	ns
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	ns
Toeld	EM_OEn low to EM_Clock high		5	–	–	ns
Toehd	EM_Clock high to EM_OEn high		T	–	–	ns
Tds	Data valid before EM_OEn high		T + 15	–	–	ns
Tadscld	EM_ADSCn low to EM_Clock high		5	–	–	ns
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	ns

Note
57. Limited by GPIO output frequency, see .

11.8 PSoC System Resources

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.8.1 POR with Brown Out

For brown out detect in regulated mode, Vddd and Vdda must be ≥ 2.0 V. Brown out detect is available in externally regulated mode.

Table 11-67. Precise Power On Reset (PRES) with Brown Out DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

Table 11-68. Precise Power On Reset (PRES) with Brown Out AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR	Response time		–	–	0.5	µs
	V_{DDD}/V_{DDA} droop rate	Sleep mode	–	5	–	V/sec

11.8.2 Voltage Monitors

Table 11-69. Voltage Monitors DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-70. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Response time[59]		–	–	1	µs

Note
59. Based on device characterization (Not production tested).

11.9.2 Internal Low Speed Oscillator

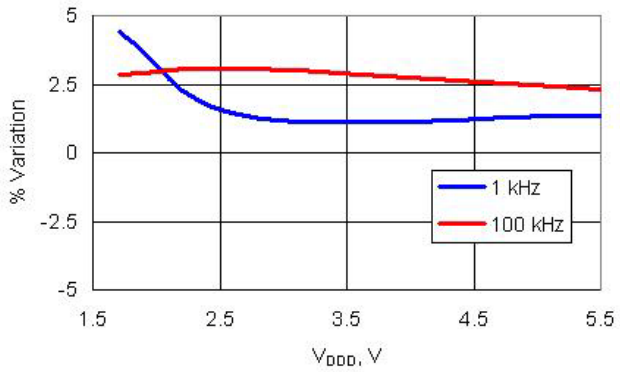
Table 11-77. ILO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[64]	F_{OUT} = 1 kHz	–	–	1.7	µA
		F_{OUT} = 33 kHz	–	–	2.6	µA
		F_{OUT} = 100 kHz	–	–	2.6	µA
	Leakage current[64]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	2.0	15	nA
		Power down mode				
	Leakage current[64]	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	200	nA
		Power down mode				

Table 11-78. ILO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time	Turbo mode	-	-	2	ms
Filo	ILO frequencies (trimmed)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C				
	100 kHz		45	100	200	kHz
	1 kHz		0.5	1	2	kHz
	ILO frequencies (untrimmed)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C				
	100 kHz		30	100	300	kHz
	1 kHz		0.3	1	3.5	kHz
Filo	ILO frequencies (trimmed)	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C				
	100 kHz		45	-	450	kHz
	1 kHz		0.5	-	5	kHz
	ILO frequencies (untrimmed)	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C				
	100 kHz		150	-	500	kHz
	1 kHz		0.3	-	6.5	kHz

Figure 11-70. ILO Frequency Variation vs. V_{DD}



Note
64. This value is calculated, not measured.
65. Based on device characterization (Not production tested).

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

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