Infineon Technologies - CY8C3866AXA-055 Datasheet

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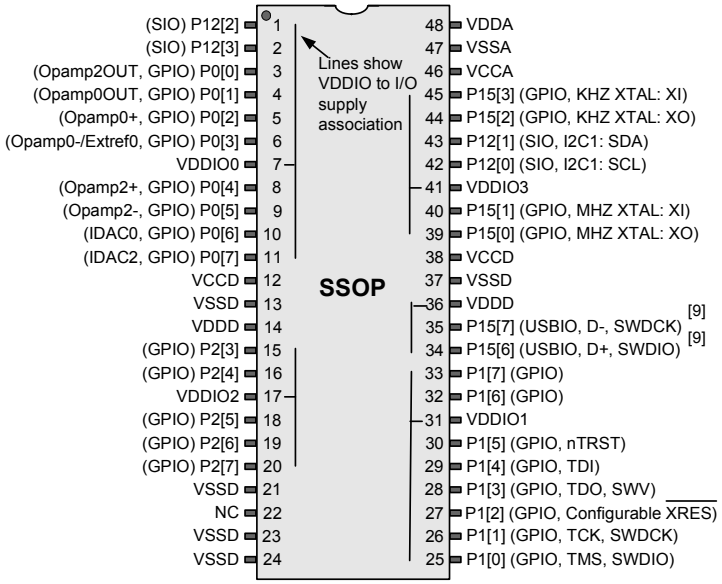
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866axa-055

Figure 2-3. 48-pin SSOP Part Pinout



Note
9. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

■ Program branching instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. Table 4-1 lists the different arithmetic instructions.

Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase ‘subchains’ can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

Figure 4-2 on page 18 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 19 shows the interrupt structure and priority polling.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I^2C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	DFB Int	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

7. Digital Subsystem

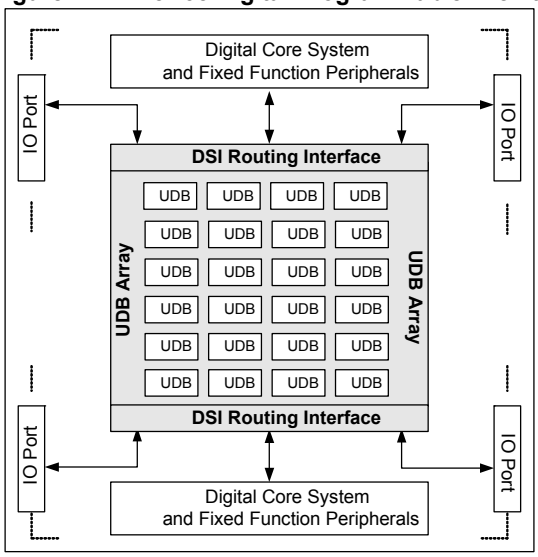
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- UDB – These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal digital block array – UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital system interconnect (DSI) – Digital signals from UDBs, fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the digital system interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the universal digital block array.

Figure 7-1. CY8C38 Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C38 family's UDBs and analog blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the data sheet, and the list is always growing. An example of a component available for use in CY8C38 family, but, not explicitly called out in this data sheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C38 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Communications
  - I^2C
  - UART
  - SPI
- Functions
  - EMIF
  - PWMs
  - Timers
  - Counters
- Logic
  - NOT
  - OR
  - XOR
  - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C38 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

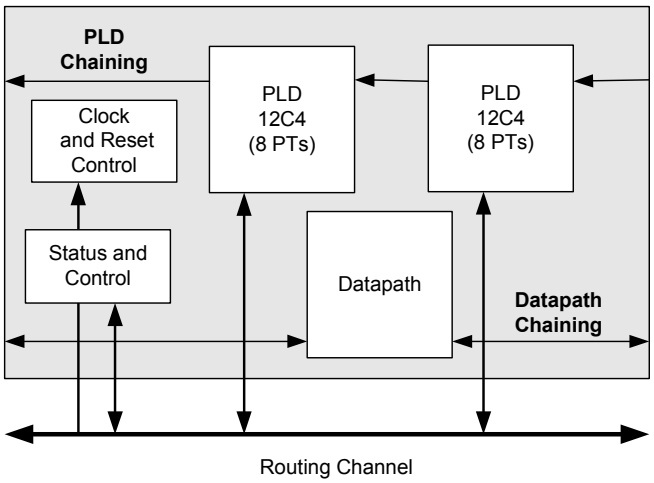
- Amplifiers
  - TIA
  - PGA
  - opamp
- ADC
  - Delta-sigma
- DACs
  - Current
  - Voltage
  - PWM
- Comparators
- Mixers

7.2 Universal Digital Block

The UDB represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



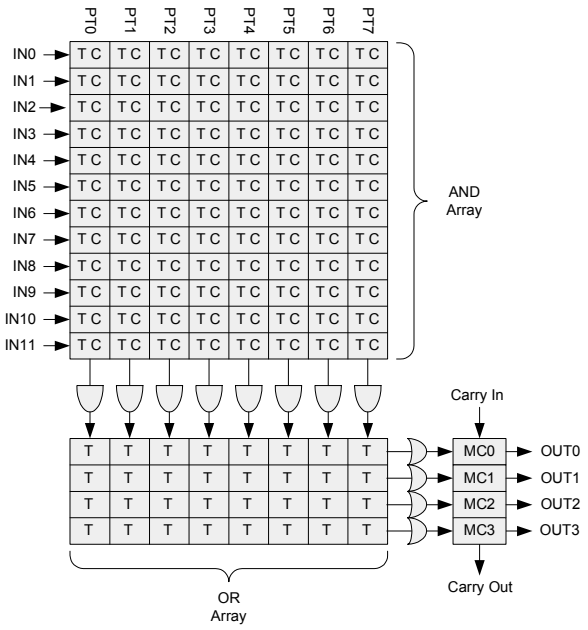
The main component blocks of the UDB are:

- PLD blocks – There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath module – This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and control module – The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and reset module – This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

7.8 I²C

The I²C peripheral provides a synchronous two wire interface designed to interface the PSoC device with a two wire I²C serial communication bus. It is compatible[16] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I2C-bus specification and user manual (UM10204). The I2C bus I/O may be implemented with GPIO or SIO in open-drain modes. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master).[17]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through DSI routing and allows direct connections to any GPIO or SIO pins.

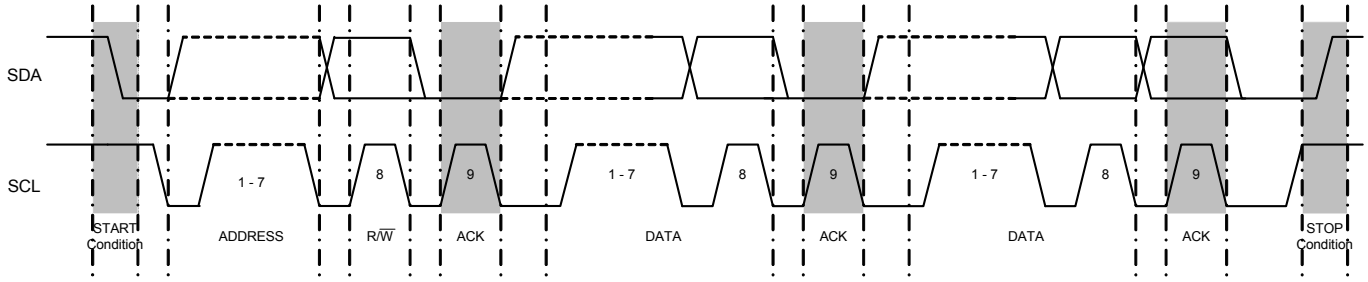
I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup functionality is required, I²C pin connections are limited to the two special sets of SIO pins.

I²C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in Figure 7-18. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

Figure 7-18. I²C Complete Transfer Timing



Notes

16. The I²C peripheral is non-compliant with the NXP I²C specification in the following areas: analog glitch filter, I/O V_{OL}/I_{OL}, I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 74 for details.
17. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

8.2.2.4 Multi Sample (Turbo)

The multi sample (turbo) mode operates identical to the Multi-sample mode for resolutions of 8 to 16 bits. For resolutions of 17 to 20 bits, the performance is about four times faster than the multi sample mode, because the ADC is only reset once at the end of conversion.

More information on output formats is provided in the Technical Reference Manual.

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

8.3 Comparators

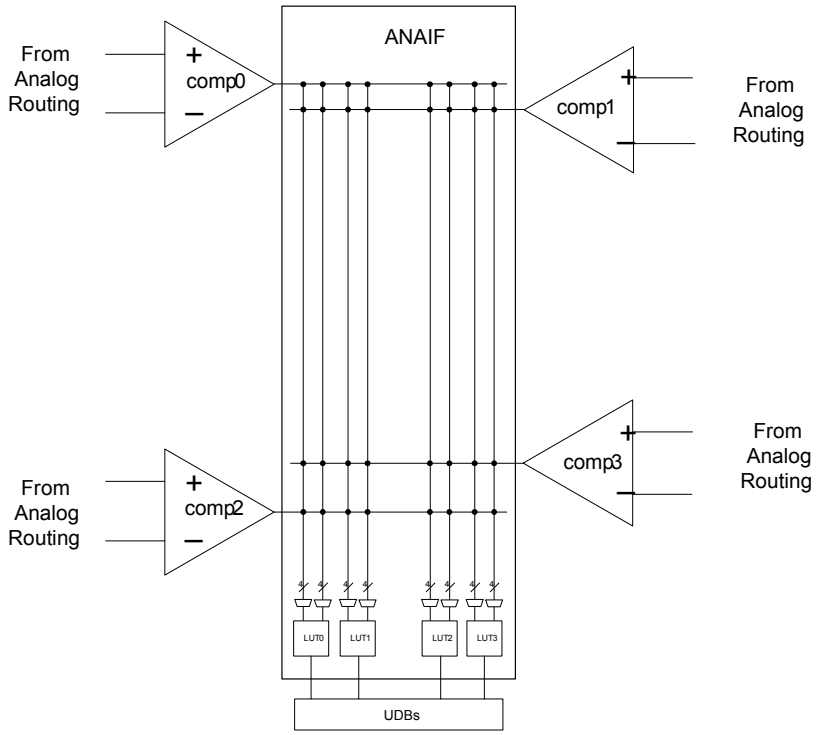
The CY8C38 family of devices contains four comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (VSSA to VDDA)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB DSI.

Figure 8-5. Analog Comparator



11.2 Device Level Specifications

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 11-2. DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled	1.8	–	5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled	1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled	1.8	–	V_{DDA}[22]	V
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled	1.71	1.8	1.89	V
V_{DDIO}[23]	I/O supply voltage relative to V_{SSIO}		1.71	–	V_{DDA}[22]	V
V_{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled	1.71	1.8	1.89	V
V_{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled	1.71	1.8	1.89	V

Notes
22. V_{DDX} = 3.3 V.
23. Based on device specifications (not production tested).

Table 11-7. GPIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode[30]	3 V Vddio Cload = 25 pF	–	–	12	ns
TfallF	Fall time in Fast Strong Mode[30]	3 V Vddio Cload = 25 pF	–	–	12	ns
TriseS	Rise time in Slow Strong Mode[30]	3 V Vddio Cload = 25 pF	–	–	60	ns
TfallS	Fall time in Slow Strong Mode[30]	3 V Vddio Cload = 25 pF	–	–	60	ns
Fgpioout	GPIO output operating frequency					
	3 V ≤ Vddio ≤ 5.5 V, fast strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	33	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	24	MHz
	1.71 V ≤ Vddio < 3 V, fast strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	20	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	16	MHz
	3 V ≤ Vddio ≤ 5.5 V, slow strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	7	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	7	MHz
	1.71 V ≤ Vddio < 3 V, slow strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	3.5	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	3.5	MHz
Fgpioin	GPIO input operating frequency					
	1.71 V ≤ Vddio ≤ 5.5 V	90/10% better than 60/40 duty cycle, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	66	MHz
		90/10% better than 60/40 duty cycle, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	50	MHz

Figure 11-24. Delta-sigma ADC IDD vs sps, Range = ±1.024 V, Continuous Sample Mode, Input Buffer Bypassed

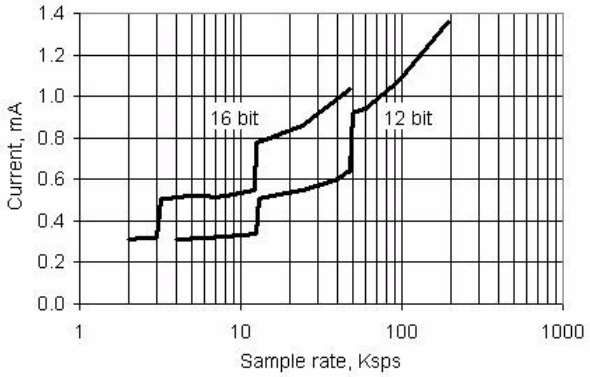


Figure 11-25. Delta-sigma ADC Noise Histogram, 1000 Samples, 20-Bit, 187 sps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

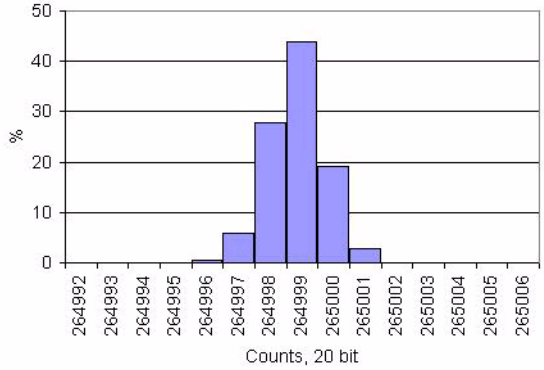


Figure 11-26. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

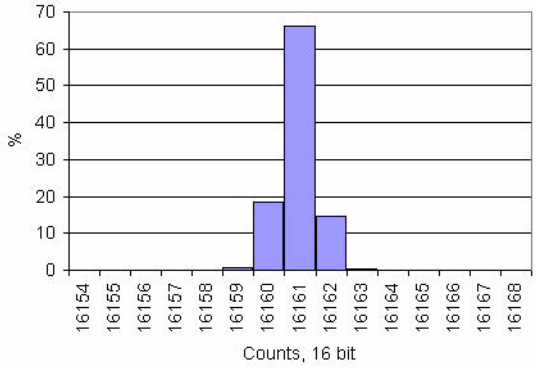


Table 11-28. IDAC (Current Digital-to-Analog Converter) DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Low speed mode, source mode, range = 31.875 µA	–	44	100	µA
		Low speed mode, source mode, range = 255 µA,	–	33	100	µA
		Low speed mode, source mode, range = 2.04 mA	–	33	100	µA
		Low speed mode, sink mode, range = 31.875 µA	–	36	100	µA
		Low speed mode, sink mode, range = 255 µA	–	33	100	µA
		Low speed mode, sink mode, range = 2.04 mA	–	33	100	µA
		High speed mode, source mode, range = 31.875 µA	–	310	500	µA
		High speed mode, source mode, range = 255 µA	–	305	500	µA
		High speed mode, source mode, range = 2.04 mA	–	305	500	µA
		High speed mode, sink mode, range = 31.875 µA	–	310	500	µA
		High speed mode, sink mode, range = 255 µA	–	300	500	µA
		High speed mode, sink mode, range = 2.04 mA	–	300	500	µA

Figure 11-32. IDAC INL vs Input Code, Range = 255 µA, Source Mode

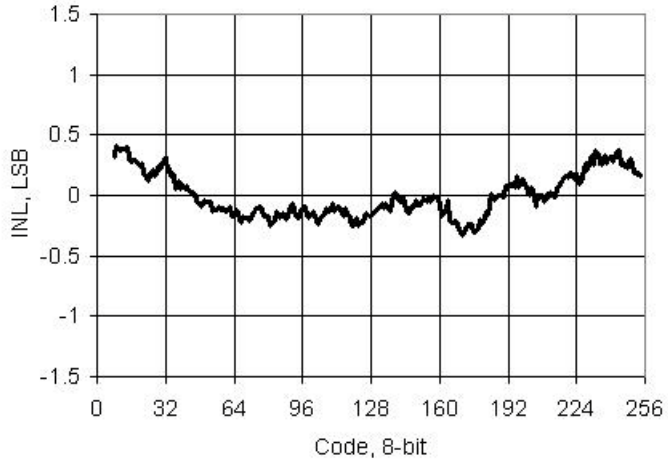


Table 11-29. IDAC (Current Digital-to-Analog Converter) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fdac	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, High speed mode, Vdda = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-42. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V

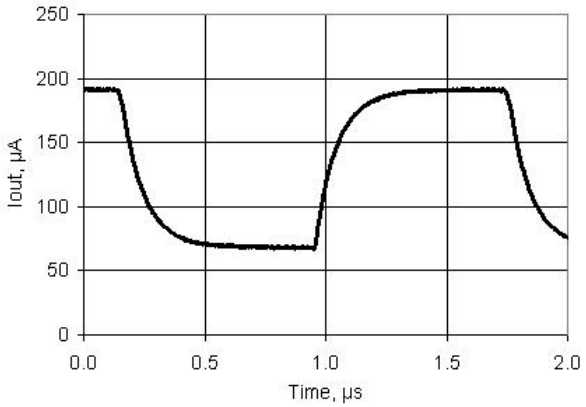
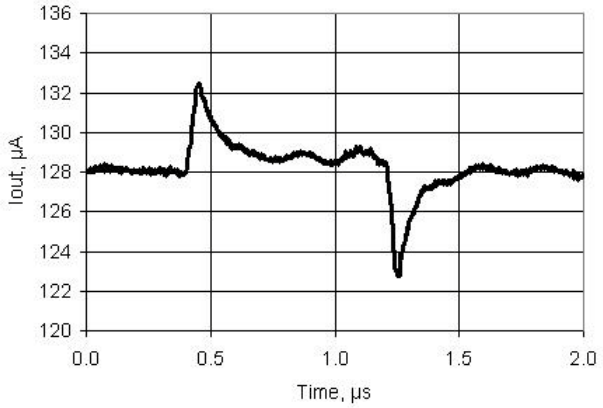


Figure 11-43. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V

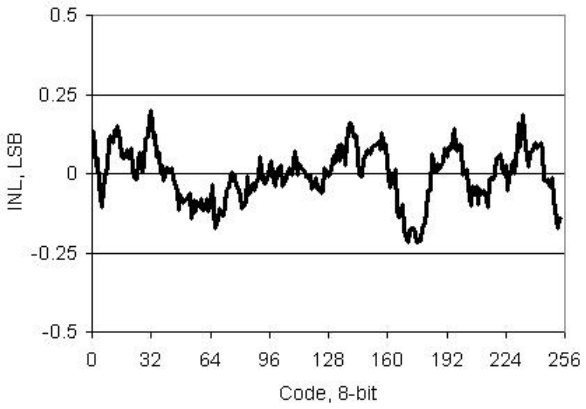


11.5.7 VDAC

Table 11-30. VDAC (Voltage Digital-to-Analog Converter) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Resolution			-	8	-	
Rout	Output resistance[30]					
	High	Vout = 4 V	-	16	-	kΩ
	Low	Vout = 1 V	-	4	-	kΩ
Vout	Output voltage range, code = 255	1 V scale	–	1.02	–	V
		4 V scale, Vdda = 5 V	–	4.08	–	V
INL	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
DNL	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
	Monotonicity		–	–	Yes	–
Eg	Gain error	1 V scale,	–	–	±2.5	%
		4 V scale	–	–	±2.5	%
TC_Eg	Temperature coefficient, gain error	1 V scale,	–	–	0.03	%FSR / °C
		4 V scale	–	–	0.03	%FSR / °C
VDAC_ICC	Operating current	Low speed mode	–	–	100	µA
		High speed mode	–	–	500	µA
V_{OS}	Zero scale error		–	0	±0.9	LSB

Figure 11-46. VDAC INL vs Input Code, 1 V Mode



11.5.9 Transimpedance Amplifier

The TIA is created using a SC/CT Analog Block, see the TIA component data sheet in PSoC Creator for full AC/DC specifications, and APIs and example code.

Table 11-34. Transimpedance Amplifier (TIA) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vioff	Input offset voltage		-	-	10	mV
Rconv	Conversion resistance[46]					
	R = 20K	40 pF load	-25	-	+35	%
	R = 30K	40 pF load	-25	-	+35	%
	R = 40K	40 pF load	-25	-	+35	%
	R = 80K	40 pF load	-25	-	+35	%
	R = 120K	40 pF load	-25	-	+35	%
	R = 250K	40 pF load	-25	-	+35	%
	R= 500K	40 pF load	-25	-	+35	%
	R = 1M	40 pF load	-25	-	+35	%
	Quiescent current		–	1.1	2	mA

Table 11-35. Transimpedance Amplifier (TIA) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW	Input bandwidth (–3 dB)	R = 20K; –40 pF load	1000	–	–	kHz
		R = 120K; –40 pF load	220	–	–	kHz
		R = 1M; –40 pF load	25	–	–	kHz

Note
46. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component data sheets. External precision resistors can also be used.

11.6.4 I^2C

Table 11-47. Fixed I^2C DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	Enabled, configured for 100 kbps	–	–	250	µA
	–	Enabled, configured for 400 kbps	–	–	260	µA
	–	Wake from sleep mode	–	–	30	µA

Table 11-48. Fixed I^2C AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		-	-	1	Mbps

11.6.5 Controller Area Network[50]

Table 11-49. CAN DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	500 kbps	-	-	285	µA
		1 Mbps	-	-	330	µA

Table 11-50. CAN AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate	Minimum 8 MHz clock	-	-	1	Mbit

11.6.6 Digital Filter Block

Table 11-51. DFB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	DFB operating current	64-tap FIR at Fdfb				
		500 kHz (6.7 ksps)	-	0.16	0.27	mA
		1 MHz (13.4 ksps)	-	0.33	0.53	mA
		10 MHz (134 ksps)	-	3.3	5.3	mA
		50 MHz (644 ksps)	-	15.7	25.5	mA
		67 MHz (900 ksps)[51]	-	21.8	35.6	mA

Table 11-52. DFB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fdfb	DFB operating frequency	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	DC	-	67 [51]	MHz
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	DC	-	50 [51]	MHz

Note
50. Refer to ISO 11898 specification for details.
51. Applicable at -40°C to 85°C; 50 MHz at -40°C to 125°C.

11.7.2 EEPROM

Table 11-57. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	-	5.5	V

Table 11-58. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	2	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, $T_A \leq 25$ °C, 1M erase/program cycles	20	–	–	years
		Average ambient temp, $T_A \leq 55$ °C, 100 K erase/program cycles	20	–	–	
		Average ambient temp. $T_A \leq 85$ °C, 10 K erase/program cycles	10	–	–	

11.7.3 Nonvolatile Latches (NVL)

Table 11-59. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	Vddd pin	1.71	-	5.5	V

Table 11-60. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25°C	1K	-	-	program/ erase cycles
		Programmed at 0-70°C	100	-	-	program/ erase cycles
	NVL data retention time	Programmed at 55°C	20	-	-	years
		Programmed at 0-70°C	10	-	-	years

11.7.4 SRAM

Table 11-61. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vsram	SRAM retention voltage		1.2	-	-	V

Table 11-62. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsram	SRAM operating frequency	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	DC	-	67	MHz
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	DC	-	50	MHz

11.9.3 External Crystal Oscillator

Table 11-79. 32 kHz External Crystal DC Specifications[66]

Parameter	Description	Conditions	Min	Typ	Max	Units
Icc	Operating current	Low power mode; C_L = 6 pF; -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	–	0.25	1.0	µA
DL	Drive level	Low-power mode; C_L = 6 pF	–	–	1	µW

Table 11-80. 32 kHz External Crystal AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
Ton	Startup time	High power mode	–	1	–	s

Table 11-81. MHz ECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency range		4	–	25	MHz

11.9.4 External Clock Reference

Table 11-82. External Clock Reference AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at V_{DDIO}/2	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.51	–	–	V/ns

11.9.5 Phase-Locked Loop

Table 11-83. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-84. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[67]	Output of Prescalar	1	-	48	MHz
	PLL intermediate frequency[68]		1	-	3	MHz
Fpllout	PLL output frequency[67]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	24	-	67	MHz
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	24	-	50	MHz
	Lock time at startup		-	-	250	µs
Jperiod-rms	Jitter (rms)[30]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	250	ps
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	400	ps

Notes
66. Based on device characterization (not production tested).
67. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
68. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C38 device includes: a precision on-chip voltage reference, precision oscillators, Flash, ECC, DMA, a fixed function I^2C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and Analog Subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C38 derivatives incorporate device and Flash security in user-selectable security levels; see TRM for details.

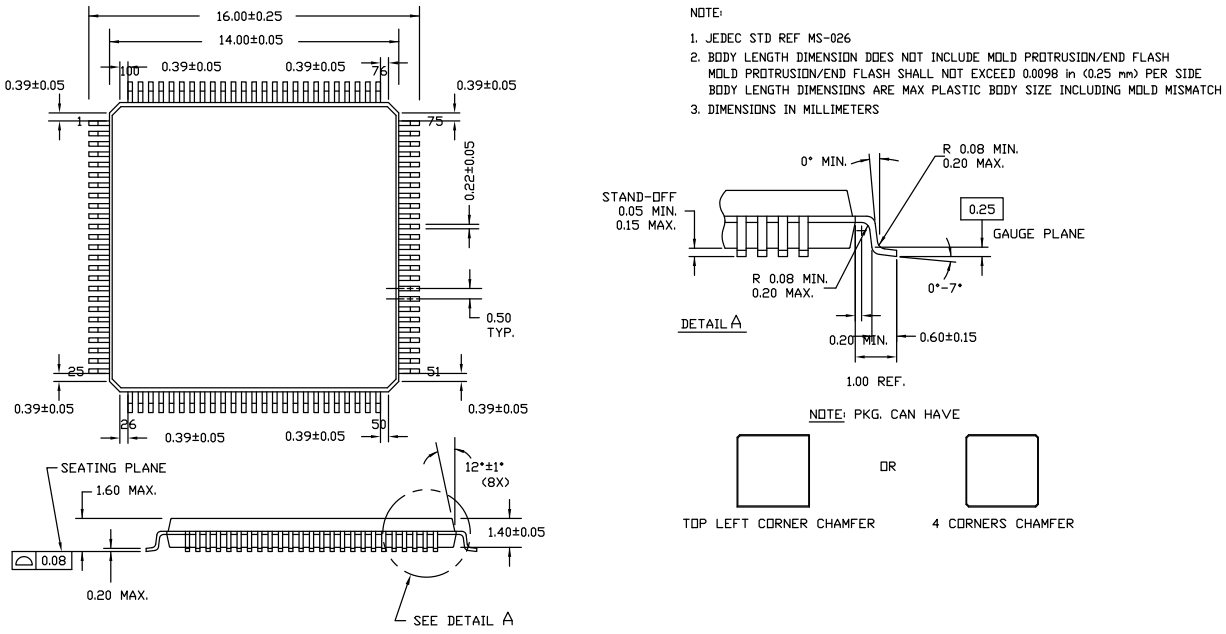
Table 12-1. CY8C38 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[70]				Package	JTAG ID[71]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks	Opamps	DFB	CapSense	UDBs[69]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
32 KB Flash																						
CY8C3845PVE-173	50	32	4	1	-	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	-	-	29	25	4	0	48-SSOP	0x1E0AD069
CY8C3865AXA-018	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	-	-	70	62	8	0	100-TQFP	0x1E012069
CY8C3865AXA-019	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	-	72	62	8	2	100-TQFP	0x1E013069
CY8C3865PVA-060	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	-	-	29	25	4	0	48-SSOP	0x1E03C069
CY8C3865PVA-063	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	-	31	25	4	2	48-SSOP	0x1E03F069
64 KB Flash																						
CY8C3846AXE-175	50	64	8	2	-	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	-	✔	70	62	8	0	100-TQFP	0x1E0AF069
CY8C3846AXE-176	50	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x1E0B0069
CY8C3846PVE-174	50	64	8	2	-	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E0AE069
CY8C3866AXA-035	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	-	✔	70	62	8	0	100-TQFP	0x1E023069
CY8C3866AXA-038	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	-	-	70	62	8	0	100-TQFP	0x1E026069
CY8C3866AXA-039	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	-	72	62	8	2	100-TQFP	0x1E027069
CY8C3866AXA-040	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x1E028069
CY8C3866AXA-055	67	64	8	2	-	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	-	✔	70	62	8	0	100-TQFP	0x1E037069
CY8C3866PVA-005	67	64	8	2	-	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	-	-	29	25	4	0	48-SSOP	0x1E005069
CY8C3866PVA-021	67	64	8	2	-	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	-	31	25	4	2	48-SSOP	0x1E015069
CY8C3866PVA-047	67	64	8	2	-	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E02F069
CY8C3866PVA-070	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E046069

Notes

69. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the "Example Peripherals" section on page 40 for more information on how UDBs may be used.
70. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the ""I/O System and Routing" section on page 33" for details on the functionality of each of these types of I/O.
71. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Figure 13-2. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048



51-85048 *I