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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866pva-070

1. Architectural Overview

Introducing the CY8C38 family of ultra low-power, flash Programmable System-on-Chip (PSoC®) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C38 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of automotive consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

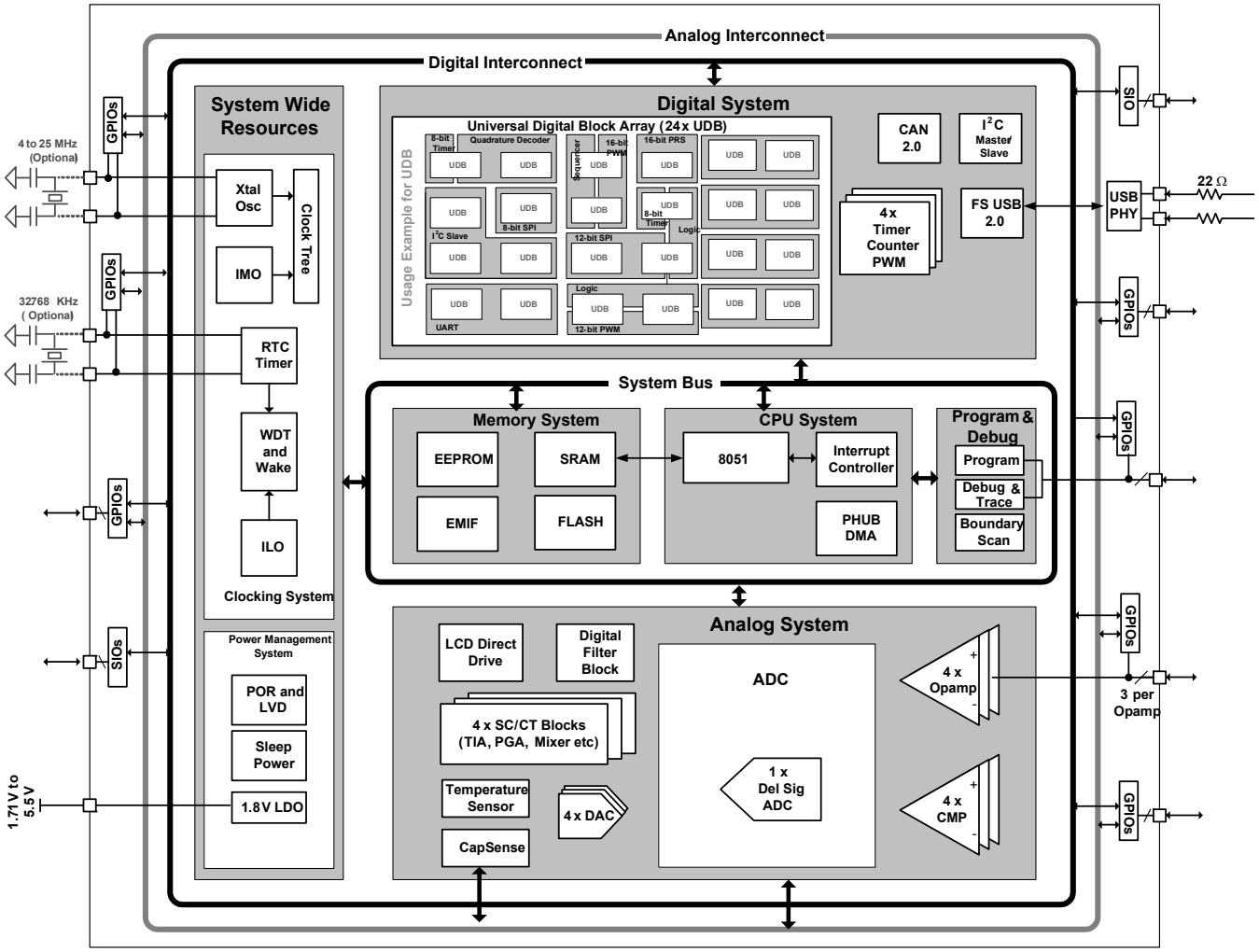


Figure 1-1 illustrates the major components of the CY8C38 family. They are:

- 8051 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C38 family these blocks can include four 16-bit timers, counters, and PWM blocks; I²C slave, master, and multimaster; FS USB; and Full CAN 2.0b.

4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase ‘subchains’ can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

Figure 4-2 on page 18 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 19 shows the interrupt structure and priority polling.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I^2C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	DFB Int	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

7.1.3 Example System Function Components

The following is a sample of the system function components available in PSoC Creator for the CY8C38 family. The exact amount of hardware resources (UDBs, DFB taps, SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- CapSense
- LCD drive
- LCD control
- Filters

7.1.4 Designing with PSoC Creator

7.1.4.1 More Than a Typical IDE

A successful design tool allows for the rapid development and deployment of both simple and complex designs. It reduces or eliminates any learning curve. It makes the integration of a new design into the production stream straightforward.

PSoC Creator is that design tool.

PSoC Creator is a full featured Integrated Development Environment (IDE) for hardware and software design. It is optimized specifically for PSoC devices and combines a modern, powerful software development platform with a sophisticated graphical design tool. This unique combination of tools makes PSoC Creator the most flexible embedded design platform available.

Graphical design entry simplifies the task of configuring a particular part. You can select the required functionality from an extensive catalog of components and place it in your design. All components are parameterized and have an editor dialog that allows you to tailor functionality to your needs.

PSoC Creator automatically configures clocks and routes the I/O to the selected pins and then generates APIs to give the application complete control over the hardware. Changing the PSoC device configuration is as simple as adding a new component, setting its parameters, and rebuilding the project.

At any stage of development you are free to change the hardware configuration and even the target processor. To retarget your application (hardware and software) to new devices, even from 8- to 32-bit families, just select the new device and rebuild.

You also have the ability to change the C compiler and evaluate an alternative. Components are designed for portability and are validated against all devices, from all families, and against all supported tool chains. Switching compilers is as easy as editing the from the project options and rebuilding the application with no errors from the generated APIs or boot code.

7.1.4.2 Component Catalog

The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC, DACs, and filters, and communication protocols, such as I^2C, USB, and CAN. See Example Peripherals on page 40 for more details about available peripherals. All content is fully characterized and carefully documented in data sheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

7.1.4.4 Software Development

Anchoring the tool is a modern, highly customizable user interface. It includes project management and integrated editors for C and assembler source code, as well the design entry tools.

Project build control leverages compiler technology from top commercial vendors such as ARM® Limited, Keil™, and CodeSourcery (GNU). Free versions of Keil C51 and GNU C Compiler (GCC) for ARM, with no restrictions on code size or end product distribution, are included with the tool distribution. Upgrading to more optimizing compilers is a snap with support for the professional Keil C51 product and ARM RealView™ compiler.

7.1.4.5 Nonintrusive Debugging

With JTAG (4-wire) and SWD (2-wire) debug connectivity available on all devices, the PSoC Creator debugger offers full control over the target device with minimum intrusion. Breakpoints and code execution commands are all readily available from toolbar buttons and an impressive lineup of windows—register, locals, watch, call stack, memory and peripherals—make for an unparalleled level of visibility into the system.

PSoC Creator contains all the tools necessary to complete a design, and then to maintain and extend that design for years to come. All steps of the design flow are carefully integrated and optimized for ease-of-use and to maximize productivity.

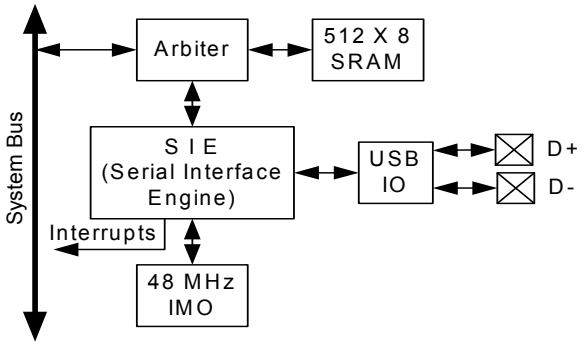
7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 33.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual memory management with no DMA access
  - Manual memory management with manual DMA access
  - Automatic memory management with automatic DMA access
- Internal 3.3-V regulator for transceiver
- Internal 48-MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB reset, suspend, and resume operations
- Bus-powered and self-powered modes

Figure 7-16. USB



7.7 Timers, Counters, and PWMs

The timer/counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in UDBs as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The timer/counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-17. Timer/Counter/PWM

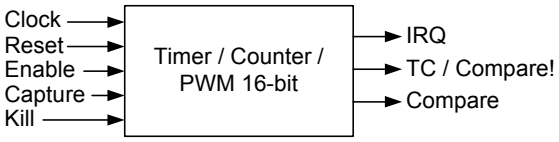
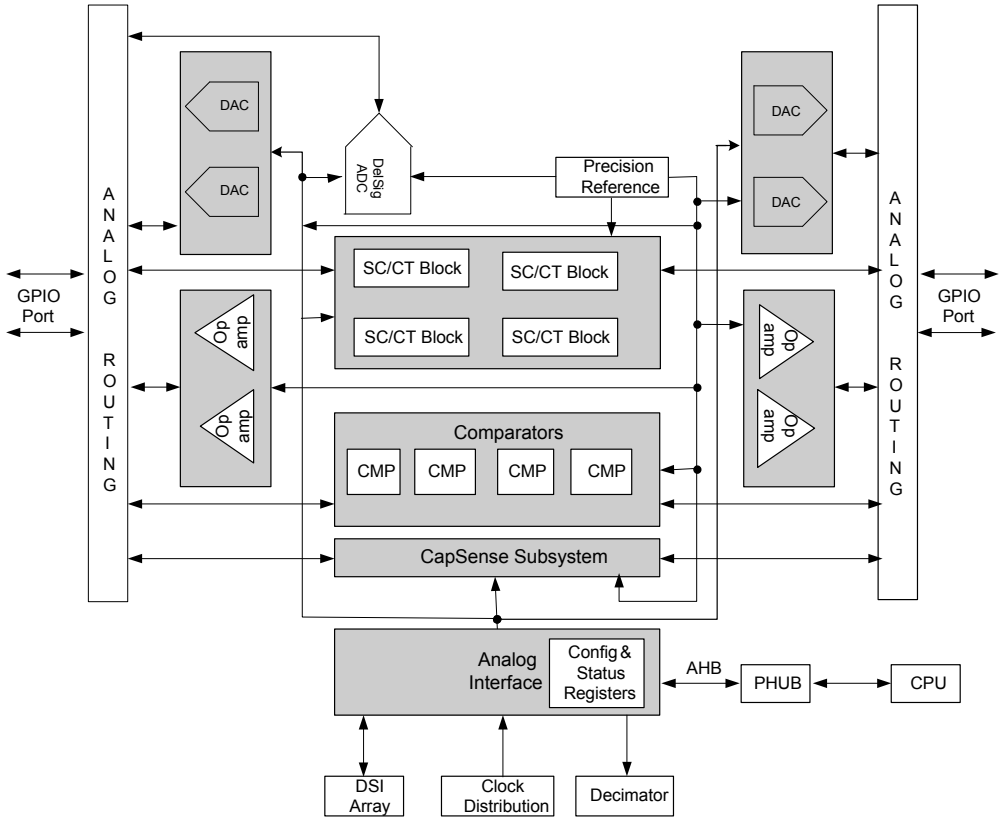


Figure 8-1. Analog Subsystem Block Diagram



The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

8.1 Analog Routing

The CY8C38 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

For information on how to make pin selections for optimal analog routing, refer to the application note, AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs.

8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- Eight analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the CY8C38 family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in CY8C38, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2 on page 53.

8.3.2 LUT

The CY8C38 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

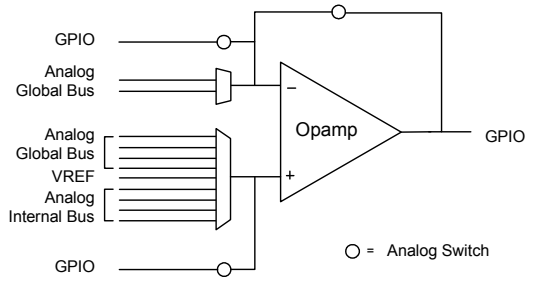
Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** (‘0’)
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** (‘1’)

8.4 Opamps

The CY8C38 family of devices contain up to four general purpose opamps in a device.

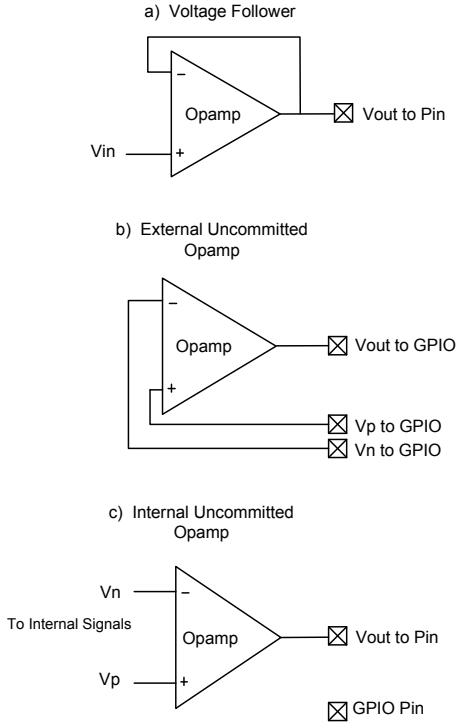
Figure 8-6. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-7. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-7. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

The CY8C38 family of devices contains up to four switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

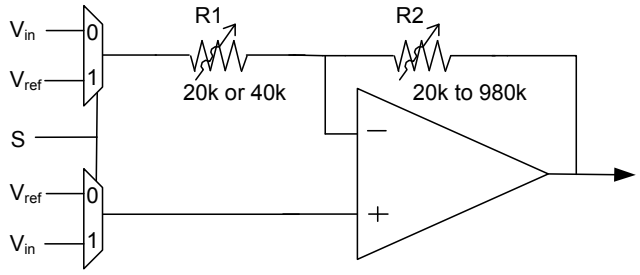
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8. The schematic in Figure 8-8 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	5.5 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-8. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

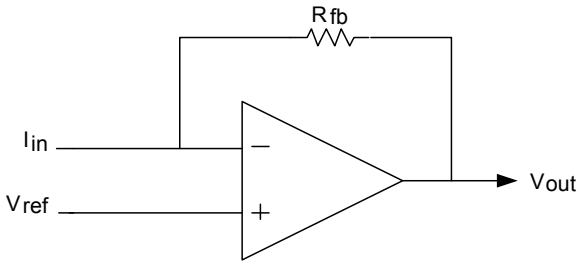
8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-9. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

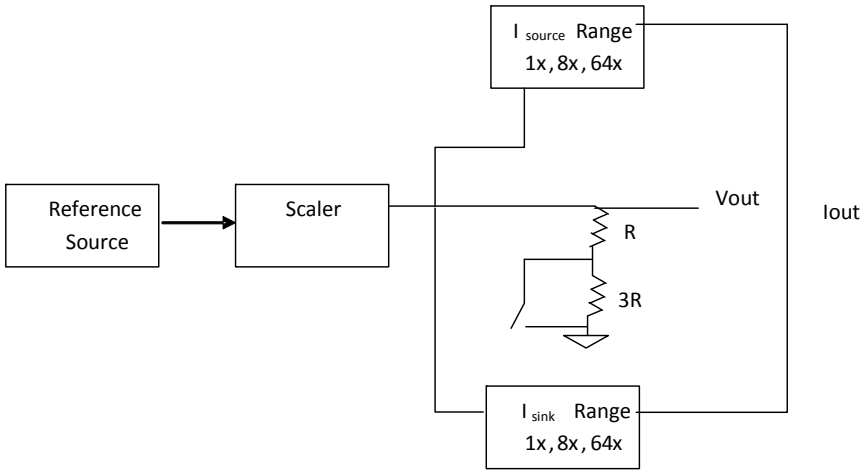
The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C38 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

8.9 DAC

The CY8C38 parts contain up to four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25 percent of gain error
- Source and sink option for current output
- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-11. DAC Block Diagram



8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.9.2 Voltage DAC

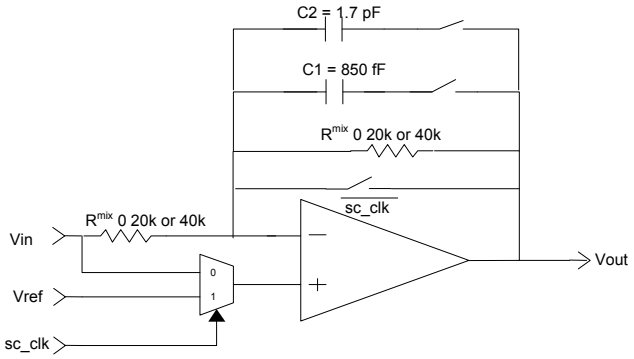
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk – Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-12. Mixer Configuration



8.11 Sample and Hold

The main application for a sample and hold, is to hold a value stable while an ADC is performing a conversion. Some applications require multiple signals to be sampled simultaneously, such as for power calculations (V and I).

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ	Max	Units
	Sleep Mode[26]						
	CPU OFF RTC = ON (= ECO32K ON, in low power mode) Sleep timer = ON (= ILO ON at 1 kHz) [27] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V–5.5 V	T = –40 °C	–	1.1	2.3	µA
			T = 25 °C	–	1.1	2.2	µA
			T = 85 °C	–	15	30	µA
			T = 125 °C	–	20.3	30	µA
		$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = –40 °C	–	1	2.2	µA
			T = 25 °C	–	1	2.1	µA
			T = 85 °C	–	12	28	µA
			T = 125 °C	–	18.5	28	µA
		$V_{CC} = V_{DDIO}$ = 1.71 V–1.95 V	T = 25 °C	–	2.2	4.2	µA
			T = 125 °C	–	16.2	28	µA
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I^2C Wake = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = 25 °C	–	2.2	2.7	µA
	I^2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = 25 °C	–	2.2	2.8	µA

Notes
26. If Vccd and Vcca are externally regulated, the voltage difference between Vccd and Vcca must be less than 50 mV.
27. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.

Figure 11-11. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

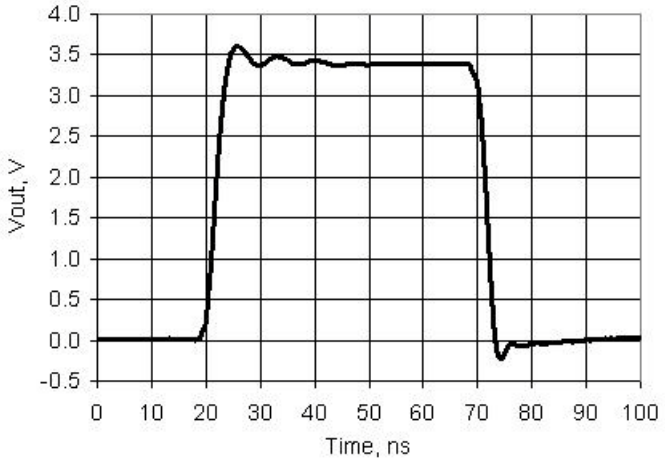


Figure 11-12. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

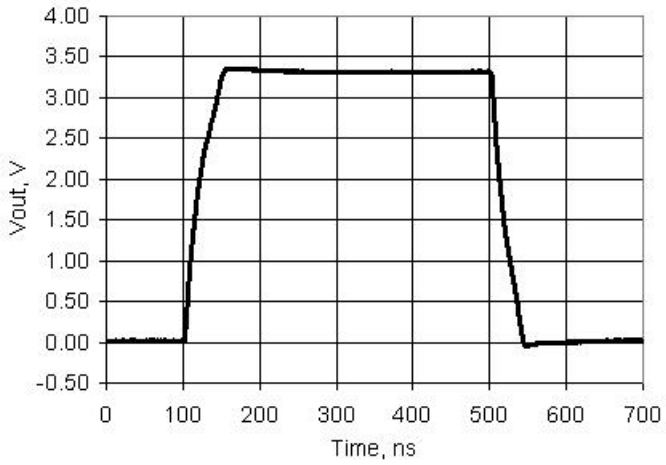


Figure 11-22. Opamp Step Response, Rising

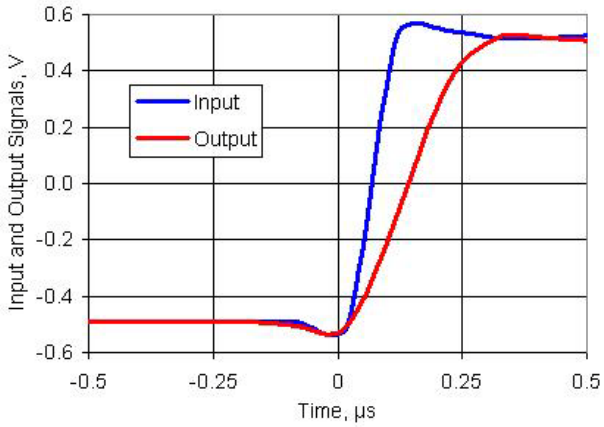
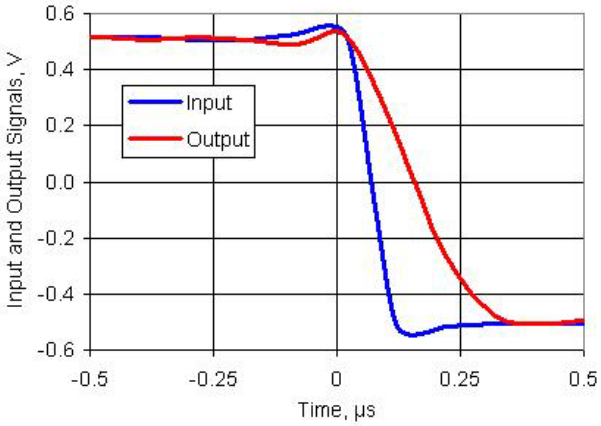


Figure 11-23. Opamp Step Response, Falling



11.5.2 Delta-Sigma ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- fclk = 3.072 MHz for resolution = 16 to 20 bits; fclk = 6.144 MHz for resolution = 8 to 15 bits
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-17. 20-bit Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	20	bits
	Number of channels, single ended		–	–	No. of GPIO	–
	Number of channels, differential	Differential pair is formed using a pair of GPIOs.	–	–	No. of GPIO/2	–
	Monotonic	Yes	–	–	–	–
Ge	Gain error	Buffered, buffer gain = 1, Range = ±1.024 V, 16-bit mode, 25 °C	–	–	±0.2	%
Gd	Gain drift	Buffered, buffer gain = 1, Range = ±1.024 V, 16-bit mode	–	–	50	ppm/°C
Vos	Input offset voltage	Buffered, 16-bit mode, full voltage range	–	–	±0.2	mV
		Buffered, 16-bit mode, V_{DDA} = 1.8 V ± 5%	–	–	±0.1	mV
TCVos	Temperature coefficient, input offset voltage	Buffer gain = 1, 16-bit, Range = ±1.024 V	–	–	1	µV/°C
	Input voltage range, single ended[36]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential unbuffered[36]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential, buffered[36]		V_{SSA}	–	V_{DDA} – 1	V
PSRRb	Power supply rejection ratio, buffered[36]	Buffer gain = 1, 16-bit, Range = ±1.024 V	90	–	–	dB
CMRRb	Common mode rejection ratio, buffered[36]	Buffer gain = 1, 16 bit, Range = ±1.024 V	85	–	–	dB
INL20	Integral non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±32	LSB
DNL20	Differential non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL16	Integral non linearity[36]	Range = ±1.024 V, unbuffered; 2.7 V ≤ V_{DDA} ≤ 5.5 V range	–	–	±2	LSB
		1.71 V ≤ V_{DDA} < 2.7 V range	–2.1	–	+2.7	LSB
DNL16	Differential non linearity[36]	Range = ±1.024 V, unbuffered; 2.7 V ≤ V_{DDA} ≤ 5.5 V range	–	–	±1	LSB
		1.71 V ≤ V_{DDA} < 2.7 V range	–1	–	+1.1	LSB
INL12	Integral non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL12	Differential non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL8	Integral non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL8	Differential non linearity[36]	Range = ±1.024 V, unbuffered	–	–	±1	LSB

Note
36. Based on device characterization (not production tested).

Figure 11-27. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

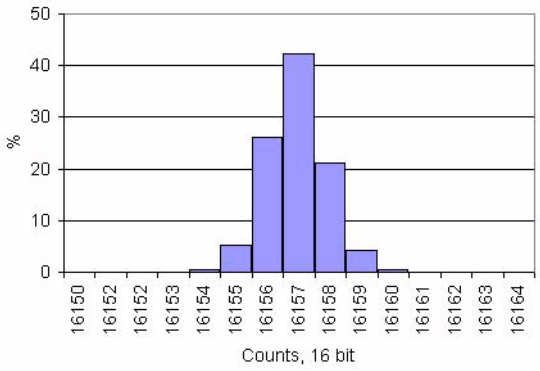


Table 11-20. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 16-bit, Internal Reference, Single Ended

Sample rate, sps	Input Voltage Range			
	0 to VREF	0 to VREF x 2	VSSA to VDDA	0 to VREF x 6
2000	1.21	1.02	1.14	0.99
3000	1.28	1.15	1.25	1.22
6000	1.36	1.22	1.38	1.22
12000	1.44	1.33	1.43	1.40
24000	1.67	1.50	1.43	1.53
48000	1.91	1.60	1.85	1.67

Table 11-21. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 16-bit, Internal Reference, Differential

Sample rate, sps	Input Voltage Range				
	±VREF	±VREF / 2	±VREF / 4	±VREF / 8	±VREF / 16
2000	0.56	0.65	0.74	1.02	1.77
4000	0.58	0.72	0.81	1.10	1.98
8000	0.53	0.72	0.82	1.12	2.18
15625	0.58	0.72	0.85	1.13	2.20
32000	0.60	0.76	INVALID OPERATING REGION		
43750	0.58	0.75			
48000	0.59				

Table 11-22. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 20-bit, External Reference, Single Ended

Sample rate, sps	Input Voltage Range			
	0 to VREF	0 to VREF x 2	VSSA to VDDA	0 to VREF x 6
8	1.28	1.24	6.02	0.97
23	1.33	1.28	6.09	0.98
45	1.77	1.26	6.28	0.96
90	1.65	0.91	6.84	0.95
187	1.87	1.06	7.97	1.01

Table 11-23. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 20-bit, External Reference, Differential

Sample rate, sps	Input Voltage Range				
	±VREF	±VREF / 2	±VREF / 4	±VREF / 8	±VREF / 16
8	0.70	0.84	1.02	1.40	2.65
11.3	0.69	0.86	0.96	1.40	2.69
22.5	0.73	0.82	1.25	1.77	2.67
45	0.76	0.94	1.02	1.76	2.75
61	0.75	1.01	1.13	1.65	2.98
170	0.75	0.98	INVALID OPERATING REGION		
187	0.73				

Figure 11-28. Delta-sigma ADC DNL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V

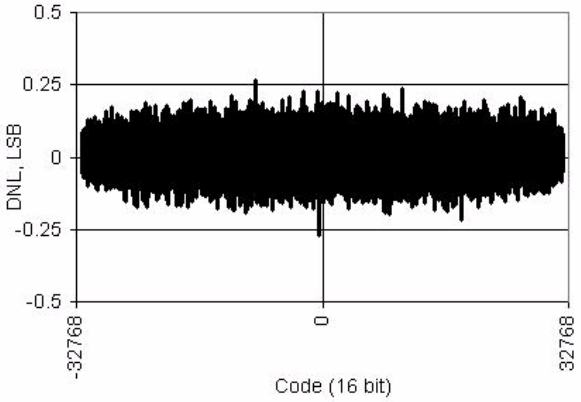
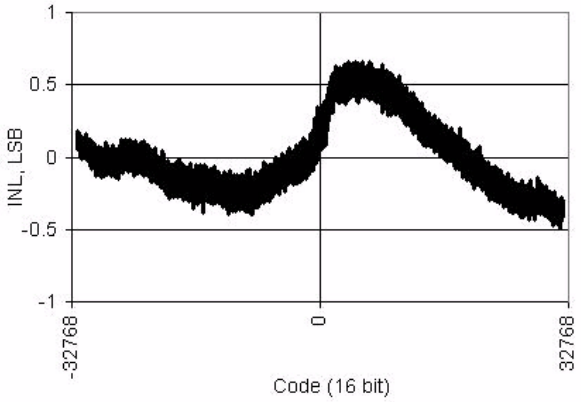


Figure 11-29. Delta-sigma ADC INL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V



11.5.6 IDAC

All specifications are based on use of the low-resistance IDAC output pins (see Pin Descriptions on page 9 for details). See the IDAC component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-28. IDAC (Current Digital-to-Analog Converter) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Resolution			-	8	-	
I_{OUT}	Output current at code = 255	Range = 2.04 mA, code = 255, $V_{DDA} \geq 2.7$ V, Rload = 600 Ω	–	2.04	–	mA
		Range = 2.04 mA, high speed mode, code = 255, $V_{DDA} \leq 2.7$ V, Rload = 300 Ω	–	2.04	–	mA
		Range = 255 µA, code = 255, Rload = 600 Ω	–	255	–	µA
		Range = 31.875 µA, code = 255, Rload = 600 Ω	–	31.875	–	µA
	Monotonicity		–	–	Yes	
INL	Integral nonlinearity	Sink mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.9	±1	LSB
		Source mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±1.2	±1.6	LSB
DNL	Differential nonlinearity	Sink mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
Ezs	Zero scale error	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	0	±1	LSB
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	±2	LSB
Eg	Gain error	Range = 2.04 mA, 25 °C	–	–	±2.5	%
		Range = 255 µA, 25 ° C	–	–	±2.5	%
		Range = 31.875 µA, 25 ° C	–	–	±3.5	%
TC_Eg	Temperature coefficient of gain error	Range = 2.04 mA	–	–	0.04	% / °C
		Range = 255 µA	–	–	0.04	% / °C
		Range = 31.875 µA	–	–	0.05	% / °C
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to Vdda or Rload to Vssa, Vdiff from Vdda	1	–	–	V

Figure 11-33. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

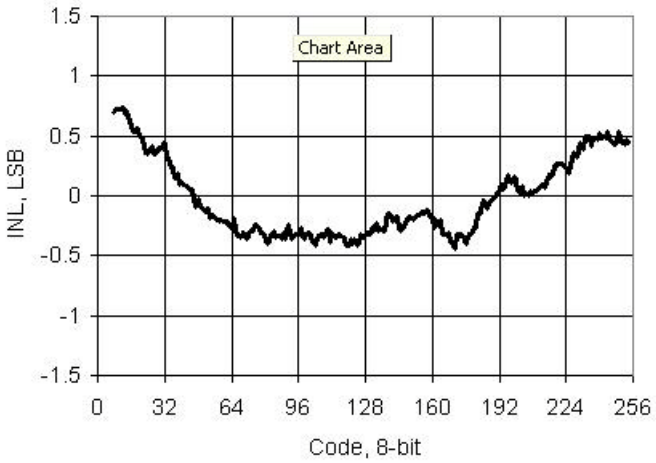


Figure 11-34. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

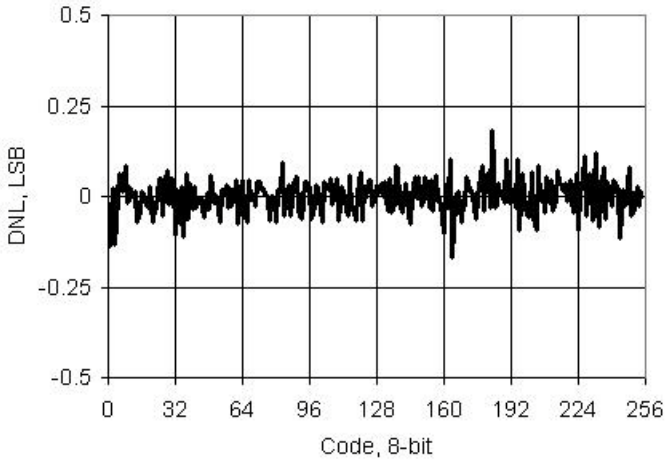
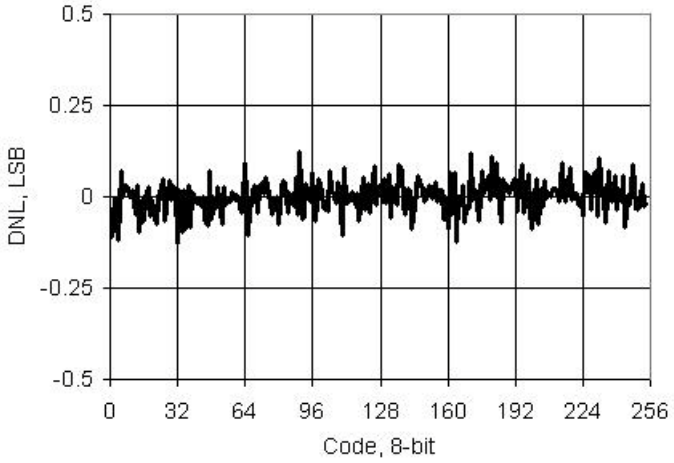


Figure 11-35. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode



11.7 Memory

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-55. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	Vddd pin	1.71	-	5.5	V

Table 11-56. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Twrite	Block write time (erase + program)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	15	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	15	ms
Terase	Block erase time	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	10	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	10	ms
	Block program time	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	5	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	5	ms
Tbulk	Bulk erase time (16 KB to 64 KB)[53]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	35	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	35	ms
	Sector erase time (8 KB to 16 KB)[53]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	15	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	15	ms
	Total device program time (including JTAG, etc.)	No overhead [54]	-	-	5	seconds
	Flash data retention time [55]	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Retention period measured from last erase cycle after 100k progra/erase cycles at T_A ≤ 85 °C	10	–	–	

Notes
53. ECC not included.
54. See PSoC® 3 Device Programming Specifications for a description of a low-overhead method of programming PSoC 3 flash. (Please take care of Foot note numbers)
55. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +125 °C ambient temperature range. Contact customercare@cypress.com.

11.8.3 Interrupt Controller

Table 11-71. Interrupt Controller AC Specifications

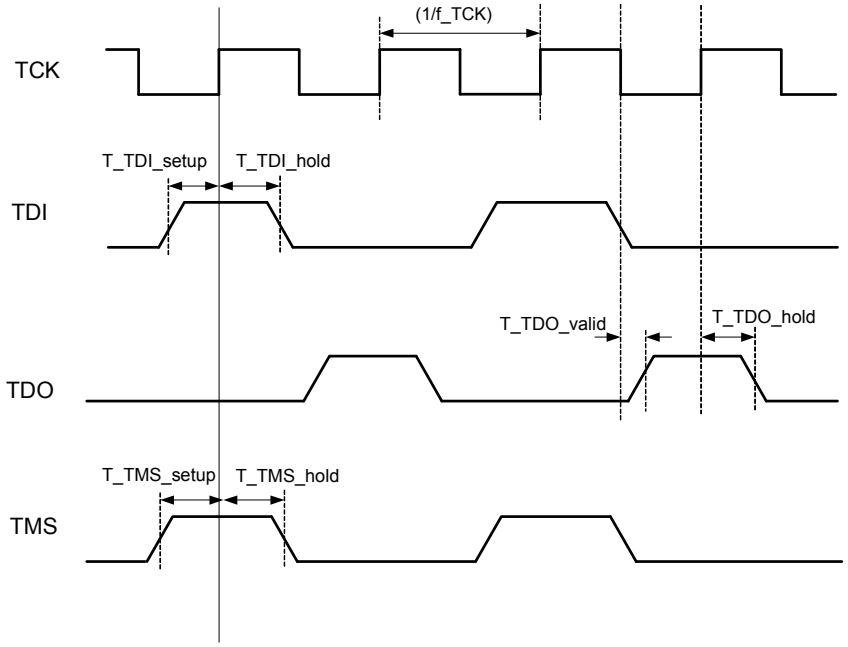
Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from Interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	-	-	25	Tcy CPU

11.8.4 JTAG Interface

Table 11-72. JTAG Interface AC Specifications[30]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14[60]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[60]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10) – 5	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	–	–	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	–	–	

Figure 11-65. JTAG Interface Timing



11.9 Clocking

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.9.1 Internal Main Oscillator

Table 11-75. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	62.6 MHz		–	–	600	µA
	48 MHz		–	–	500	µA
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	µA
	24 MHz – non USB mode		–	–	300	µA
	12 MHz		–	–	200	µA
	6 MHz		–	–	180	µA
	3 MHz		–	–	150	µA

Figure 11-67. IMO Current vs. Frequency